
AT478-A/B, AT481-A/B IOU AND ASSOCIATED EQUIPMENT

BOARD TYPES:

JA	JF
JC/JU	JG
JD	JH
JE/JV	JJ

L4 DIAGRAMS

VOLUME 2, BOOK 1 OF 3

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (08-20-86)	Preliminary release.
B (11-07-86)	Manual released and revised to include ECO 47746.
C (11-07-86)	Manual revised to include FCO 48197.
D (11-07-86)	Manual revised to include ECO 48326.
E (11-07-86)	Manual revised to include ECO 48400. This edition obsoletes all previous editions. This publication has been divided into two volumes (publication numbers 60462210 and 60463540).
F (06-15-87)	Manual revised to include ECO 48318, changes both versions of JA-01, -02, -06, -11, and -12.
G (06-15-87)	Manual revised to include ECO 48478, changes JK-01, -07, and -20.
H (06-15-87)	Manual revised to include ECO 48479, changes JZ(22113019)-01, -08 through -13, -22, -25, and -28 and deletes JZ(53575518)-01 through -29; ECO 48330, changes JD-01 and -05, JL-01 and -10, JQ-01 and -17, JR(53575515)-01 and -10, JR(22105675)-01, -09, and -10, both versions of JS-01 and -23, JT-01 and -08, JW(53575537)-01 and -17, and JX(53575512)-01 and -05. This edition also adds KX-01 through -21, KZ-01 through -22 LZ-01 through -23, and LX-01 through -13; and changes A-1 and A-2. ECO 48628, changes KZ-01, -02, -18, and -21; and ECO 48633, changes JK-01 and -22.
J (01-15-88)	Manual revised to include ECO 48633, affected diagrams (JK-01 and -22) included in revision H edition.
K (01-15-88)	Manual revised to include FCO 48632, changes both versions of JE/JV-01 and -04 through 07. This edition also includes ECOs 48483 and 48860. ECO 48483 changes JG (53575506) -01 and -09. ECO 48860 changes both versions of JF-01, 14, and 17; JE/JV (22105672) -01, 15, and 17; both versions of JC/JU-01, -19, and -22.
L (01-15-88)	Manual revised to include FCO 48862, changes KX-01, -05, -08, -09, -13, and -15; KZ-01, -16, and -18. This edition also includes ECOs 48855 and 49123. ECO 48855 changes LX-01, -08, -09, -11, and -12; LZ-01 and -21. ECO 49123 changes JQ-01, -03, -11, -12, -13, and -16; JM-01 and -26.
M (08-05-88)	Manual revised to include FCO 49637. Also includes ECOs 49486, 49487, and 49505. Changes pages 4-57, 4-75, 4-85, 4-97, 4-141, 4-153 through 4-157, 4-159, 4-171 through 4-175, 4-199, 4-212, 4-217, and 4-219 in book 1; 4-431, 4-432, 4-473 through 4-502, 4-527, 4-540, 4-555, 4-557, 5-576, 4-595, 4-597, 4-608, and 4-616 in book 2; 4-725, 4-726, 5-755, 4-776, 4-783, 4-804, 4-841, 4-868, 4-927, 4-935, and 4-936 in book 3.
N (08-05-88)	Field Change Order 49705. No change to manual.
P (08-05-88)	Manual revised to include ECO 49723. Changes pages 4-660 in book 2; A-1 and A-2 in book 3. Pages 4-660.1 through 4-660.12 in book 2 are added.
Publication No. 60462210	

REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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this manual.

REVISION RECORD

REVISION	DESCRIPTION
Publication No. 60462210	

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AT478-A	01	-	Released
	02	47441	
	03	47450	
	04	ECO 47840	
	05	47727	
	06	47740	
	07	47748	
	08	48197	
	09	48326	
	10	48400	
	11	48318	
	12	48478	
	13	48631	
	14	48632	
	15	ECO 48404	
AT478-B	01	-	Released
AT481-A	01	-	Released
	02	ECO 47840	
	03	47748	
	04	48326	
	05	48400	
	06	48318	
	07	ECO 48494	
	08	48632	
	09	ECO 49485	
AT481-B	01	-	Released
AT482-A	01	-	Released
	02	ECO 49485	
	03	ECO 49494	
AT482-B	01	-	Released
AT490-A	01	-	Released
	02	48479	
	03	ECO 49485	
	04	ECO 49484	
AT490-B	01	-	Released
AT497-A	01	-	Released
	02	ECO 49485	
	03	49637	
	04	ECO 49494	
AT497-B	01	-	Released

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AT498-A	01	-	Released
	02	48862	
	03	ECO 49485	
	04	ECO 49494	
AT498-B	01	-	Released
AT501-A	01	-	Released
AT501-B	01	-	Released
AT501-C	01	-	Released
AT509-A	01	-	Released
AT510-A	01	-	Released

This manual contains the multi-level diagram set for:

- AT478-A Non-Concurrent Input/Output Unit (NIO)
- AT478-B Non-Concurrent Input/Output Unit (NIO)
- AT481-A 1st Concurrent PP Increment Input/Output Unit (CIO)
- AT481-B 1st Concurrent PP Increment Input/Output Unit (CIO)
- AT482-A 2nd Concurrent PP Increment Input/Output Unit (CIO)
- AT482-B 2nd Concurrent PP Increment Input/Output Unit (CIO)
- AT490-A Intelligent Standard Interface (ISI) Channel Adapter
- AT490-B Intelligent Standard Interface (ISI) Channel Adapter
- AT497-A Intelligent Peripheral Interface (IPI) Channel Adapter
- AT497-B Intelligent Peripheral Interface (IPI) Channel Adapter
- AT498-A Direct Memory Access (DMA) Enhanced C170 Channel Adapter
- AT498-B Direct Memory Access (DMA) Enhanced C170 Channel Adapter
- AT501-A CYBER 990 Secondary I4 Conversion Kit
- AT501-B CYBER 840/850/860 Secondary I4 Conversion Kit
- AT501-C CYBER 992 Secondary I4 Conversion Kit
- AT509-A I4 to PIP3 CM Interface
- AT510-A I4 to 8XX/990 CM Interface

Level 4 diagrams consist of logic diagrams for each board in panels A through D. Where a board is used in more than one location, the signal names (both English names and the six-character identifiers used in the wire list) shown on the level 4 diagram apply to the first occurrence of that board only. The first occurrence is the location that is listed first on the board's level 4 diagram cover sheet. Most pins on multi-occurrence boards have a parallel function that can be determined by referring to the wire list and to level 2 diagrams.

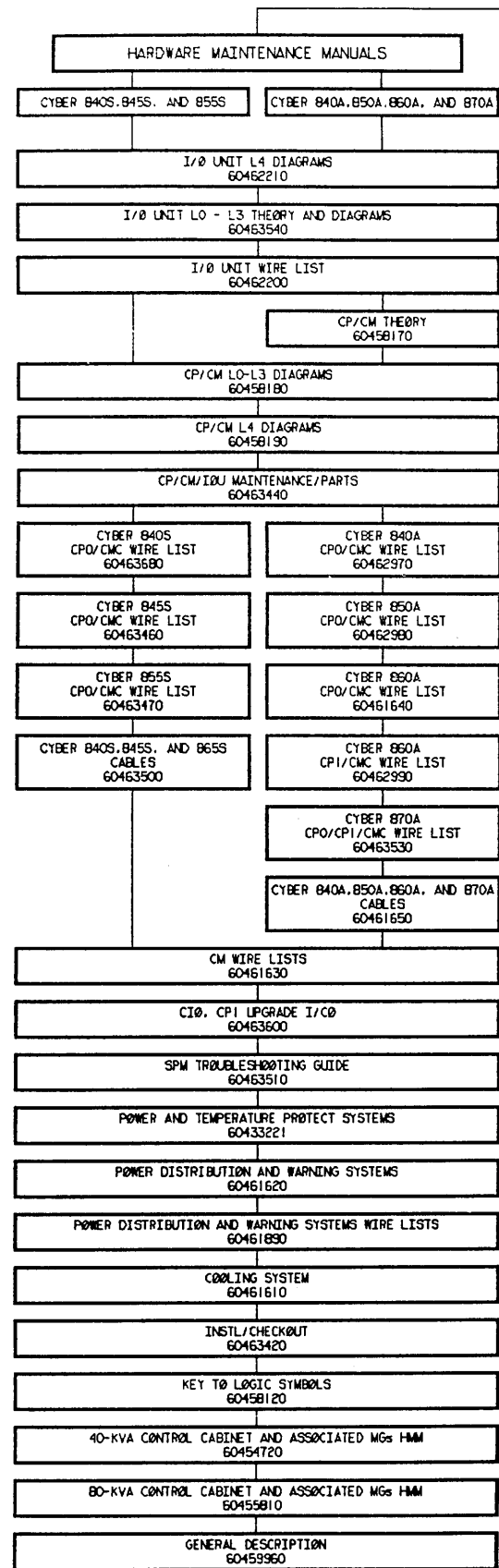
CAUTION

Some boards have two layouts, both of which are used and supported. The two layouts for each of these boards are included in this manual. It is important to check the board number in your unit and compare it to the board master (B/M) number on the appropriate level 4 diagram to be sure they match.

The System Publication Indexes on the following page include other manuals that are applicable to the equipment.

SYSTEM PUBLICATION INDEX

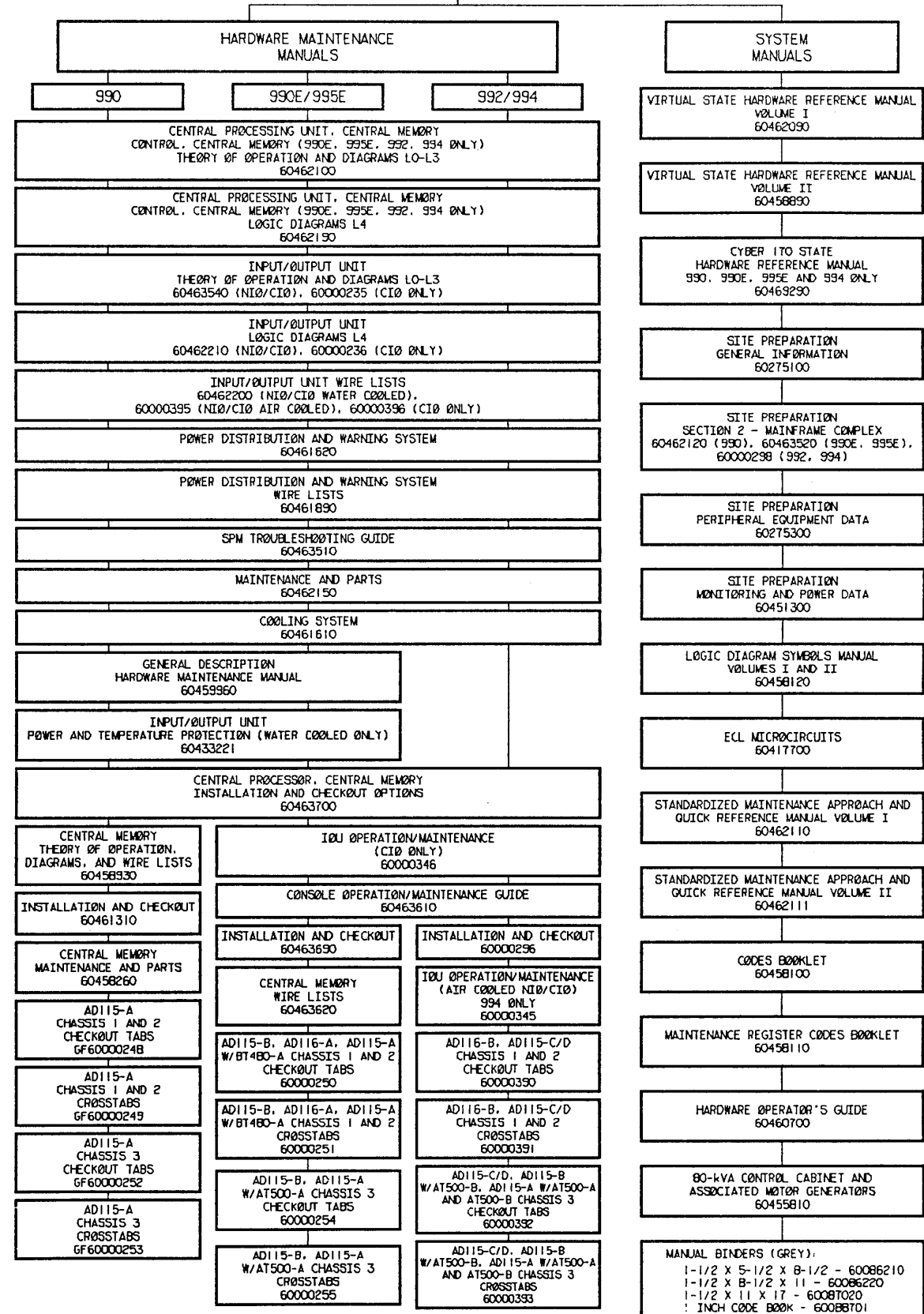
CYBER B40S, B45S, B55S, B40A, B50A, B60A, AND B70A
HARDWARE MANUALS



SYINDEX B55 S
60463640-14-A

SYSTEM PUBLICATION INDEX

CDC CYBER 180 MODEL 990
CDC CYBER 990E, 995E, 992, 994
HARDWARE MANUALS



SYINDEX 990 E
60463640-15-B

VOLUME 1

- 1. LEVEL 0 and 1 DIAGRAMS
- 2. LEVEL 2 DIAGRAMS
- 3A. LEVEL 3 DIAGRAMS
- 3B. 170 DMA LEVELS 0-3
- 3C. IPI LEVELS 0-3

APPENDIX

A ABBREVIATIONS

VOLUME 2

1-1	4. LEVEL 4 DIAGRAMS ①
2-1	BOOK 1
3A-1	Panel A
3B-1	JA† 53575500. 4-1
3C-1	JA† 22105670. 4-15
	JC/JU 53575502. 4-29
	JC/JU 22105671. 4-57
	JD 4-85
	JE/JV 53575504. 4-101
	JE/JV 22105672. 4-121
A-1	JF 53575505. 4-141
	JF 22105620. 4-159
	JG 53575506. 4-177
	JG 22105673. 4-199
	JH 53575507. 4-221
	JH 22105679. 4-251
	JJ 53575508. 4-281
	JJ 22105674. 4-305

① Two sets of logic diagrams are provided for a board that has two layouts. The appropriate logic diagram set has a board master (B/M) number that matches the printed wiring board (PWB) number of the board.

†Also in panel C.

Panel A

JQ	4-329
JR	53575515.	4-351
JR	22105675.	4-363
JS†	53575516.	4-375
JS†	22130333.	4-403
JT†	4-431
HR	4-660.1

Panel B

CQ	4-447
HK/JK	4-473
JL	4-503
JM	4-527
JW††	53575537.	4-555
JW	22105621.	4-595
KB††	4-635
KR	(Diagrams are located in book 3)	

Panels C and D

KR†††	4-661
JX	53575512.	4-695
JX	22105623.	4-725
JY	53575513.	4-755
JY	22105622.	4-783
JZ	4-841
KA	22127690.	4-871
KA	22105610.	4-877
KX	4-883
KZ	4-905
LX	4-927
LZ	4-941

APPENDIX

A PANEL MAPS

†Also in panel D.
††Also in panels C and D.
†††Also in panel B

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

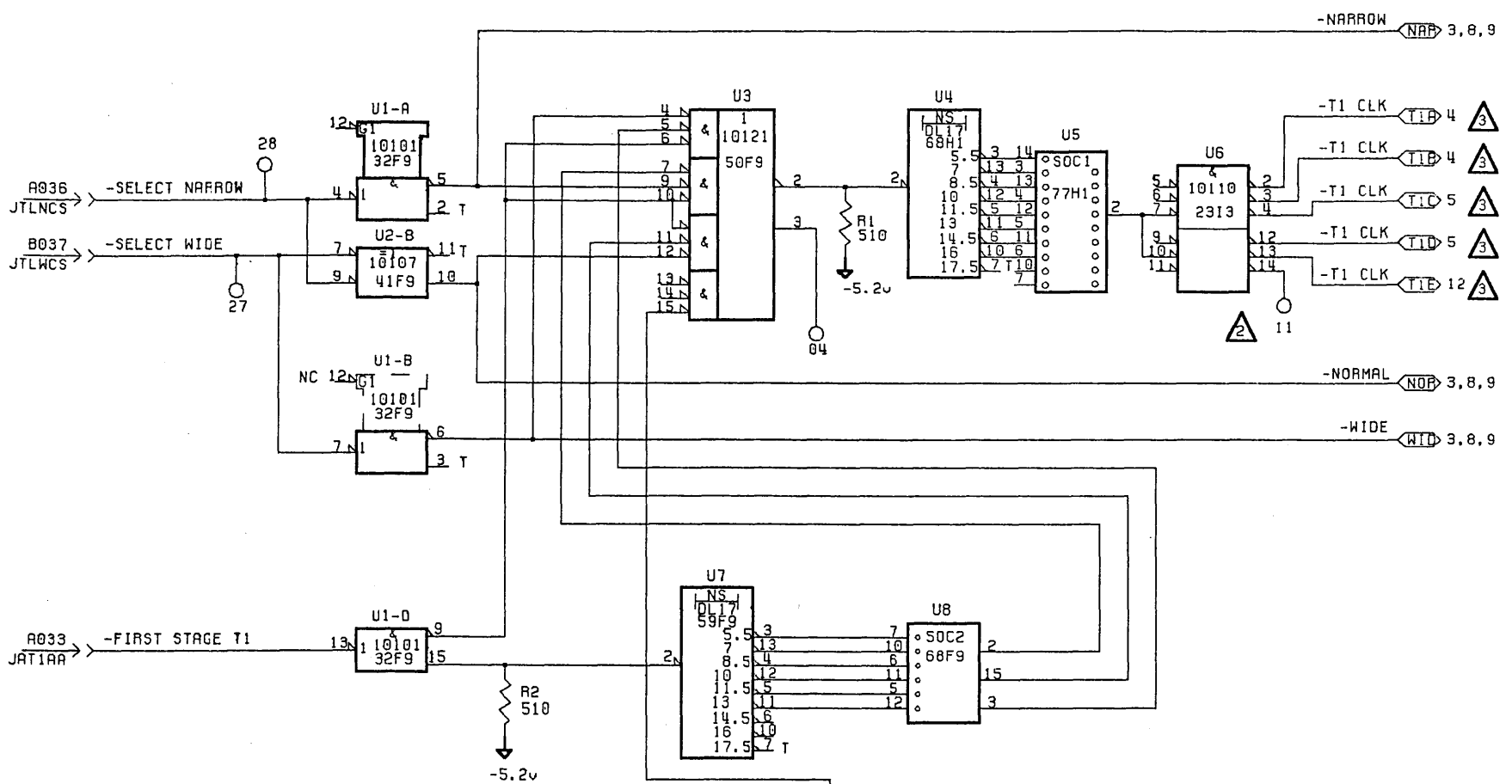
CLOCK BOARD

DWN	L H JOHNSON	11/01/85
CHKO	D R FORD	12/04/85
ENG	J P STROMBECK	12/04/85
PUBS	R K BONDE	12/04/85
APP	J P STROMBECK	12/04/85

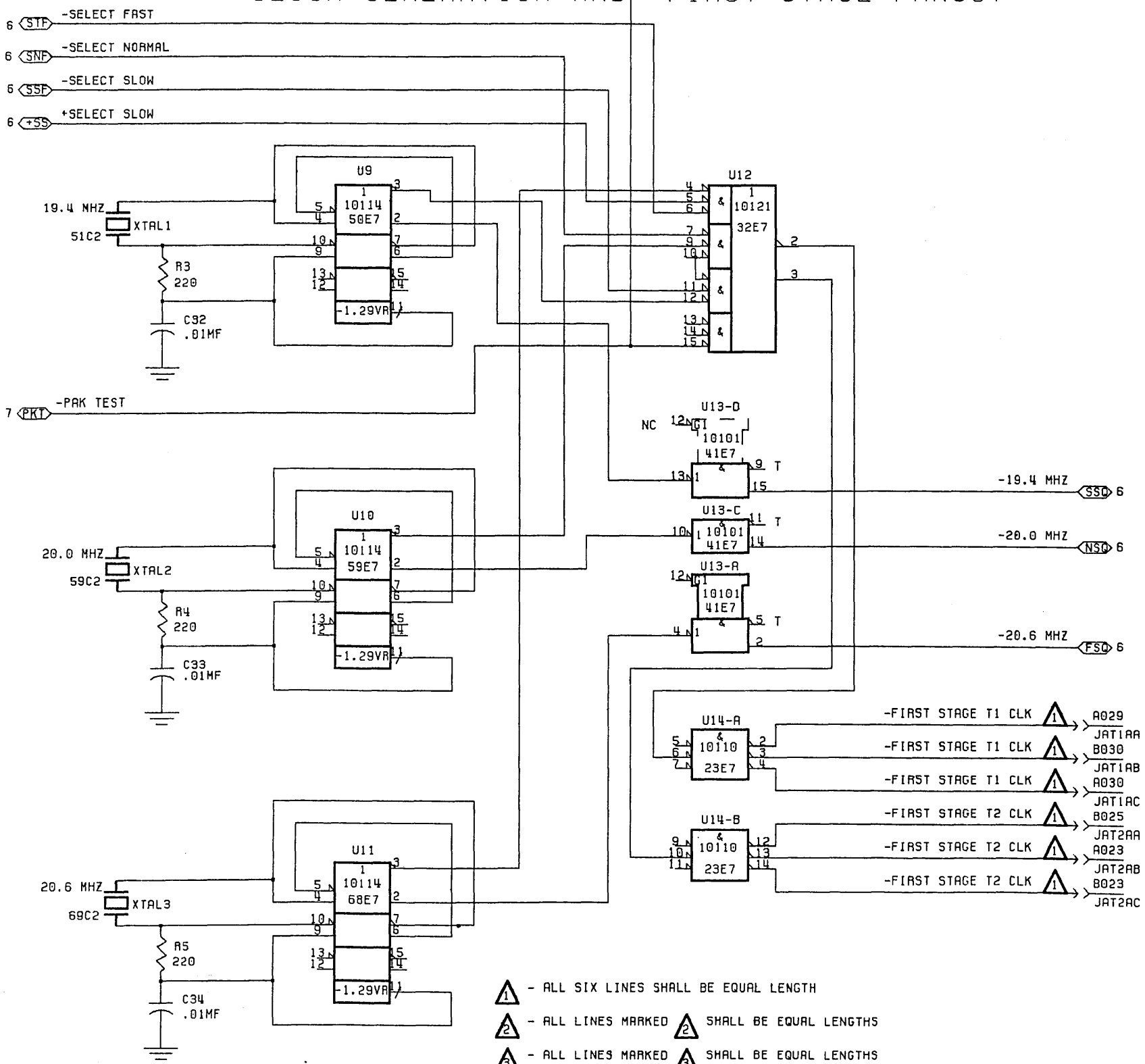
LOC: A31 C28

60462210 F

T1 CLOCK PULSE SHAPING



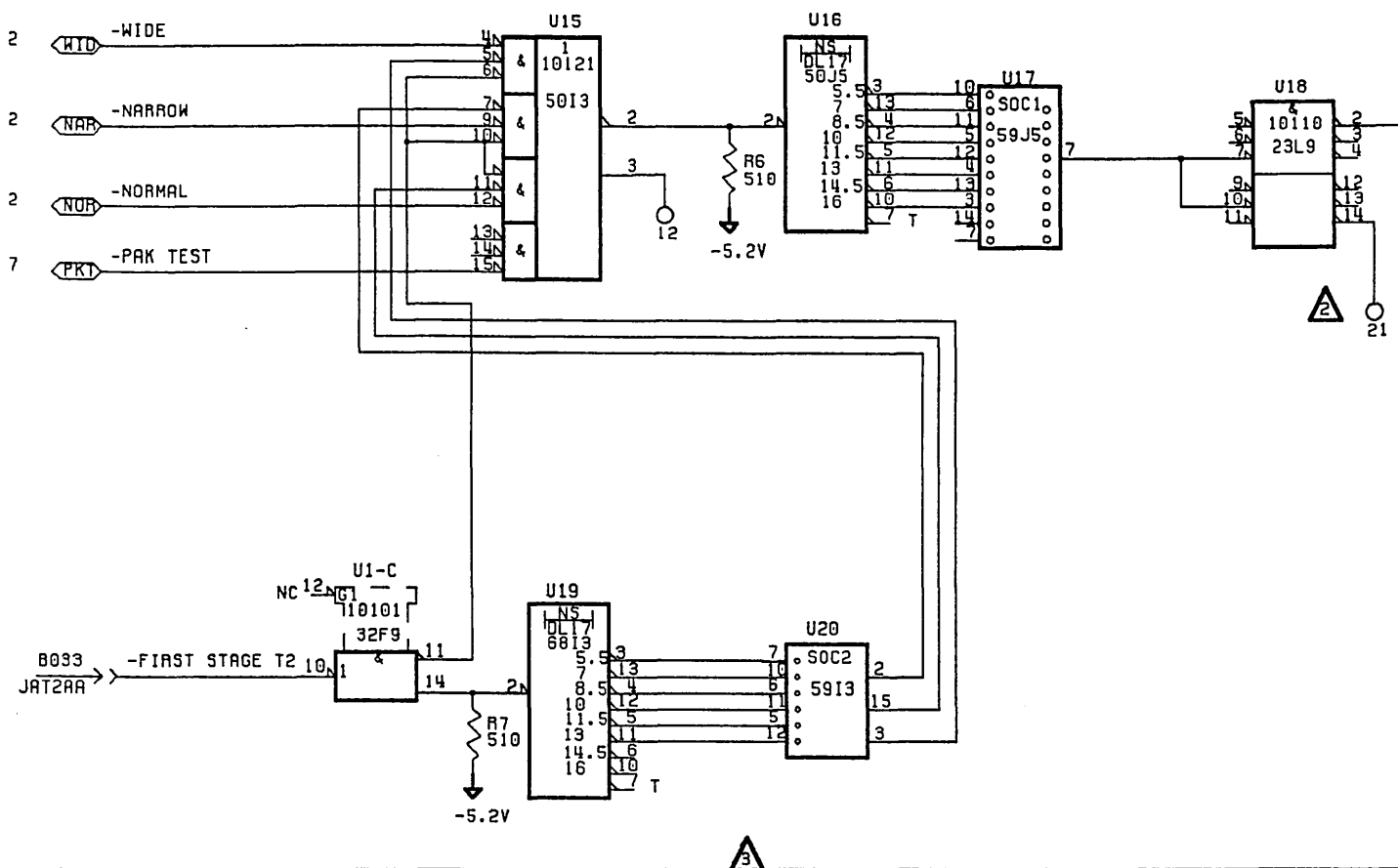
CLOCK GENERATION AND FIRST STAGE FANOUT



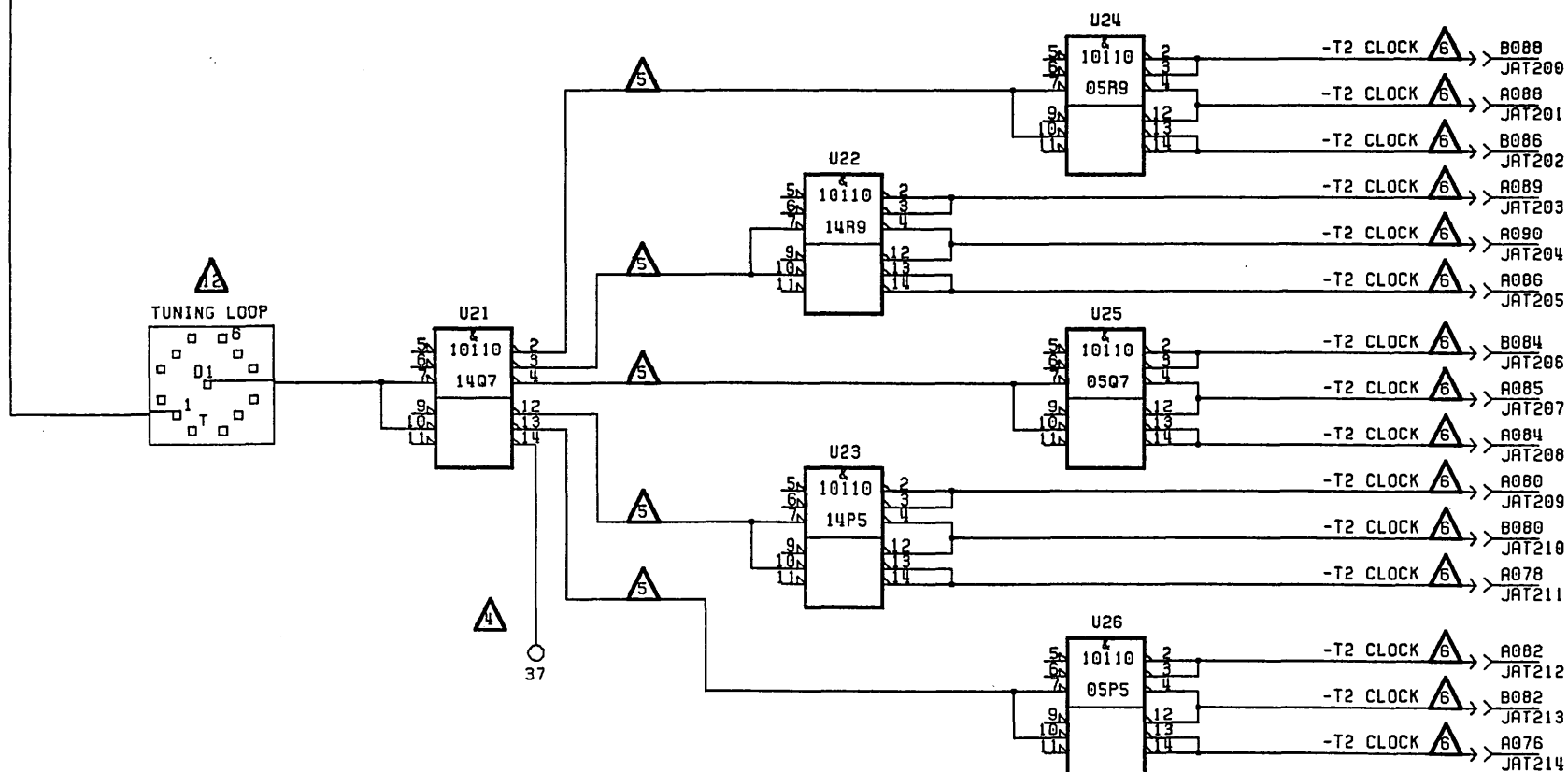
- ① - ALL SIX LINES SHALL BE EQUAL LENGTH
- ② - ALL LINES MARKED ② SHALL BE EQUAL LENGTHS
- ③ - ALL LINES MARKED ③ SHALL BE EQUAL LENGTHS

CD CONTROL DATA	14 CLOCK BOARD T1 CLOCK PULSE SHAPING AND CLK GENERATION & FIRST STAGE F/O TYPE 1JAH	8	DWG NO. 53575500	DATE 12/15/86	REV C
			SHEET NO. 2	60462210	PAGE JR-02


T2 CLOCK PULSE GENERATION



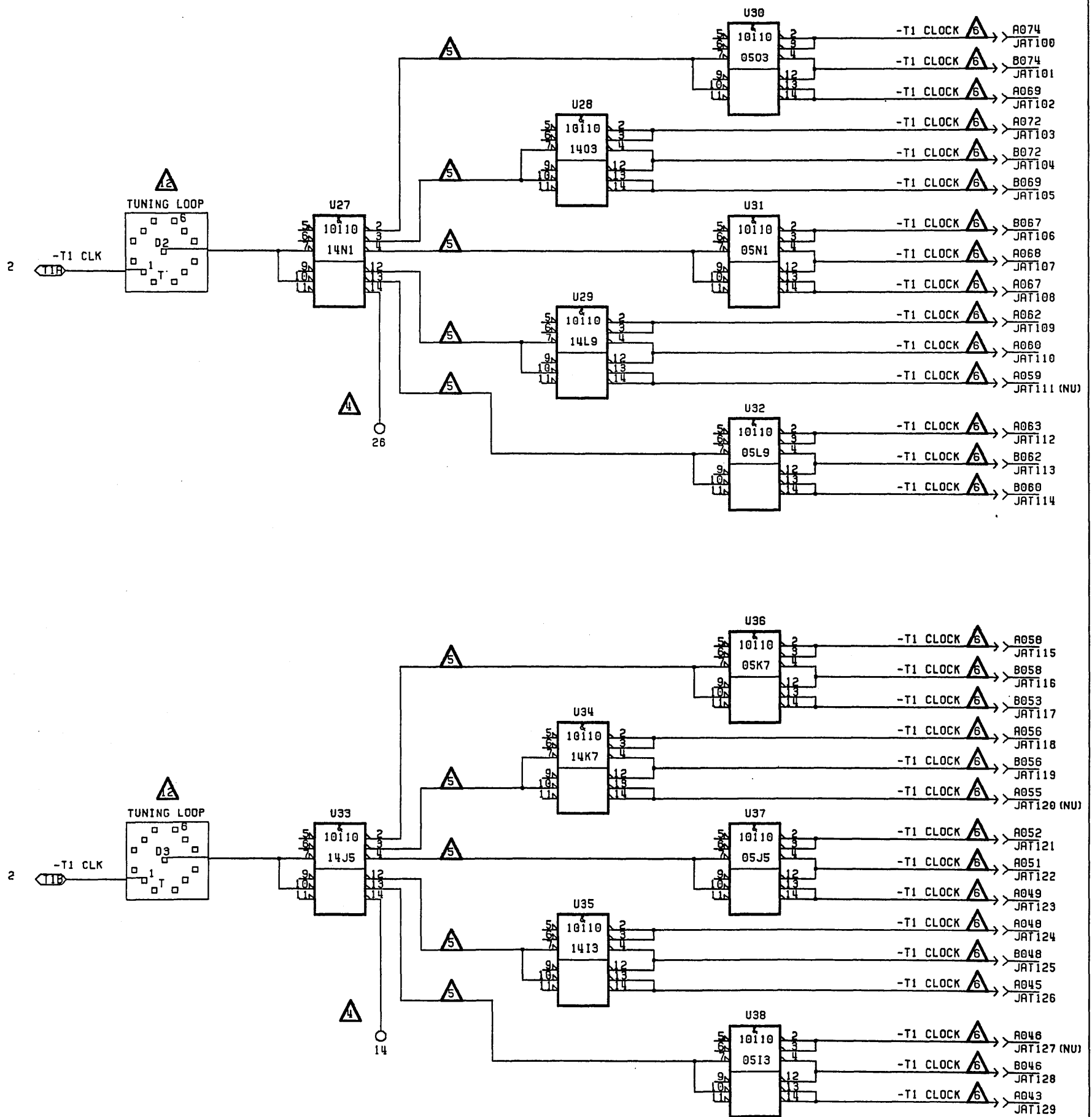
T2 CLOCK FANOUT




- 2 - ALL LINES MARKED 2 SHALL BE EQUAL LENGTHS
 3 - ALL LINES MARKED 3 SHALL BE EQUAL LENGTHS
 4 - ALL LINES MARKED 4 SHALL BE EQUAL LENGTHS
 5 - ALL LINES MARKED 5 SHALL BE EQUAL LENGTHS
 6 - ALL LINES MARKED 6 SHALL BE EQUAL LENGTHS
 12 FIRST 10 TAPS 0.2 NS, LAST 2 TAPS 0.4 NS

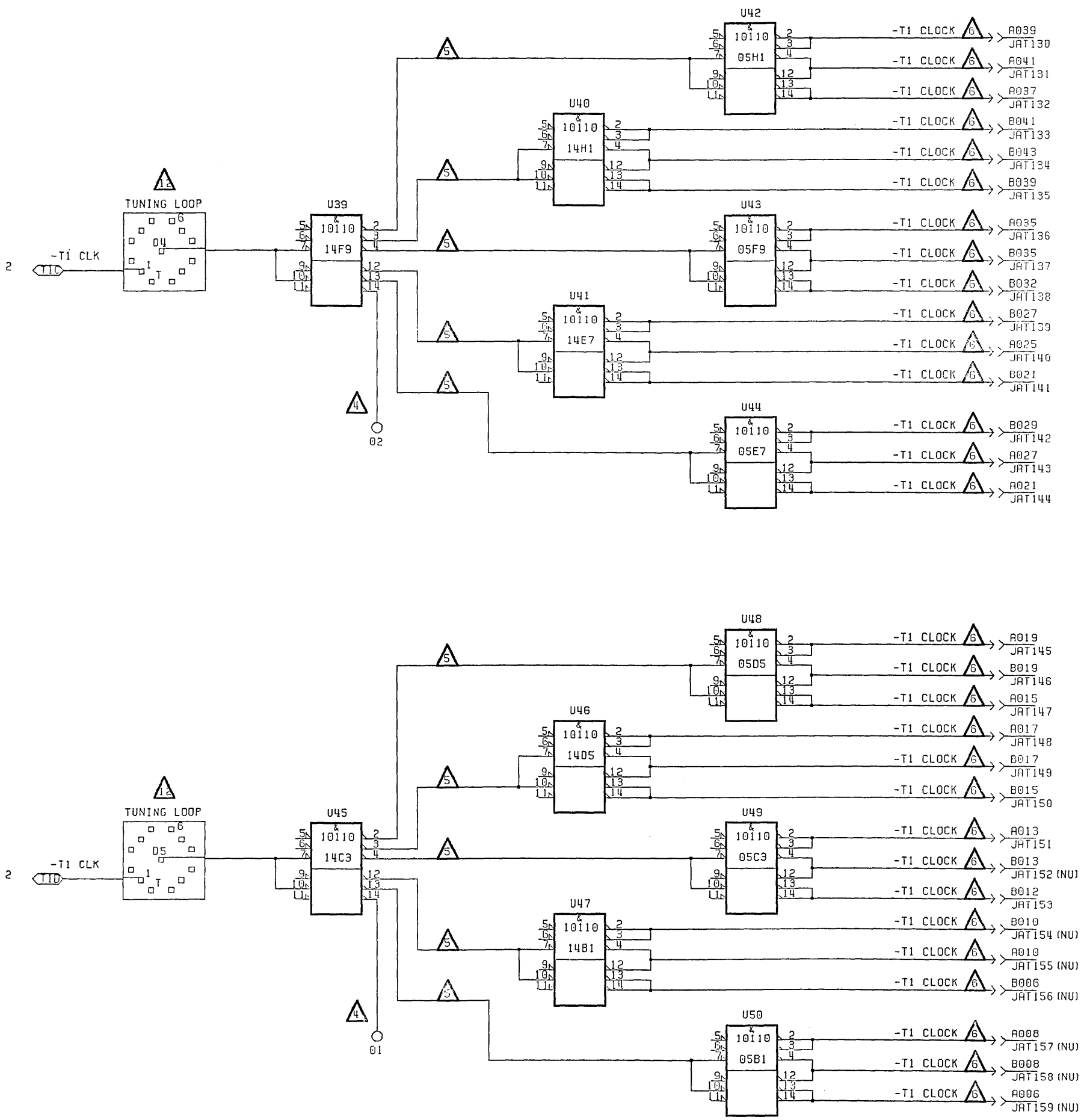
 CONTROL DATA	I4 CLOCK BOARD T2 CLOCK PULSE GENERATION AND T2 CLOCK FANOUT TYPE 1JAH	8	DWG NO.	DATE	REV
			53575500	11/01/85	A
			SHEET NO. 3		

T1 CLOCK FANOUT PART I



 CONTROL DATA	I4 CLOCK BOARD T1 CLOCK FANOUT PART I TYPE 1JAH	8	DWG NO.	DATE	REV
			53575500	11/01/85	A
			SHEET NO. 4		60462210

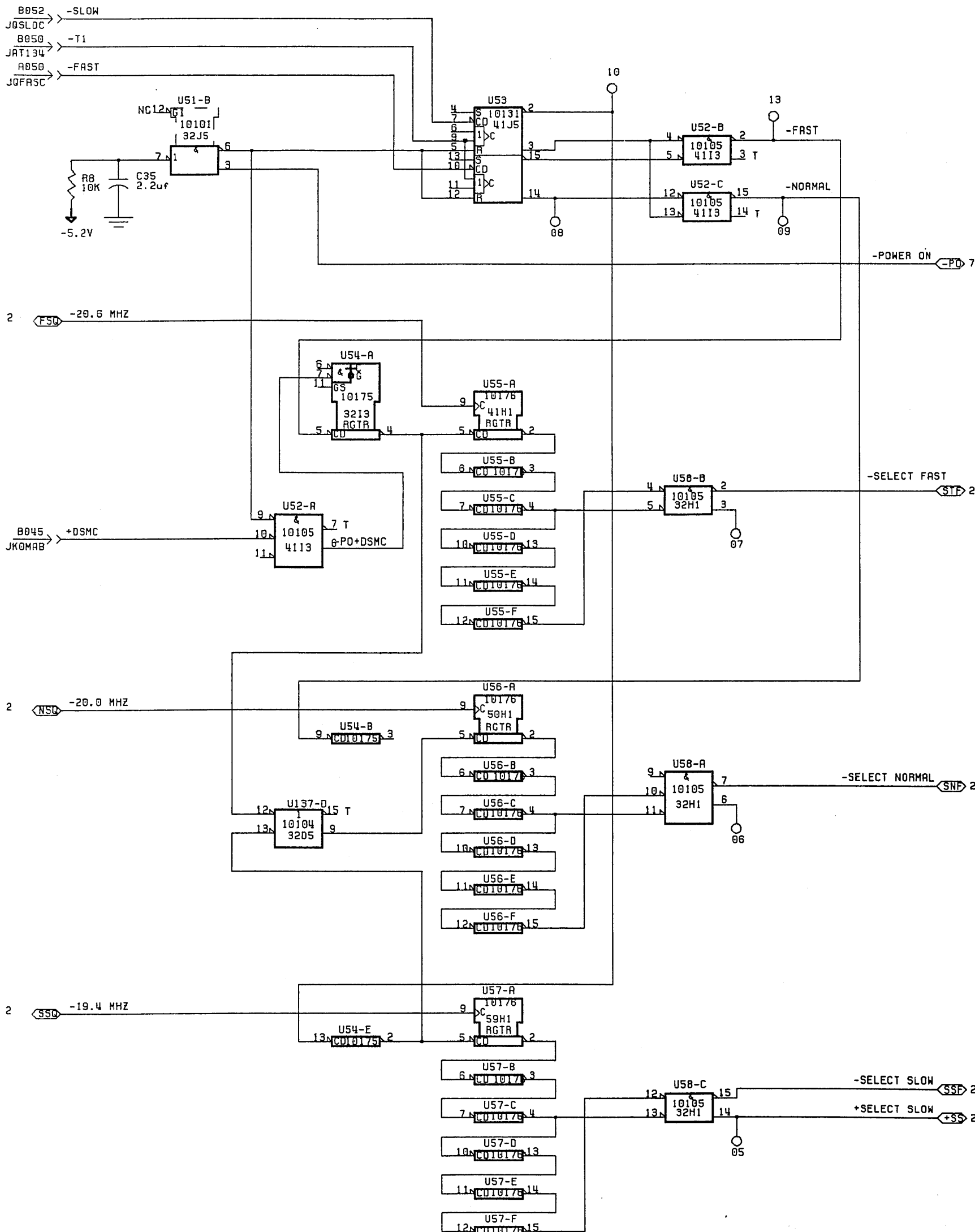
T1 CLOCK FANOUT PART II




- △4 - ALL LINES MARKED △4 SHALL BE EQUAL LENGTHS
- △5 - ALL LINES MARKED △5 SHALL BE EQUAL LENGTHS
- △6 - ALL LINES MARKED △6 SHALL BE EQUAL LENGTHS
- △2 - FIRST 10 TAPS 0.2 NS, LAST 2 TAPS 0.4 NS

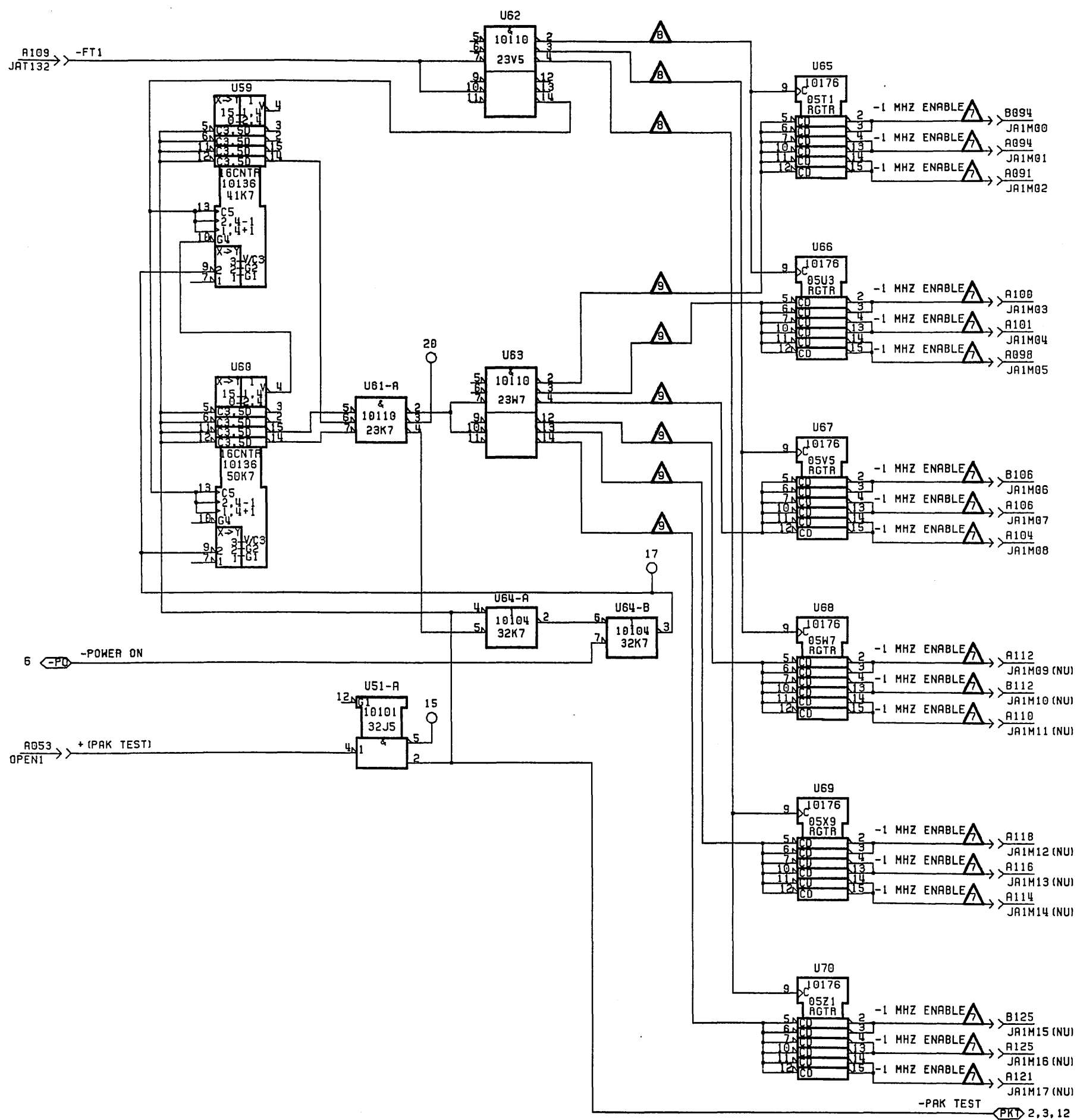
CONTROL DATA	I4 CLOCK BOARD T1 CLOCK FANOUT PART II TYPE IJAH	B	DWG NO. 53575500	DATE 11/01/85	REV A
			SHEET NO. 5	60462210	PAGE JA-05

CLOCK FREQUENCY SELECT



 CONTROL DATA	14 CLOCK BOARD CLOCK FREQUENCY SELECT	B	DWG NO. 53575500	DATE 12/15/86	REV C
	TYPE 1JAH	SHEET NO. 6	60462210	PAGE 1A-05	

1 MHZ CLOCK GENERATOR AND FANOUT



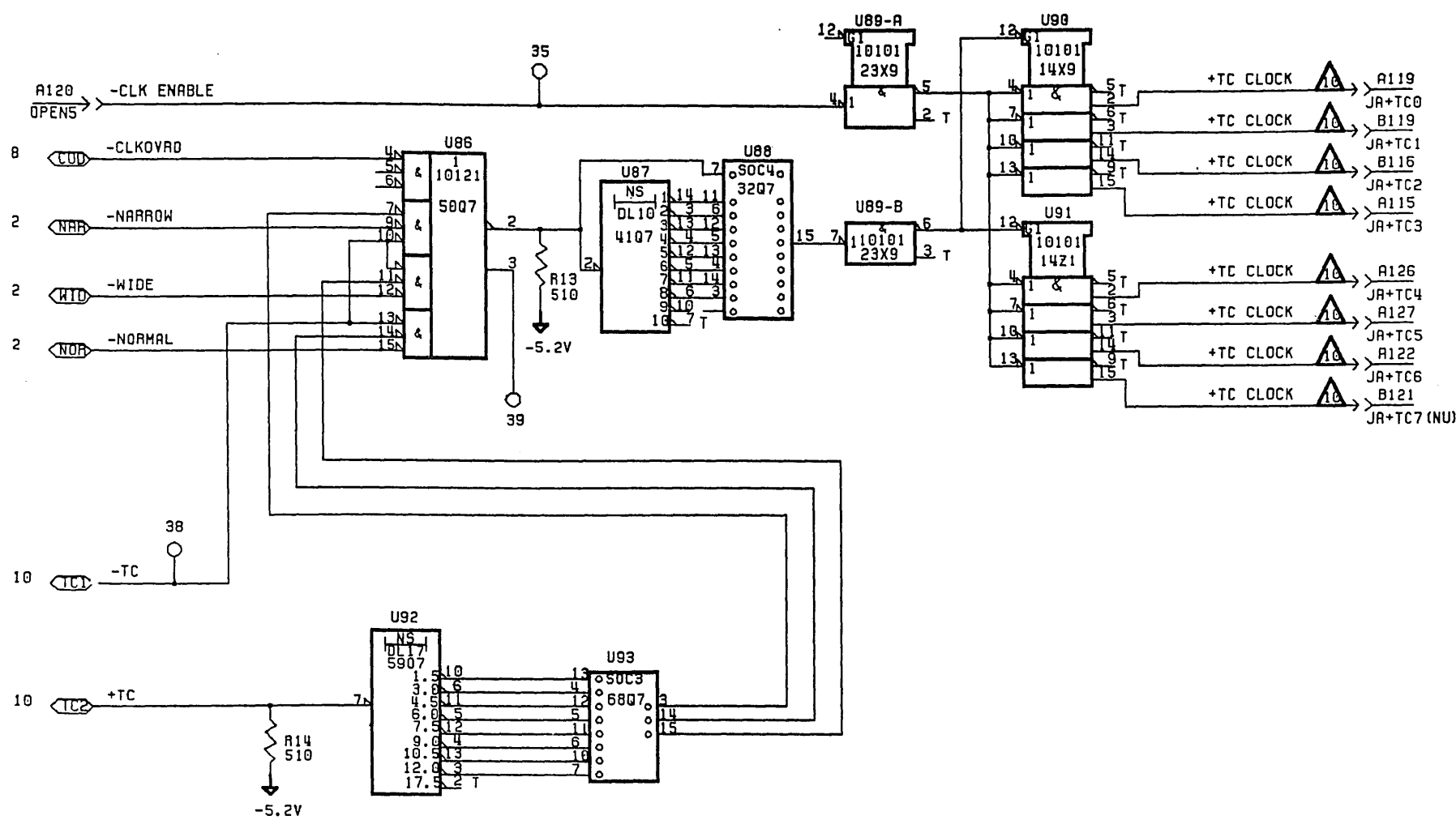
- ALL LINES MARKED SHALL BE EQUAL LENGTHS
- ALL LINES MARKED SHALL BE EQUAL LENGTHS
- ALL LINES MARKED SHALL BE EQUAL LENGTHS

 CONTROL DATA	I4 CLOCK BOARD		DWG NO.	DATE	REV
	1 MHZ CLOCK GENERATOR AND FANOUT		53575500	11/01/85	A
	TYPE 1JAH		SHEET NO. 7	60462210	PAGE JA-07

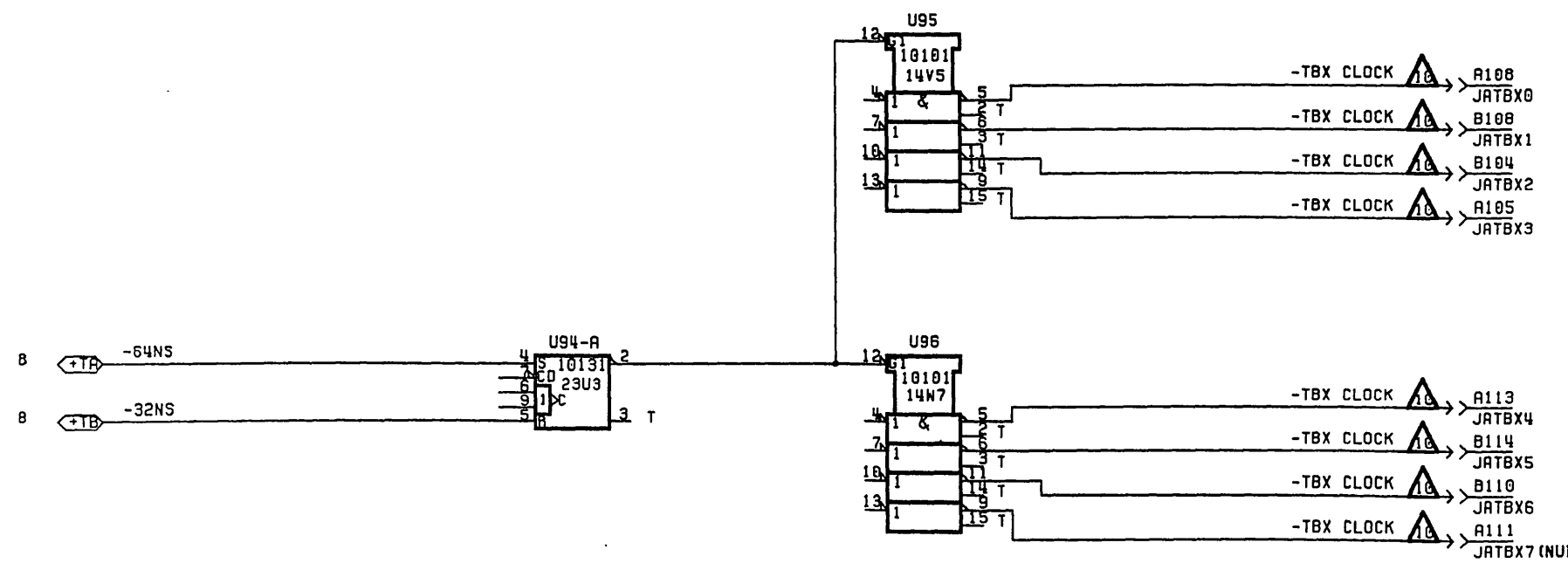
-TB CLOCK FANOUT



+TC CLOCK FANOUT



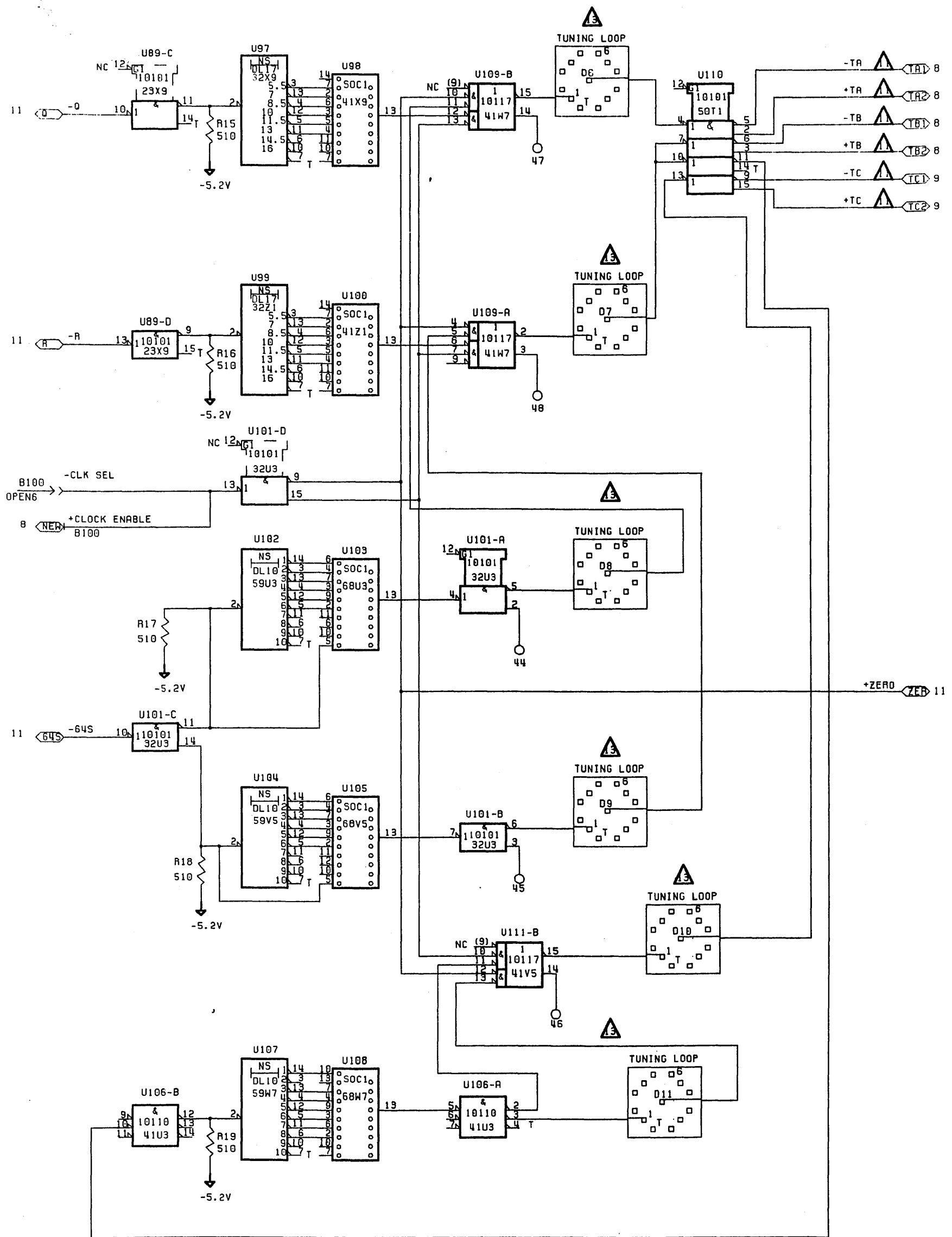
-TBX CLOCK FANOUT



ALL LINES MARKED SHALL BE EQUAL LENGTHS

CONTROL DATA	14 CLOCK BOARD +TC & -TBX CLOCK FANOUT TYPE 1JAH	8	DWG NO.	DATE	REV
			53575500	11/01/85	A
			SHEET NO. 9	60462210	PAGE JA-09

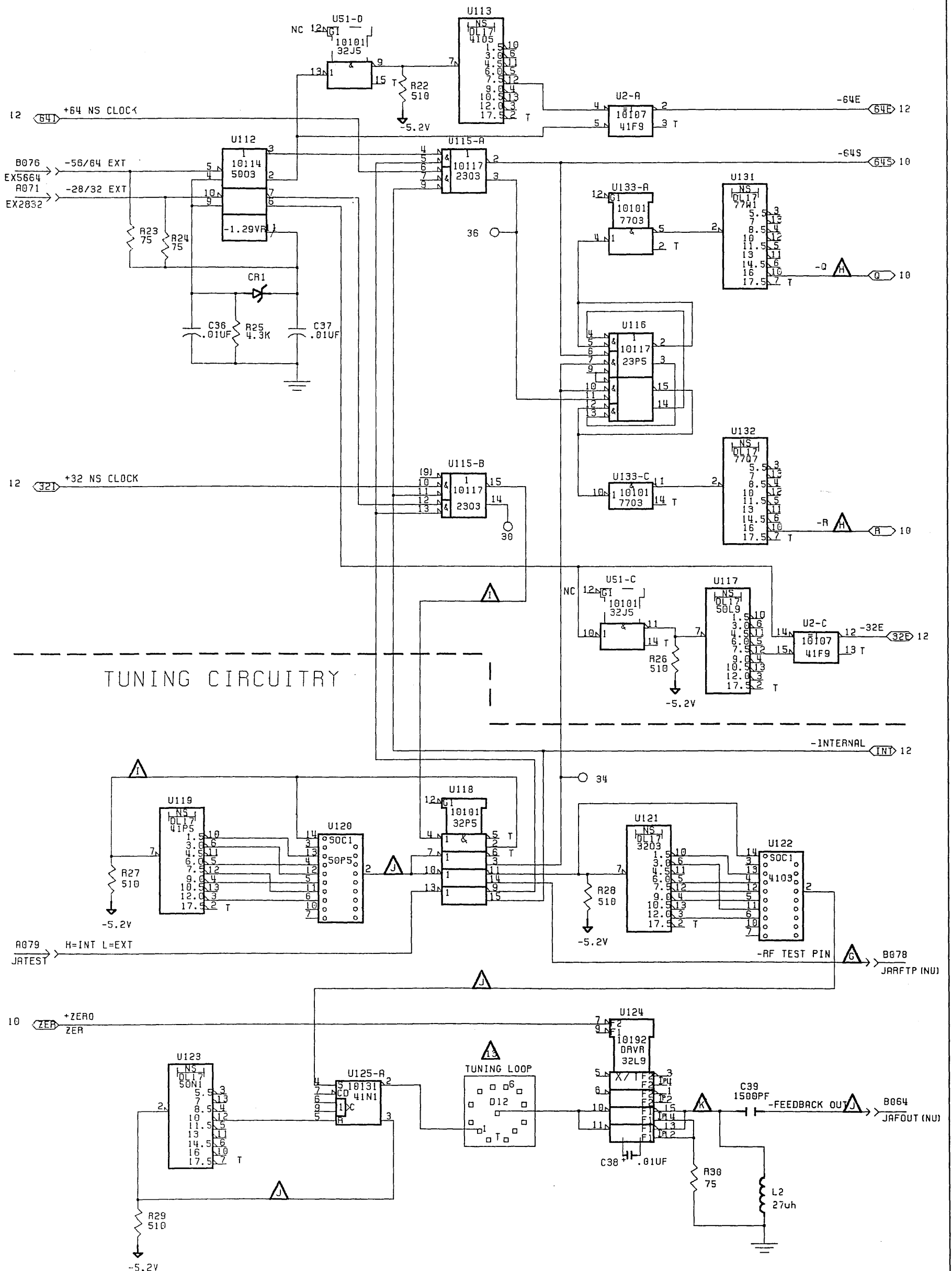
32/64 NS CLOCK SHAPING



13 ALL LINES MARKED 13 SHALL BE EQUAL LENGTHS
 13 EACH TAP 0.2 NS


	14 CLOCK BOARD 32/64 NS CLOCK SHAPING TYPE 1JAH	B	DWG NO. 53575500	DATE 06/03/86	REV B

32/64 OR 28/56 NS CLOCK RECEIVER

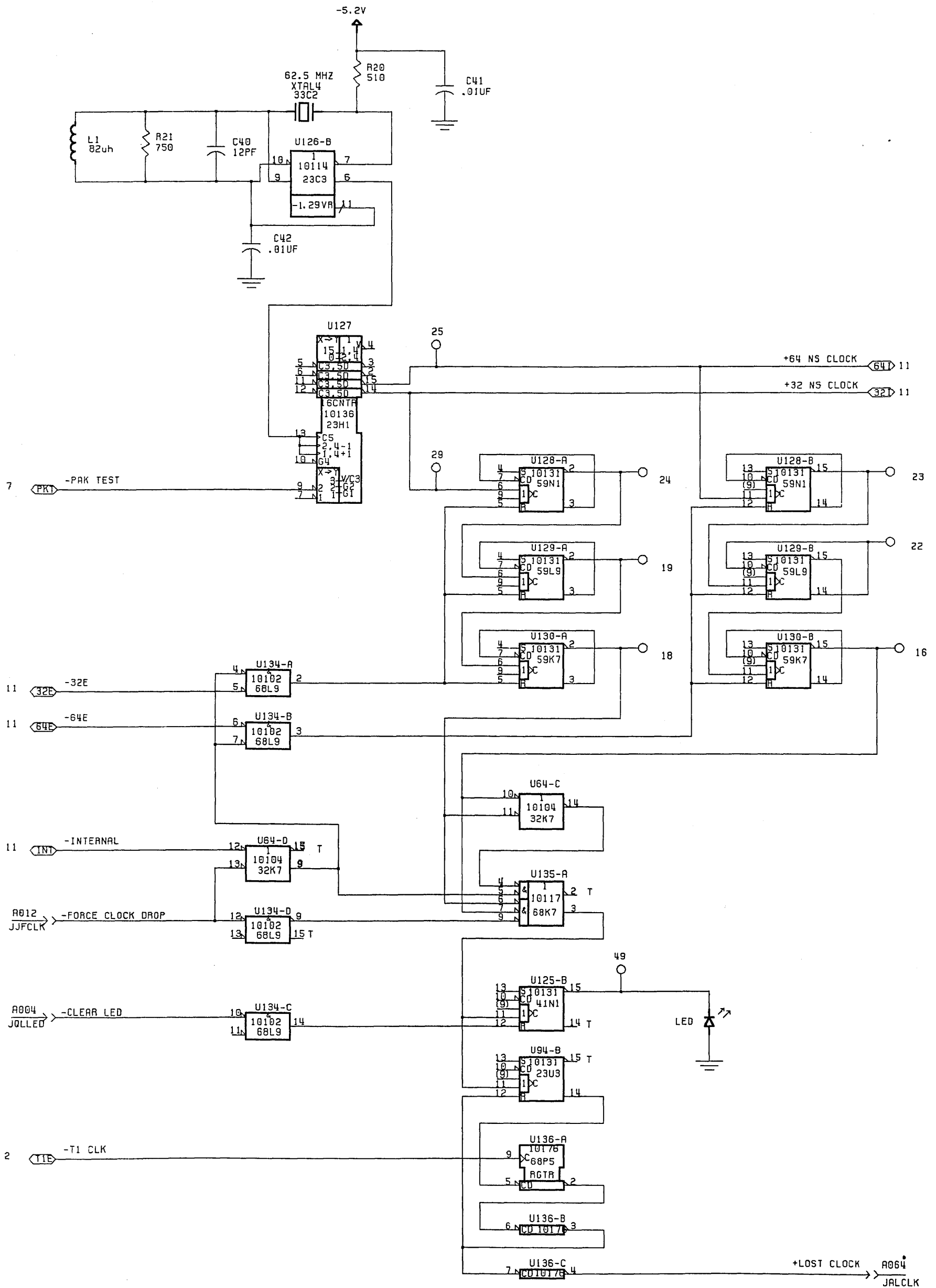



- DRIVE THIS PIN AS A TESTPOINT AT THE END OF THE LINE
 TERMINATE THE LINE AFTER THE PIN. LENGTH FROM 10101 OUTPUT
 TO CONNECTOR PIN SHALL BE 6 INCHES (1:1)
- LINE LENGTH SHALL BE 6 INCHES (1:1)
- LINE LENGTH SHALL BE 5 INCHES (1:1)

- LINE LENGTH SHALL BE 4 INCHES (1:1)
- LINE LENGTH SHALL BE 2 INCHES (1:1)
- EACH TAP 0.2 NS

 CONTROL DATA	I4 CLOCK BOARD 32/64 OR 28/56 NS CLOCK RCVR TUNING CIRCUITRY TYPE 1JAH	B	DWG NO.	DATE	REV
			53575500	12/15/86	C
			SHEET NO. 11		

CLOCK DROPOUT DETECT



 CONTROL DATA	I4 CLOCK BOARD CLOCK DROPOUT DETECT	B	DWG NO. 53575500	DATE 12/15/86	REV C	
	TYPE 1JAH					
			SHEET NO. 12	60462210	PAGE	JA-12

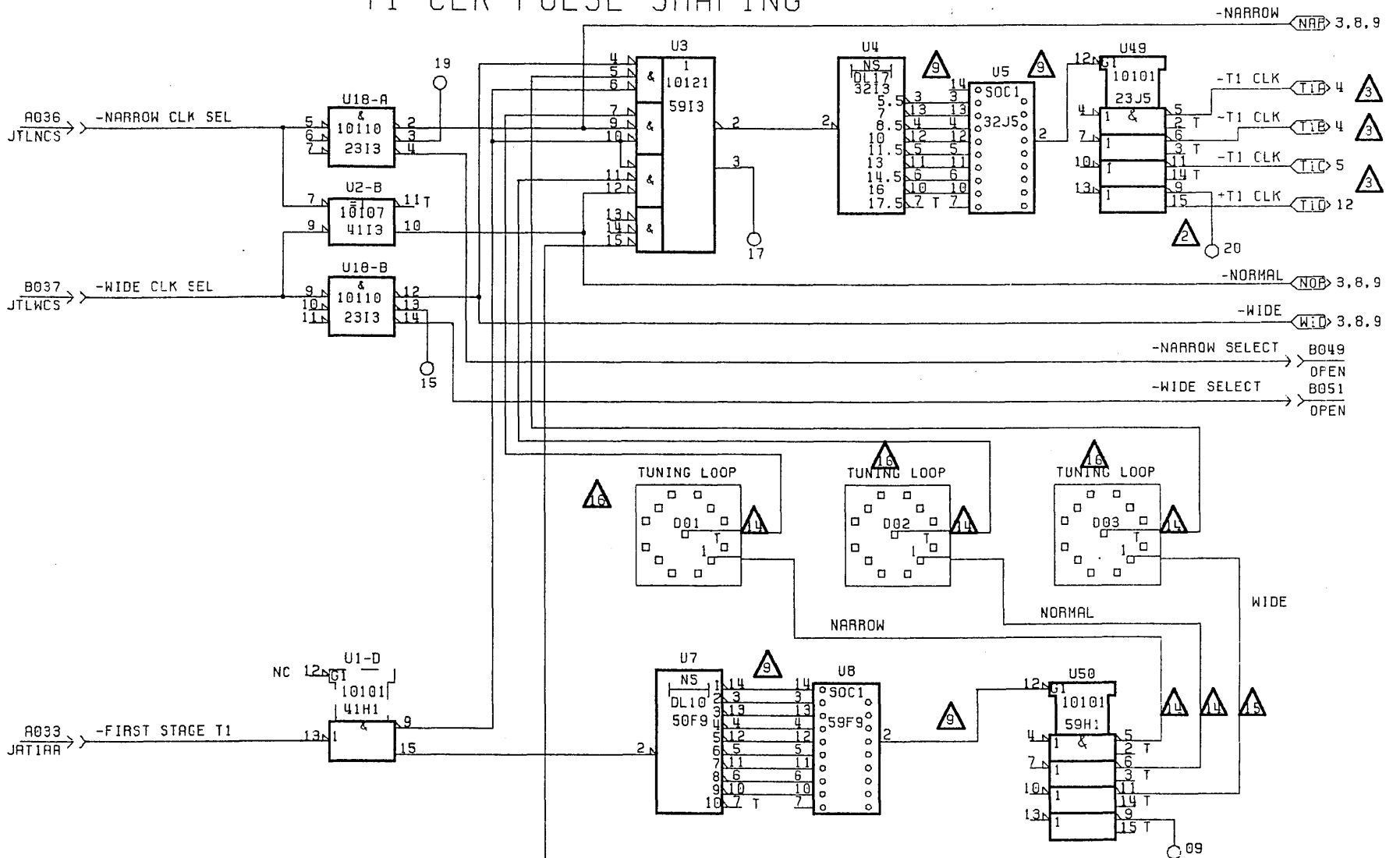
TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	05	-T1D CLOCK	27	02	-SELECT WIDE
02	05	-T1C CLOCK	28	02	-SELECT NARROW
03	08	-CLOCK OVER RIDE	29	12	+32NS CLOCK
04	02	+T1 CLOCK SHAPED	30	11	-32NS CLOCK
05	06	+SEL SLOW FREQ	31		
06	06	+SEL NORMAL FREQ	32	08	-CLOCK ENABLE TA
07	06	+SEL FAST FREQ	33	08	-CLOCK ENABLE TB
08	06	+FAST FREQ	34	11	-32NS TUNED CLOCK
09	06	-NORMAL FREQ	35	09	-CLOCK ENABLE
10	06	-SLOW FREQ	36	11	+64NS CLOCK
11	02	-T1D CLOCK	37	03	-T2 TUNED CLOCK
12	03	+T2 CLOCK	38	09	-TC CLOCK
13	06	-FAST FREQ	39	09	+TC CLOCK
14	04	-T1B CLOCK	40	08	-TB1 CLOCK
15	07	+PAK TEST	41	08	-TA1 CLOCK
16	12	+LOST CLK DET 64NS	42	08	+TB CLOCK SHAPED
17	07	-DSMC	43	08	+TA CLOCK SHAPED
18	12	+LOST CLK DET 32NS	44	10	+64S
19	12	+LOST CLK DET 32NS	45	10	-64S
20	07	-1 MHZ CLOCK	46	10	+TC CLOCK
21	03	-T2 SHAPED CLOCK	47	10	+TA CLOCK
22	12	-LOST CLK DET 64NS	48	10	+TB CLOCK
23	12	+LOST CLK DET 64NS	49	12	-LOST CLOCK
24	12	+LOST CLK DET 32NS			
25	12	+64NS CLOCK			
26	04	-T1A CLOCK			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 [NOT USED]
TERM	NONE
UNUSED	REFERENCE WIRE LIST

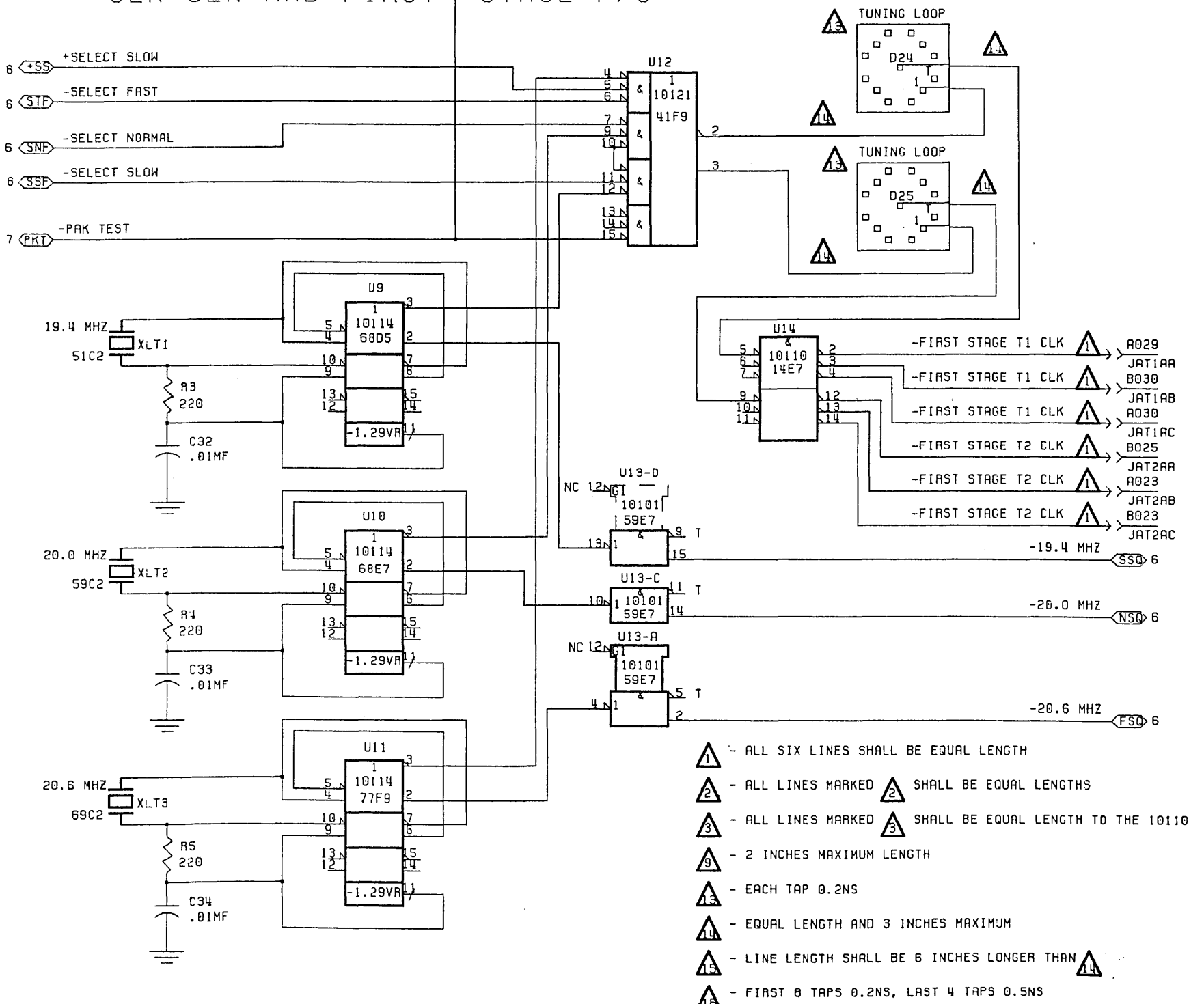
CAUTION


There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

T1 CLK PULSE SHAPING

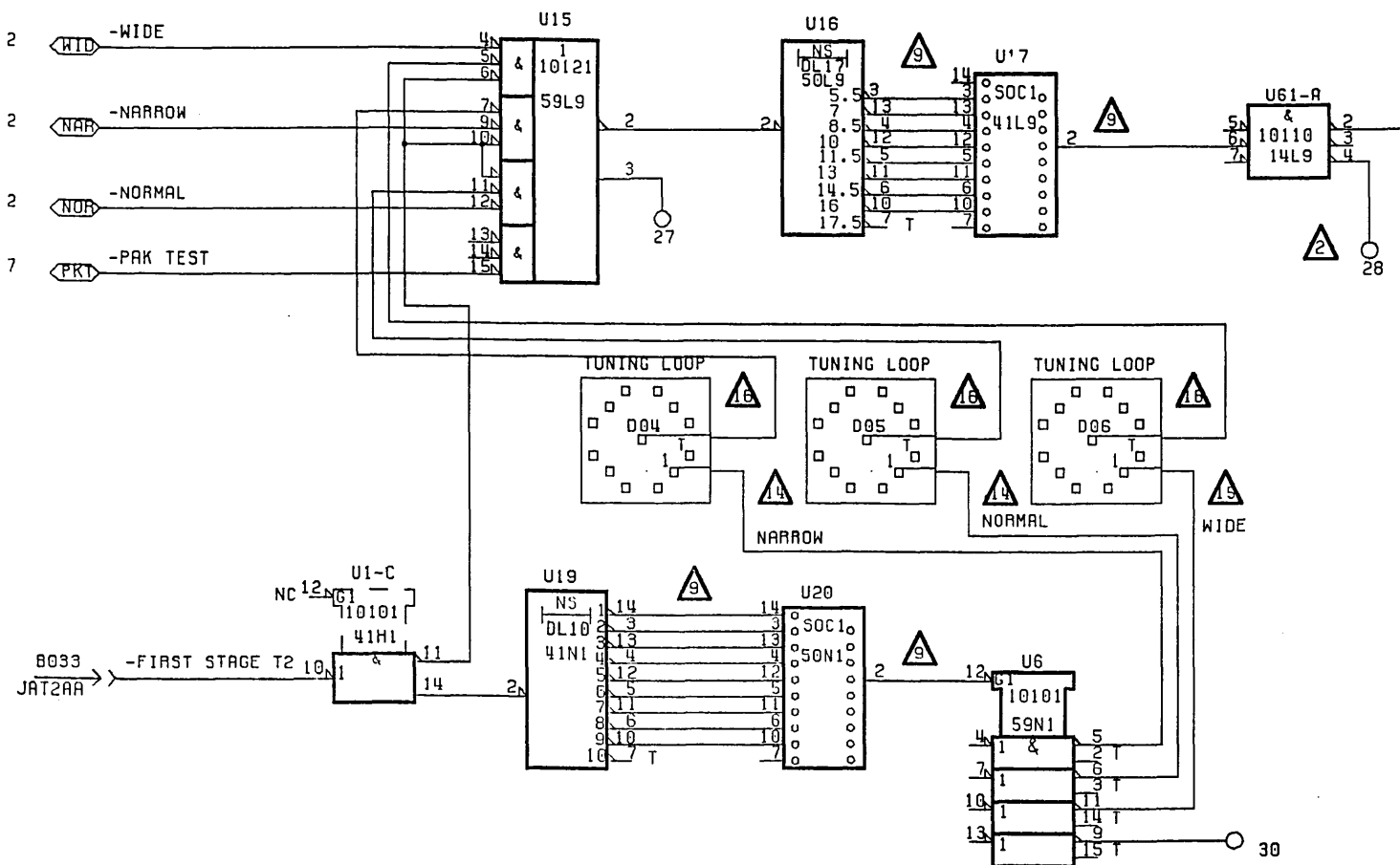


CLK	GEN	AND	FIRST	STAGE	F70
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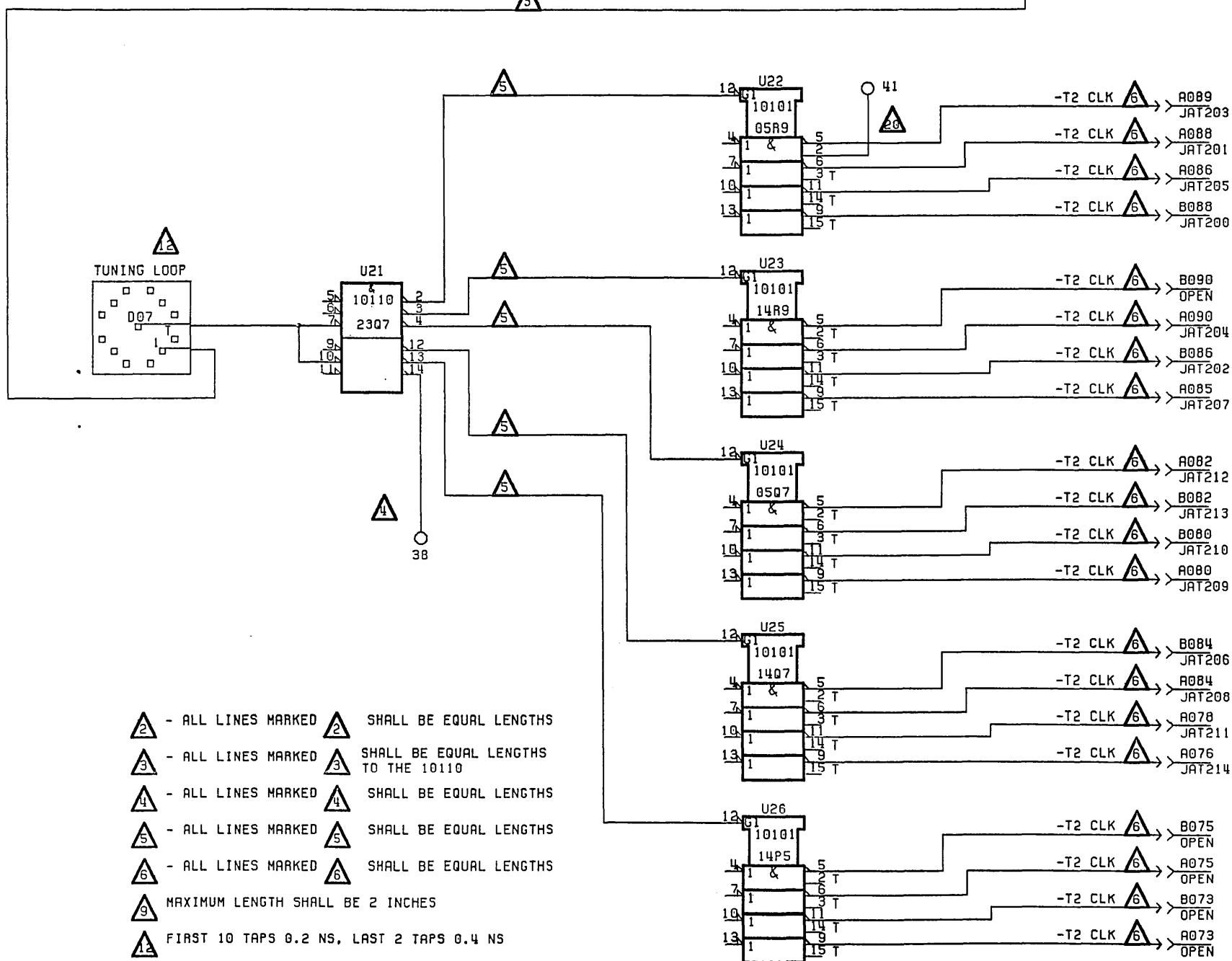


 CONTROL DATA	14 CLOCK BOARD T1 CLOCK PULSE SHAPING AND CLK GENERATION & FIRST STAGE F/D TYPE 1JAH	B	DWG NO. 22105670	DATE 12/15/86	REV C
	N	SHEET NO. 2	60462210	PAGE	JA-02

T2 CLK PULSE GEN

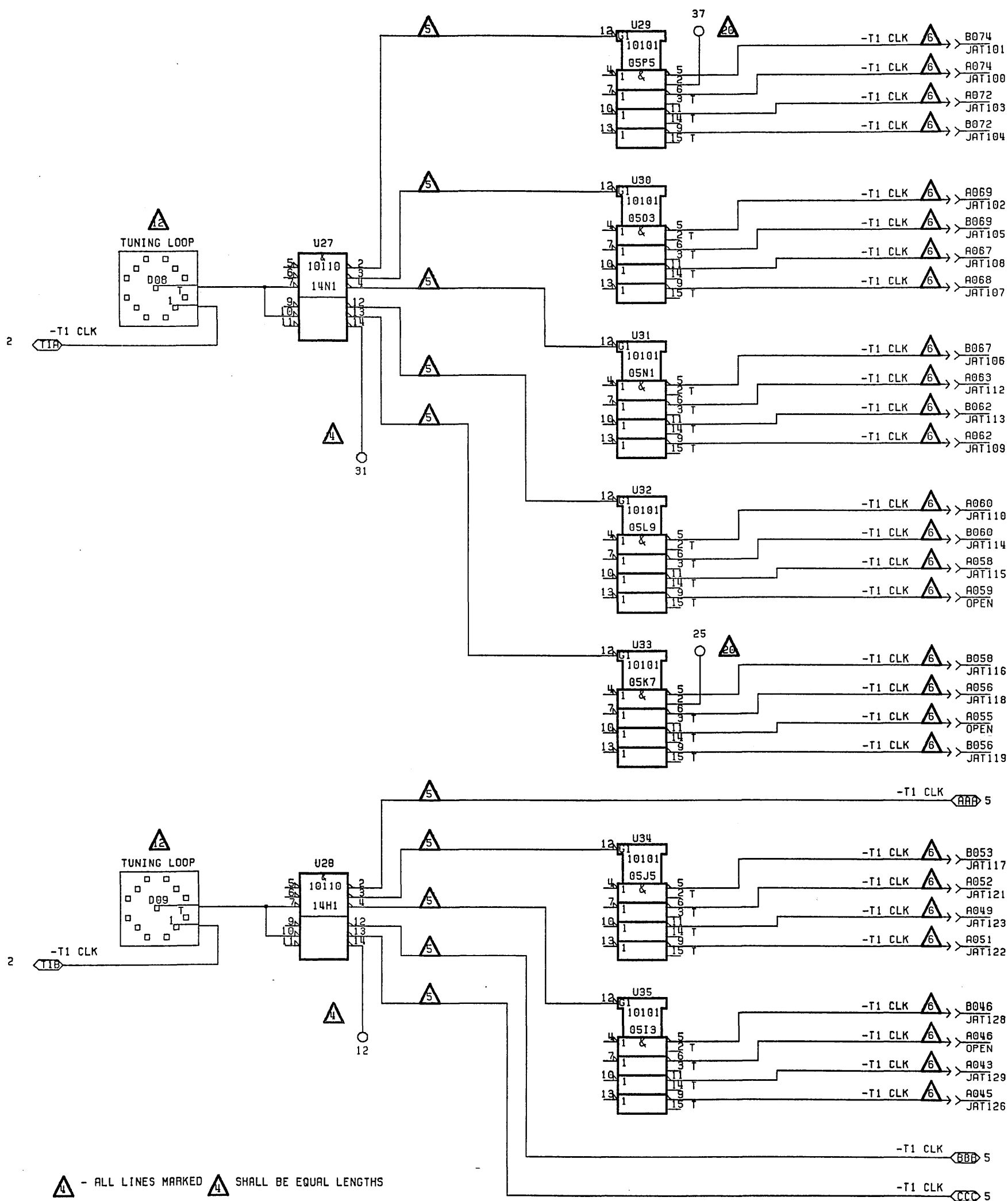


T2 CLK F/O



- 2 - ALL LINES MARKED 2 SHALL BE EQUAL LENGTHS
- 3 - ALL LINES MARKED 3 SHALL BE EQUAL LENGTHS TO THE 10110
- 4 - ALL LINES MARKED 4 SHALL BE EQUAL LENGTHS
- 5 - ALL LINES MARKED 5 SHALL BE EQUAL LENGTHS
- 6 - ALL LINES MARKED 6 SHALL BE EQUAL LENGTHS
- 9 MAXIMUM LENGTH SHALL BE 2 INCHES
- 12 FIRST 10 TAPS 0.2 NS, LAST 2 TAPS 0.4 NS
- 14 EQUAL LENGTH AND 3 INCHES MAXIMUM
- 15 - LINE LENGTH SHALL BE 6 INCHES LONGER THAN 14
- 16 FIRST 8 TAPS 0.2 NS, LAST 4 TAPS 0.5 NS
- 20 - ALL LINES MARKED 20 SHALL BE EQUAL LENGTHS

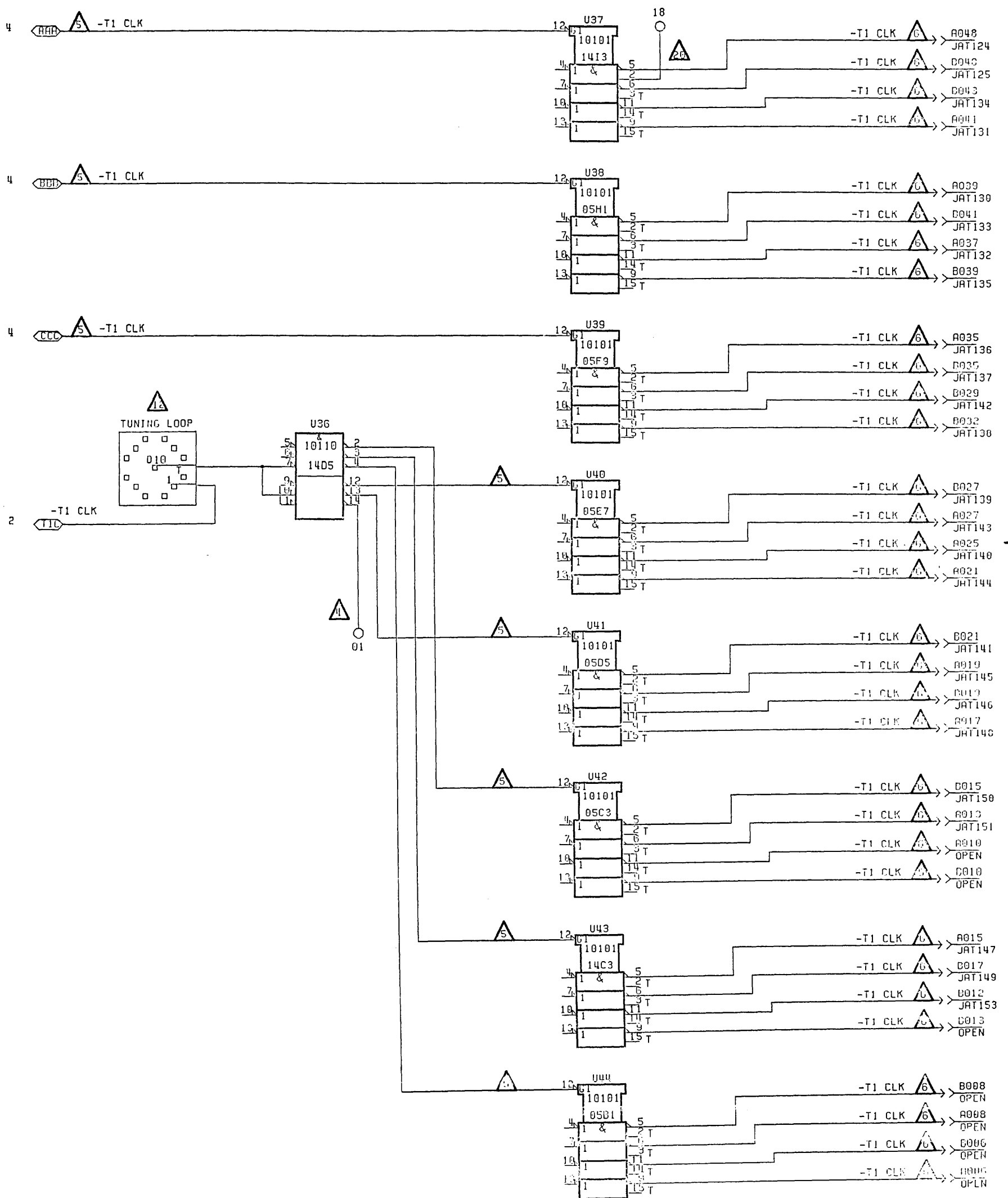
T1 CLK F/O PART I




- 4 - ALL LINES MARKED 4 SHALL BE EQUAL LENGTHS
- 5 - ALL LINES MARKED 5 SHALL BE EQUAL LENGTHS
- 6 - ALL LINES MARKED 6 SHALL BE EQUAL LENGTHS
- 42 - FIRST 10 TAPS 0.2 NS, LAST 2 TAPS 0.4 NS
- 20 - ALL LINES MARKED 20 SHALL BE EQUAL LENGTHS

 CONTROL DATA	14 CLOCK BOARD T1 CLOCK FANOUT PART I TYPE 1JAH		B	DWG NO. 22105670	DATE 12/13/85	REV A
				SHEET NO. 4	60462210	PAGE JA-04

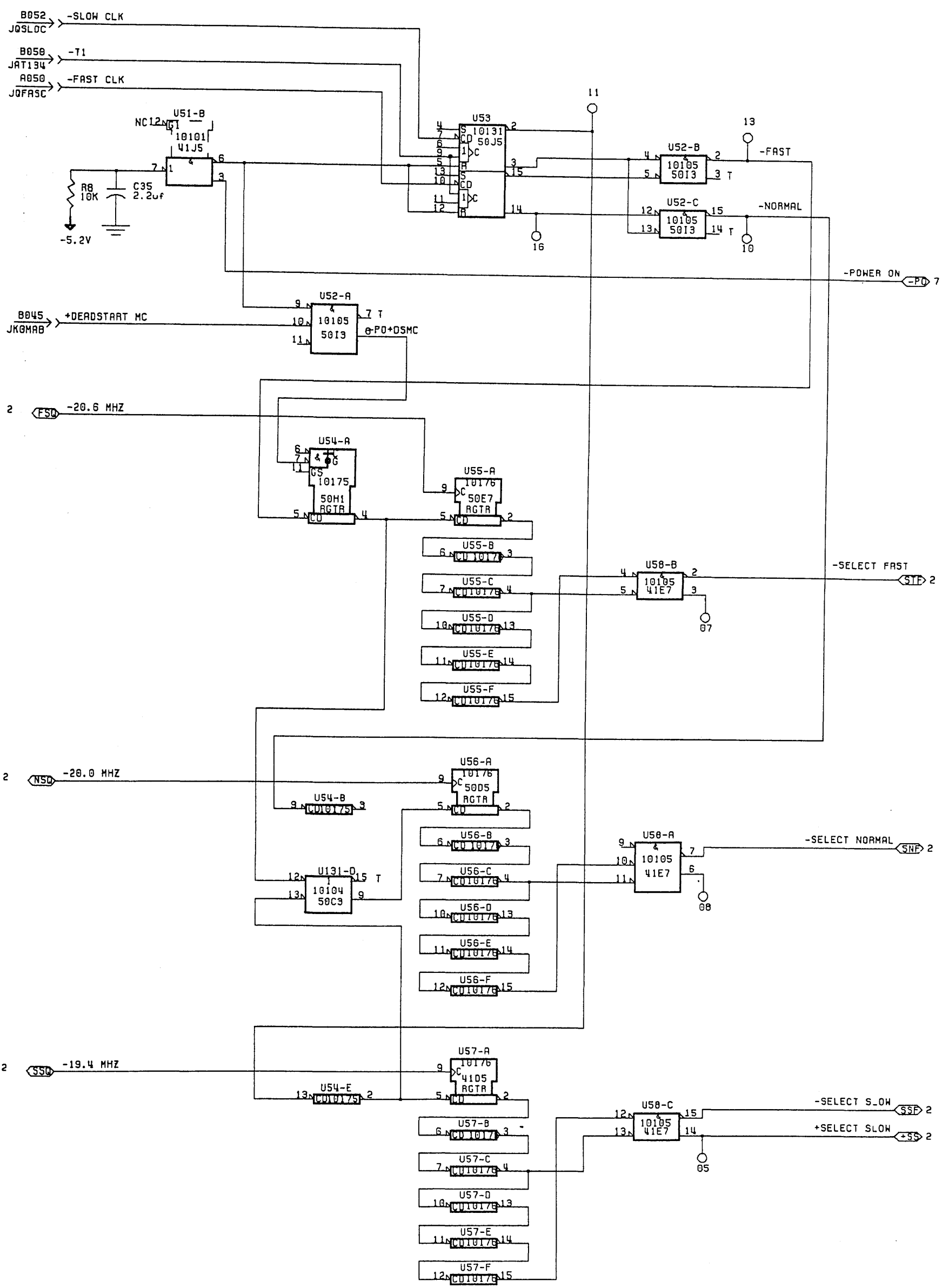
T11 CLK F/O PART II



- △ - ALL LINES MARKED △ SHALL BE EQUAL LENGTHS
- △ - ALL LINES MARKED △ SHALL BE EQUAL LENGTHS
- △ - ALL LINES MARKED △ SHALL BE EQUAL LENGTHS
- △ - FIRST 10 TAPS 0.2 NS, LAST 2 TAPS 0.4 NS
- △ - ALL LINES MARKED △ SHALL BE EQUAL LENGTHS

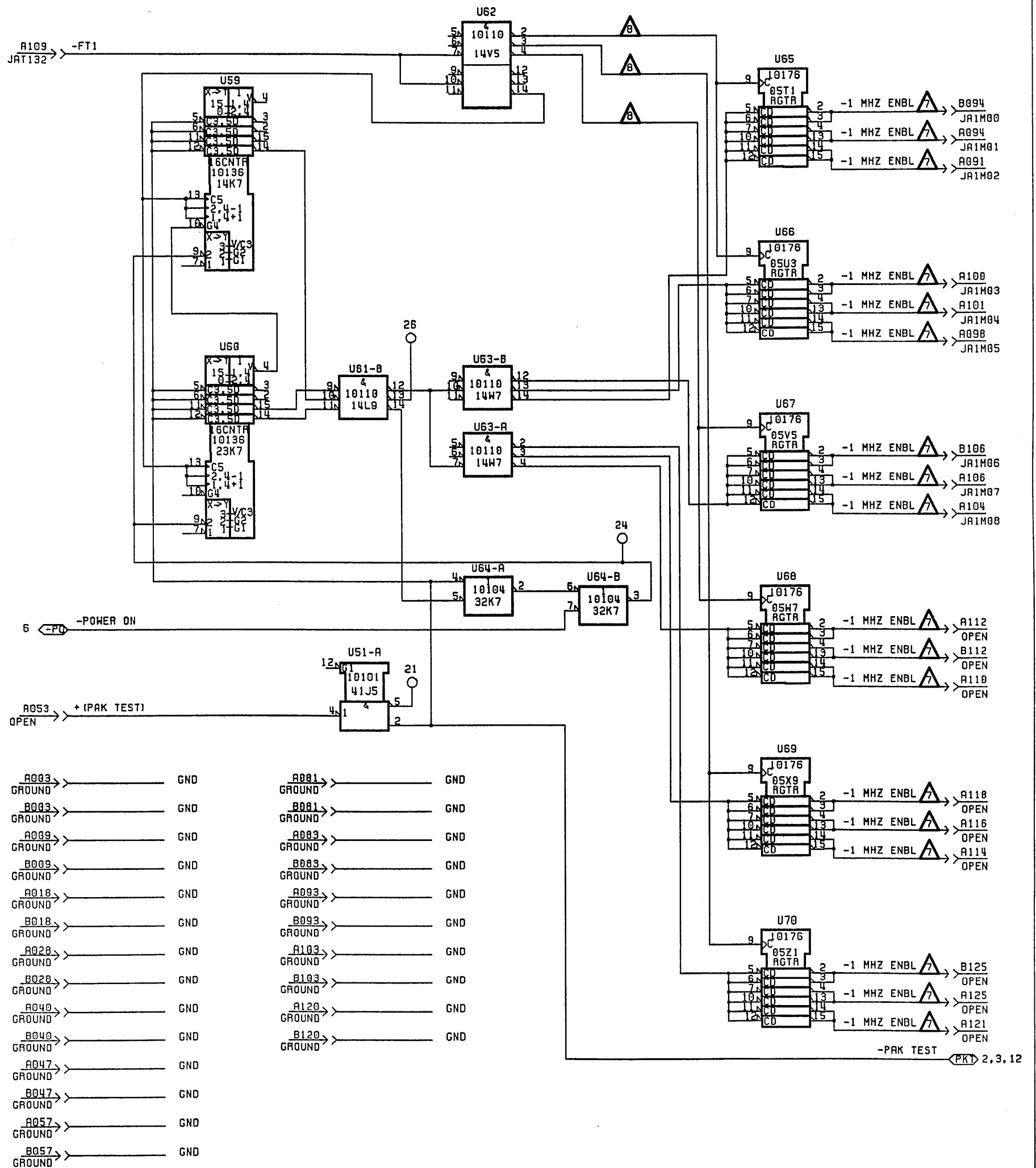
 CONTROL DATA	14 CLOCK BOARD T1 CLOCK FANOUT PART II TYPE 1JAH	8	DWG NO.	DATE	REV
			22105670	12/13/85	A
			SHEET NO. 5		60462210

CLK FREQUENCY SEL




CD CONTROL DATA	14 CLOCK BOARD CLOCK FREQUENCY SELECT		B	DWG NO. 22105670	DATE 12/15/86	REV C
	TYPE 1JAH		N	SHEET NO. 6	60462210	PAGE JA-06

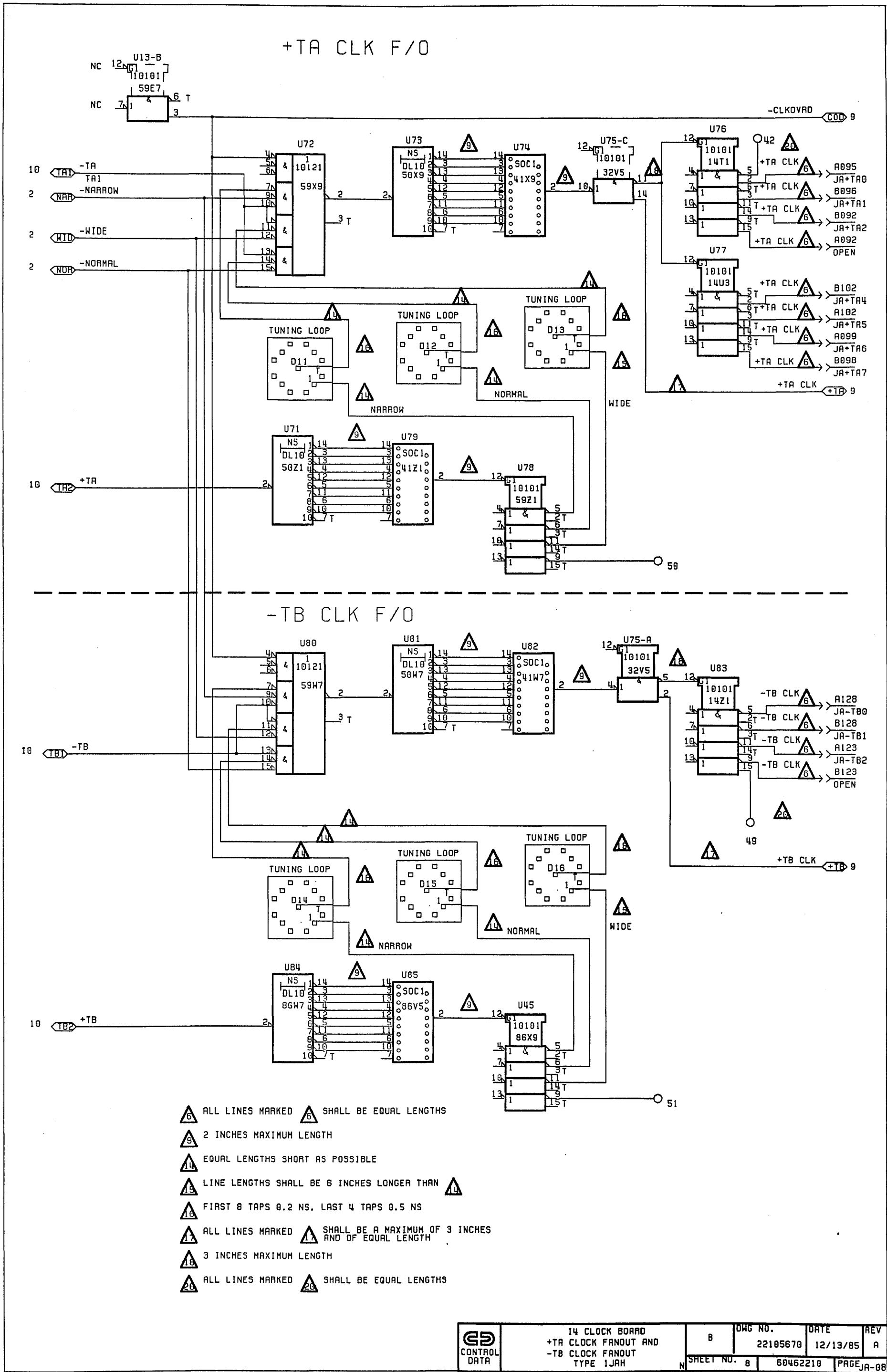
1 MHZ CLK GEN AND F/O



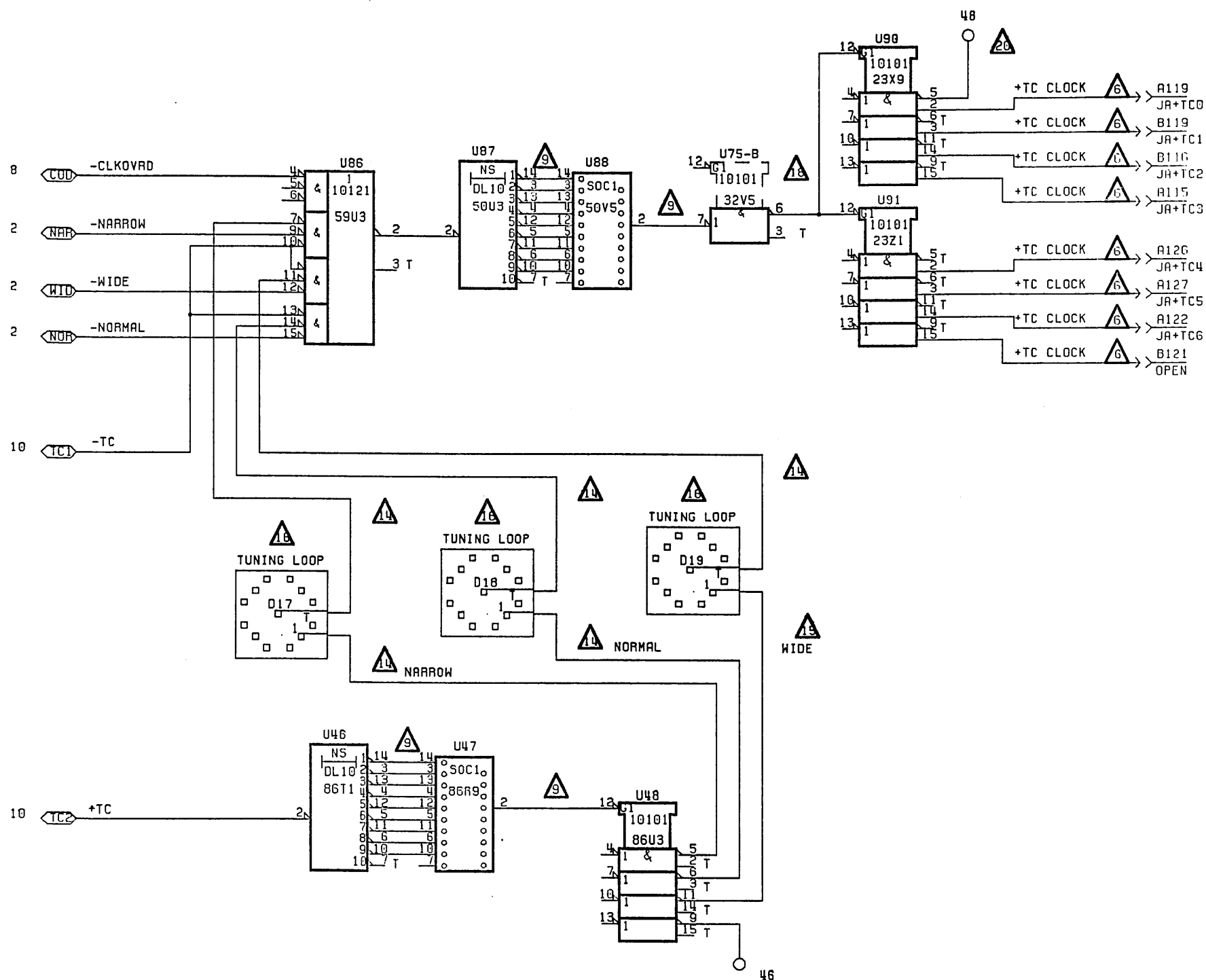
\triangle ALL LINES MARKED \triangle SHALL BE EQUAL LENGTHS

\triangle ALL LINES MARKED \triangle SHALL BE EQUAL LENGTHS AND A MAXIMUM OF 2 INCHES BETWEEN 10176 CHIPS

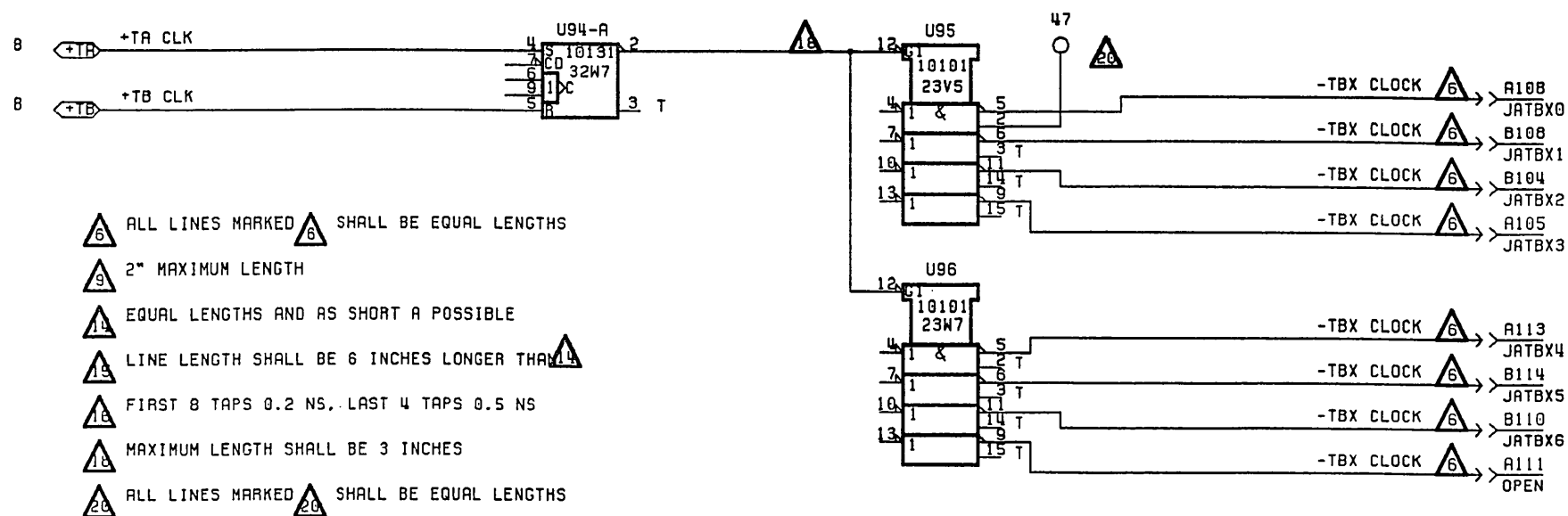
 CONTROL DATA	14 CLOCK BOARD 1 MHZ CLOCK GENERATOR AND FANOUT TYPE 1JAH	8	DWG NO.	DATE	REV
			22105670	12/13/85	A
			SHEET NO. 7		60462210



+TC CLK F/O



-TBX CLK F/O

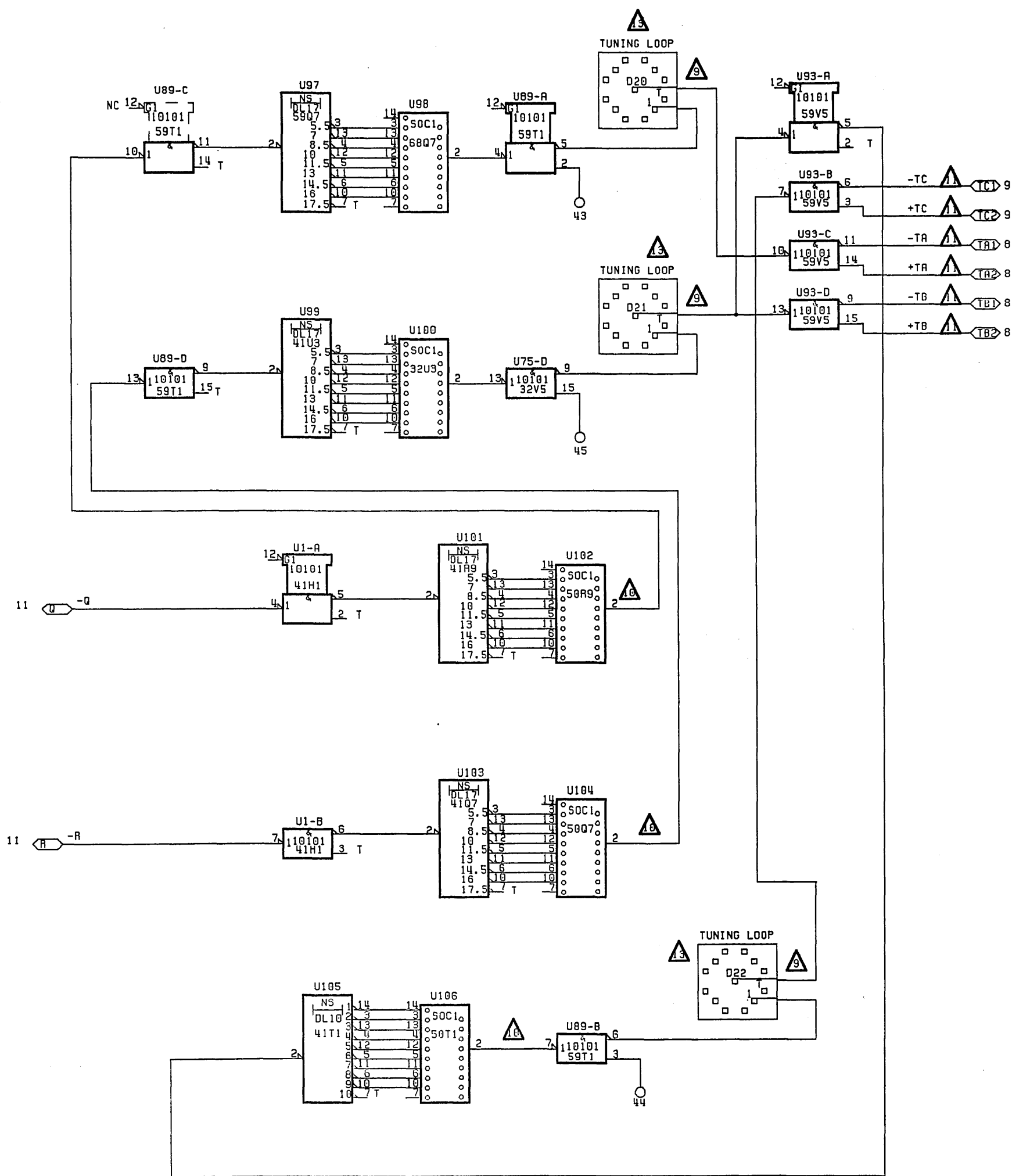


- ALL LINES MARKED SHALL BE EQUAL LENGTHS
- 2" MAXIMUM LENGTH
- EQUAL LENGTHS AND AS SHORT A POSSIBLE
- LINE LENGTH SHALL BE 6 INCHES LONGER THAN
- FIRST 8 TAPS 0.2 NS, LAST 4 TAPS 0.5 NS
- MAXIMUM LENGTH SHALL BE 3 INCHES
- ALL LINES MARKED SHALL BE EQUAL LENGTHS

	14 CLOCK BOARD +TC & -TBX CLOCK FANOUT TYPE 1JAH	B	DWG NO. 22105670	DATE 12/13/85	REV A

SHEET NO. 9 60462210 PAGE JA-09

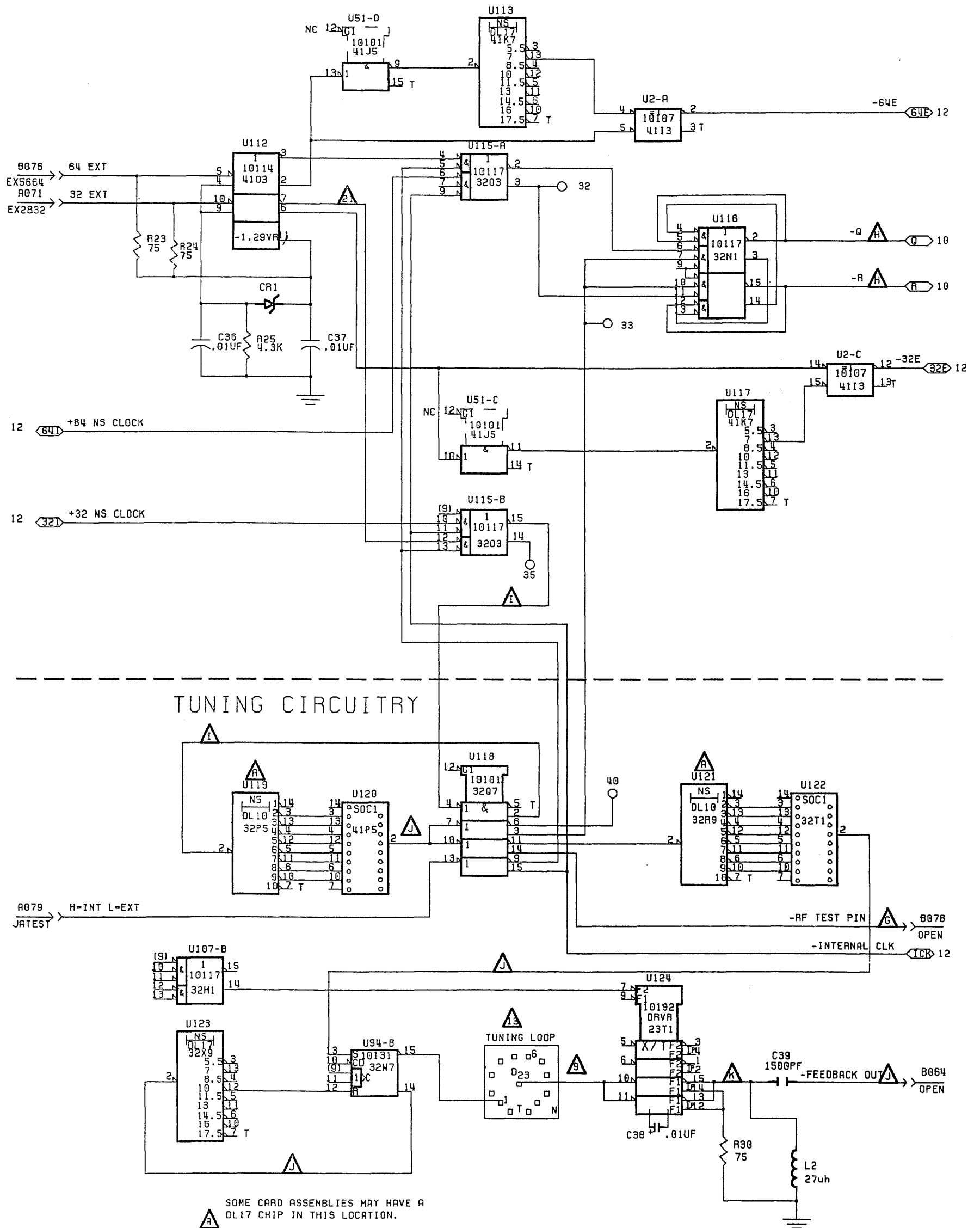
32/64 NS CLK SHAPING




- △ 9 2 INCHS MAXIMUM LENGTH
- △ 10 SHALL BE EQUAL LENGTH NOT TO EXCEED 2 INCHES
- △ 11 ALL LINES MARKED △ 11 SHALL BE EQUAL LENGTHS
- △ 13 EACH TAP 0.2 NS

CONTROL DATA	I4 CLOCK BOARD 32/64 NS CLOCK SHAPING TYPE 1JAH	B	DWG NO. 22105670	DATE 12/13/85	REV A
			SHEET NO. 10	60462210	PAGE JA-10

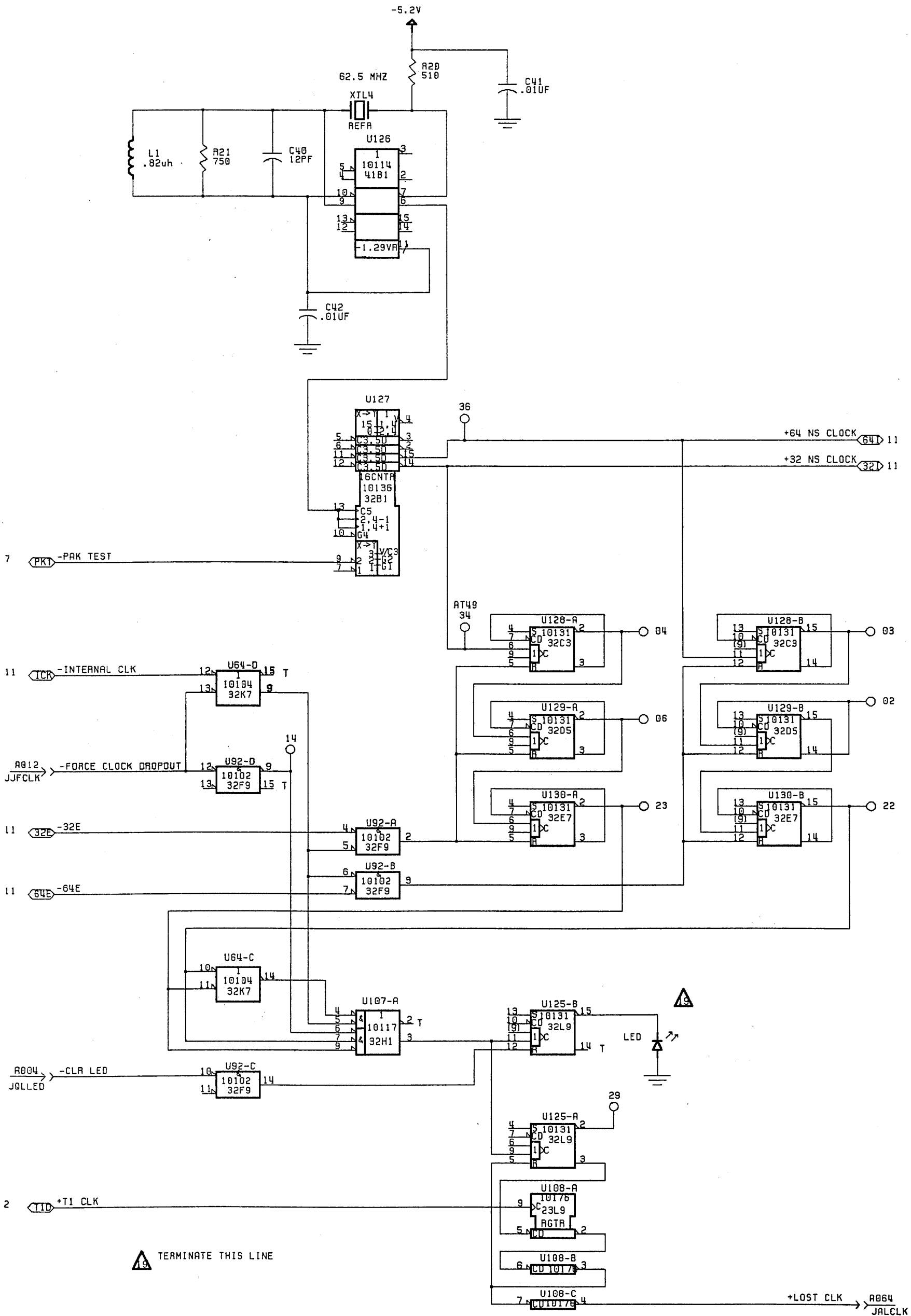
56 OR 64 NS CLK RECEIVER




- SOME CARD ASSEMBLIES MAY HAVE A DL17 CHIP IN THIS LOCATION.
- DRIVE THIS PIN AS A TESTPOINT AT THE END OF THE LINE
TERMINATE THE LINE AFTER THE PIN. LENGTH FROM 10101 OUTPUT
TO CONNECTOR PIN SHALL BE 6 INCHES (1:1)
- LINE LENGTH SHALL BE 6 INCHES (1:1)
- LINE LENGTH SHALL BE 5 INCHES (1:1)
- LINE LENGTH SHALL BE 4 INCHES (1:1)
- LINE LENGTH SHALL BE 2 INCHES (1:1)
- 2 INCHES MAXIMUM LENGTH
- EACH TAP 0.2 NS
- LINE LENGTH SHALL BE 3 INCHES

 CONTROL DATA	14 CLOCK BOARD 32/64 OR 28/56 NS CLOCK ACVR TUNING CIRCUITRY TYPE 1JAH	B	DWG NO.	DATE	REV
			22105670	12/15/88	C
			SHEET NO. 11		60462210

CLK DROPOUT DETECT



 CONTROL DATA	14 CLOCK BOARD CLOCK DROPOUT DETECT		B	DWG NO. 22105670	DATE 12/15/86	REV C
	TYPE 1JAH			SHEET NO. 12	60462210	PAGE JA-12

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	05	-T1 CLOCK	27	03	+T2 CLOCK SHAPED
02	12	+LOST CLK DET 64NS	28	03	-T2 CLOCK
03	12	-LOST CLK DET 64NS	29	12	-LOST CLOCK
04	12	-LOST CLK DET 32NS	30	03	+FRST STAGE T2 DLYD
05	06	+SEL SLOW FREQ	31	04	-T1 CLOCK
06	12	-LOST CLK DET 32NS	32	11	-64NS SQUARE WAVE
07	06	+SEL FAST FREQ	33	11	-32NS SQUARE WAVE
08	06	+SEL NORMAL FREQ	34	12	+32NS CLOCK
09	02	+FRST STAGE T1 DLYD	35	11	+32NS SQUARE WAVE
10	06	-NORMAL FREQ	36	12	+64NS CLOCK
11	06	-SLOW FREQ	37	04	+T1 CLOCK (OUTPUT)
12	04	-T1 CLOCK	38	03	-T2 TUNED CLOCK
13	06	-FAST FREQ	39		
14	12	-FORCE CLK DROPOUT	40	11	+32NS SQUARE WAVE
15	02	-SELECT WIDE	41	03	+T2 CLOCK (OUTPUT)
16	06	+FAST FREQ	42	08	-TA CLOCK (OUTPUT)
17	02	+T1 CLOCK SHAPED	43	10	-FIRST STAGE TA
18	05	+T1 CLOCK (OUTPUT)	44	10	-FIRST STAGE TC
19	02	-SELECT NARROW	45	10	-FIRST STAGE TB
20	02	-T1 CLOCK	46	09	+TC CLOCK DELAYED
21	07	+PAK TEST ENABLE	47	09	+TBX CLOCK (OUTPUT)
22	12	-LOST CLK DET 64NS	48	09	-TC CLOCK (OUTPUT)
23	12	-LOST CLK DET 32NS	49	08	+TB CLOCK (OUTPUT)
24	07	-1 MHZ COUNTER RESET	50	08	-TA CLOCK DELAYED
25	04	+T1 CLOCK (OUTPUT)	51	08	+TB CLOCK DELAYED
26	07	-1 MHZ ENABLE			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [NOT USED]
TERM	NONE
UNUSED	B004,A005,B005,A011,B011,A016,B016,A020,B020,A022,B022,A026,B026,A031,B031,A032,B036,A038,B038,A042,B042,B055,B059,B063,B068,B071,B079,B085,B089,B091,B095,A096,B099,B100,B101,B105,B109,B111,B113,B115,B118,B122,B126,B127

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

1 JCH / 1 JUH

R + A BOARD


REVISION HISTORY B/M 41650501

[illegible]

NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

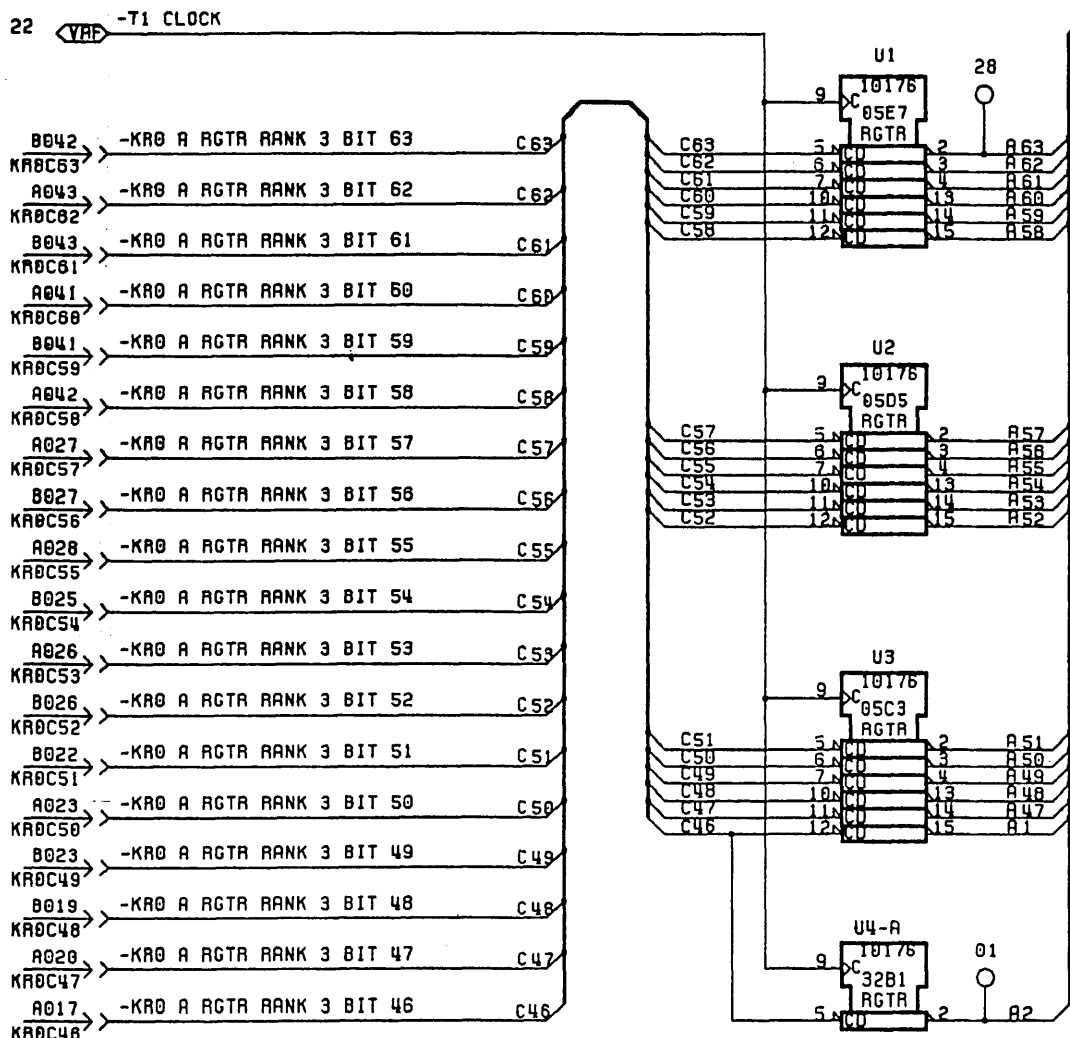
LOC: A11, A10, A09

DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	D R FORD	12/04/85
PUBS	R K BONDE	12/05/85
APP	D R FORD	12/04/85

 CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575502	DATE 08/21/87	REV D
	TYPE 1JCH/1JUH	SHEET NO. 1	60462210	PAGE	JC-01

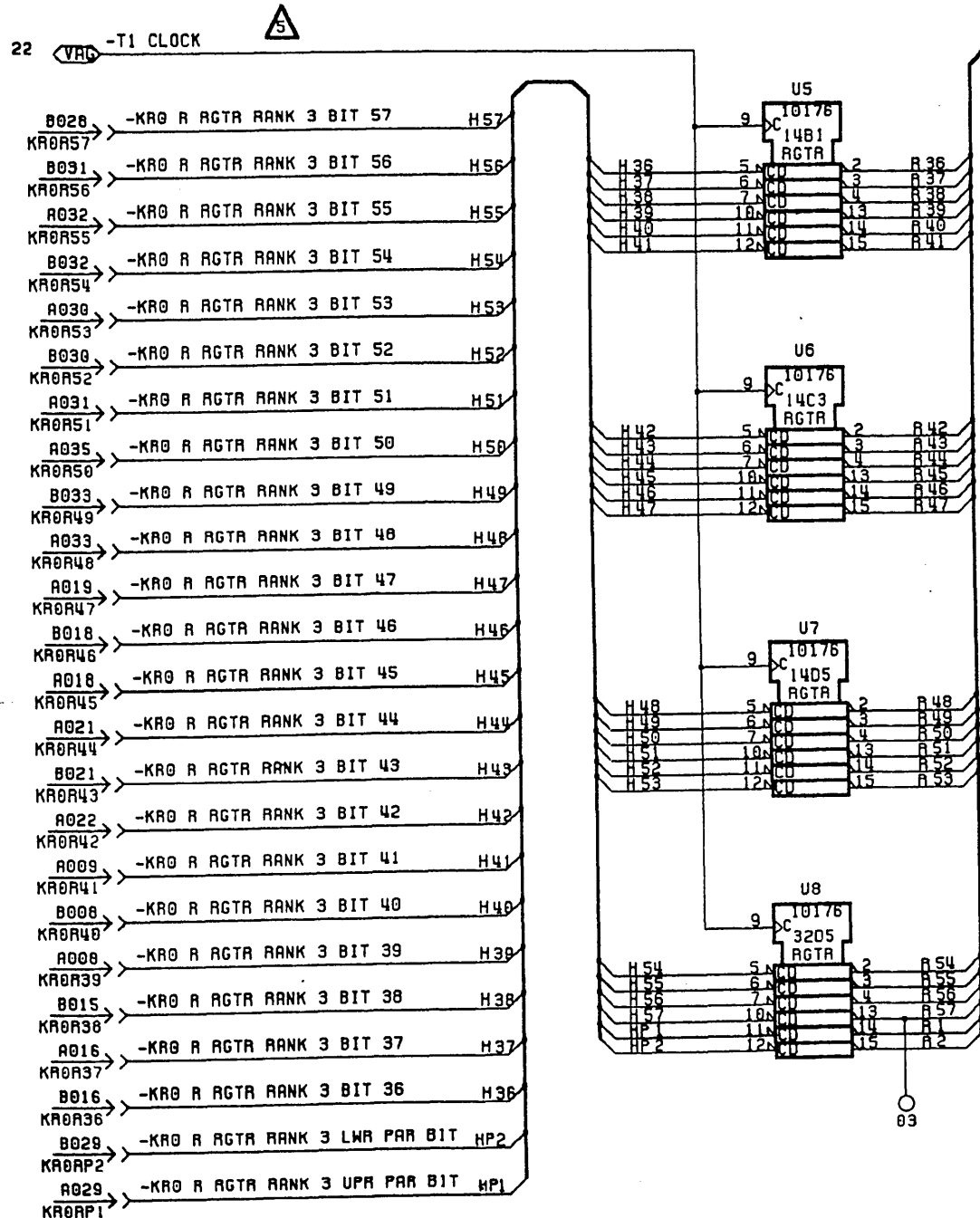
BAS 0 A RGTR RANK 4

-BAS 0 A RGTR DATA RANK 4 3,8,9



BAS 0 R RGTR RANK 4

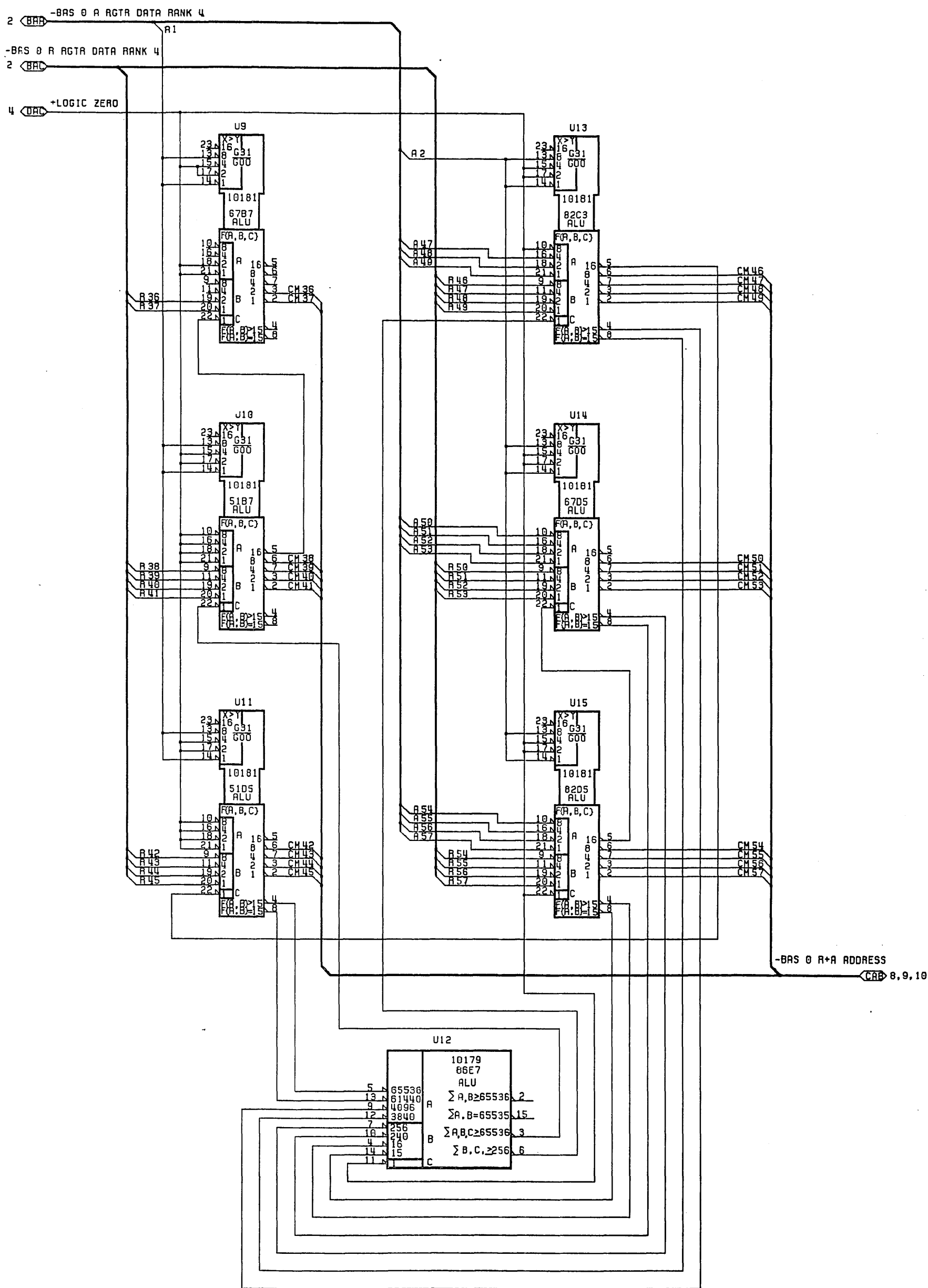
-BAS 0 R RGTR DATA RANK 4 3,4



5 TOTAL LINE LENGTH NO LONGER THEN 12 INCHES

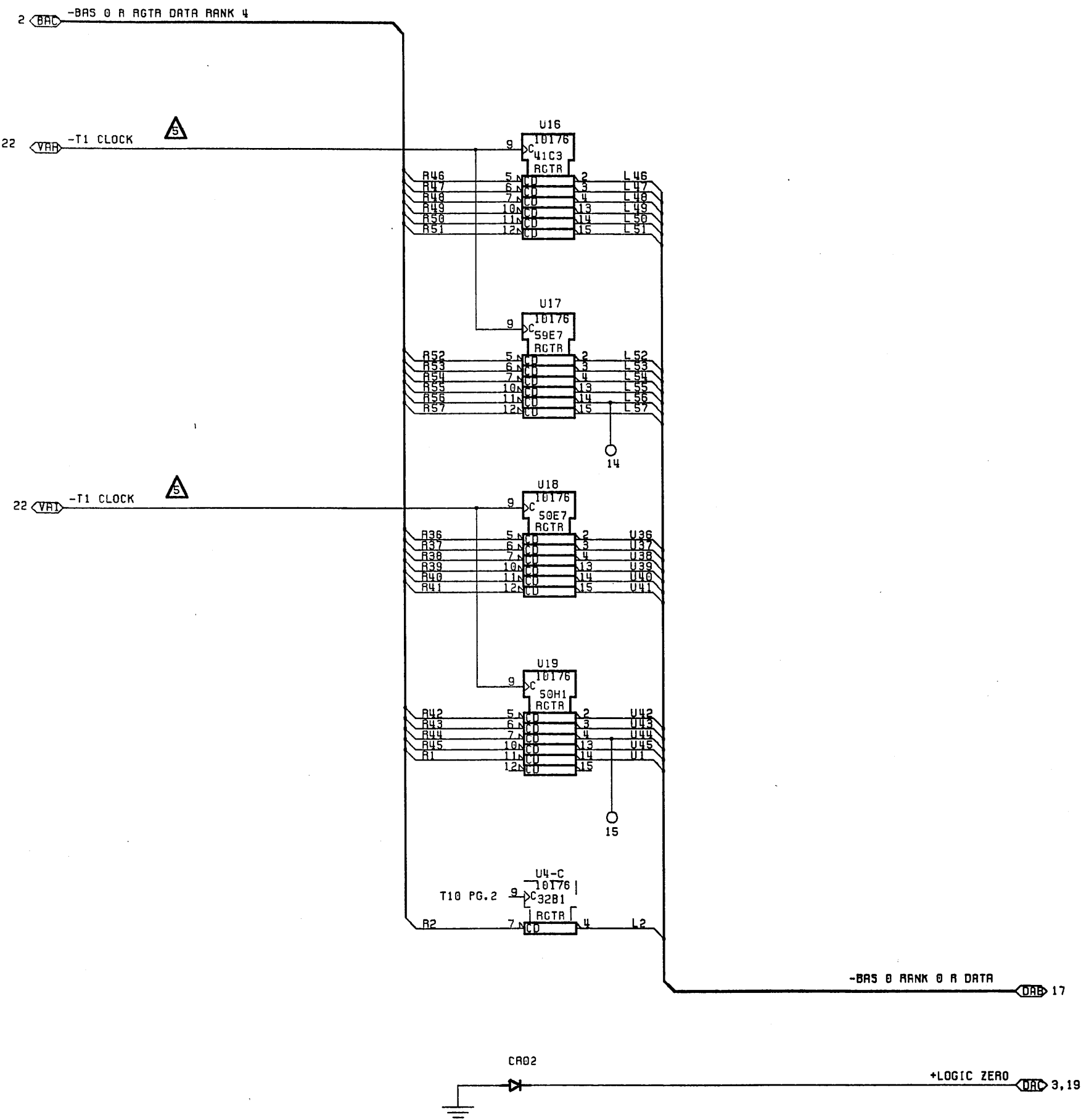
 CONTROL DATA	R+A BOARD BARREL 0 A AND A REGISTERS, RANK 4 TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV
			53575502	11/05/86	C
			SHEET NO. 2	60462210	PAGE JC-02

BAS 0 R+A ADRS



CONTROL DATA	R+A BOARD BARREL 0 R+A ADDRESS		B	DWG NO. 53575502	DATE 11/05/86	REV C
	TYPE 1JCH/1JUH		N	SHEET NO. 3	68462210	PAGE
						JC-03

BAS 0 R RGTR RANK 0



CD	R UPPER BITS
2	R36 - R50
1	R36 - R45

\triangleleft TOTAL LINE LENGTH NO LONGER THEN 12"

CONTROL DATA	A+A BOARD BARREL 0, R RGTR LOWER RANK 0 AND R RGTR UPPER RANK 0 MUX TYPE 1JCH/1JUH	B	DWG NO. 53575502	DATE 11/05/86	REV C
			SHEET NO. 4	60462210	PAGE JC-04



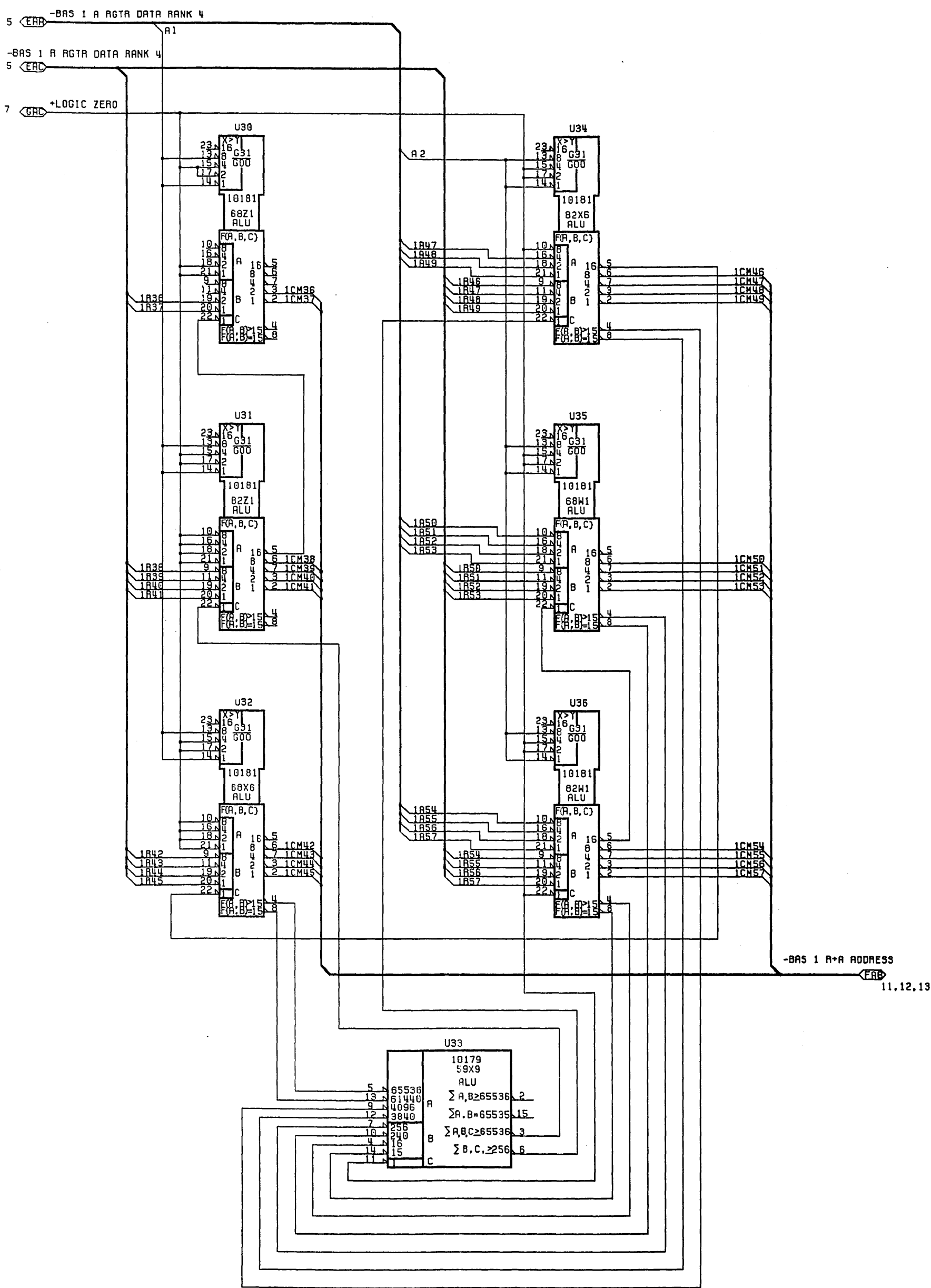
CONTROL
DATA


E

REV

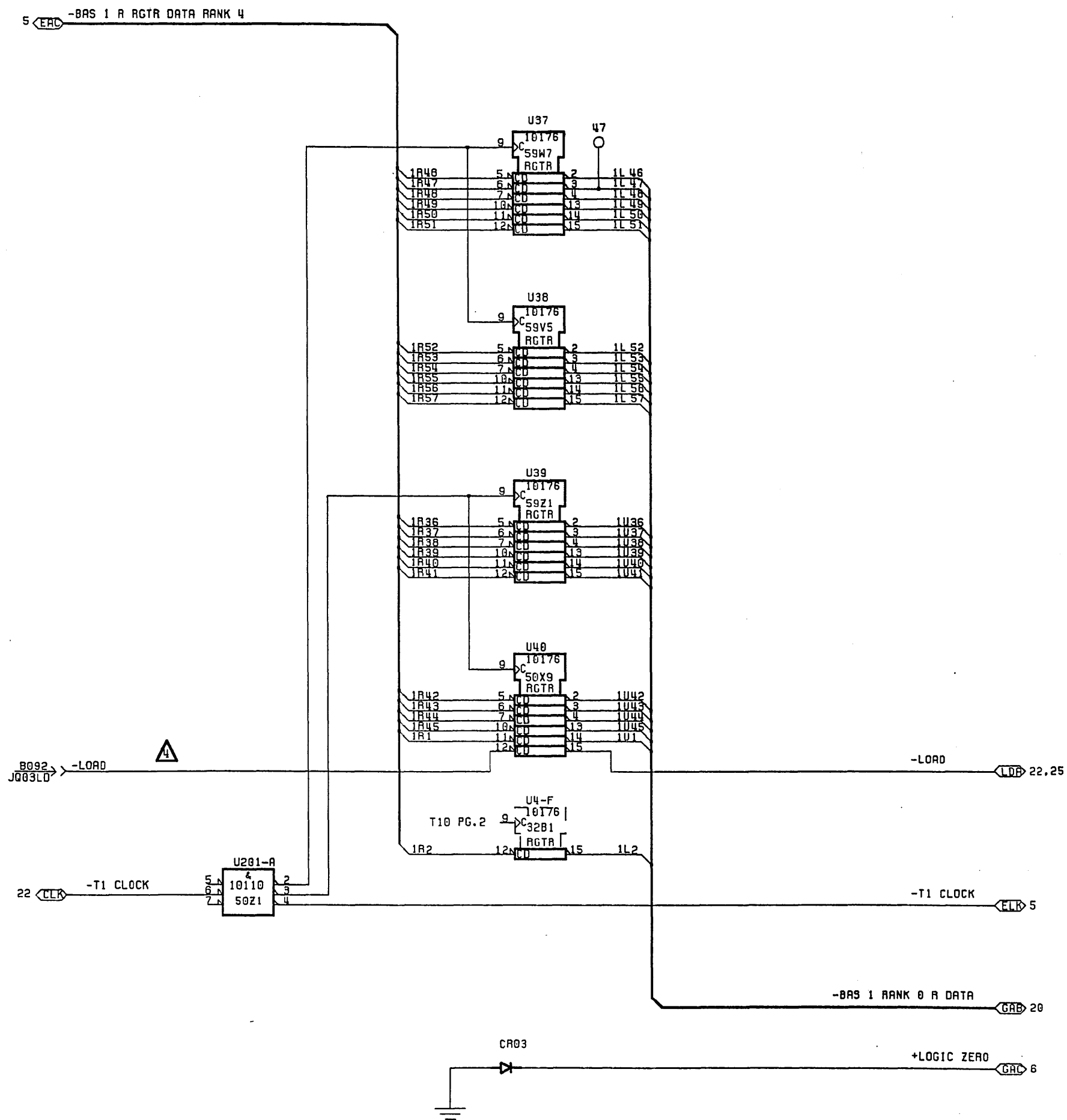
PAGE 16 OF 17

BAS 1 R+A ADRS



 CONTROL DATA	R+A BOARD BARREL 1 R+A ADDRESS		B	DWG NO. 53575502	DATE 11/05/86	REV C
	TYPE 1JCH/1JUH			SHEET NO. 6	60462210	PAGE JC-06
			N			

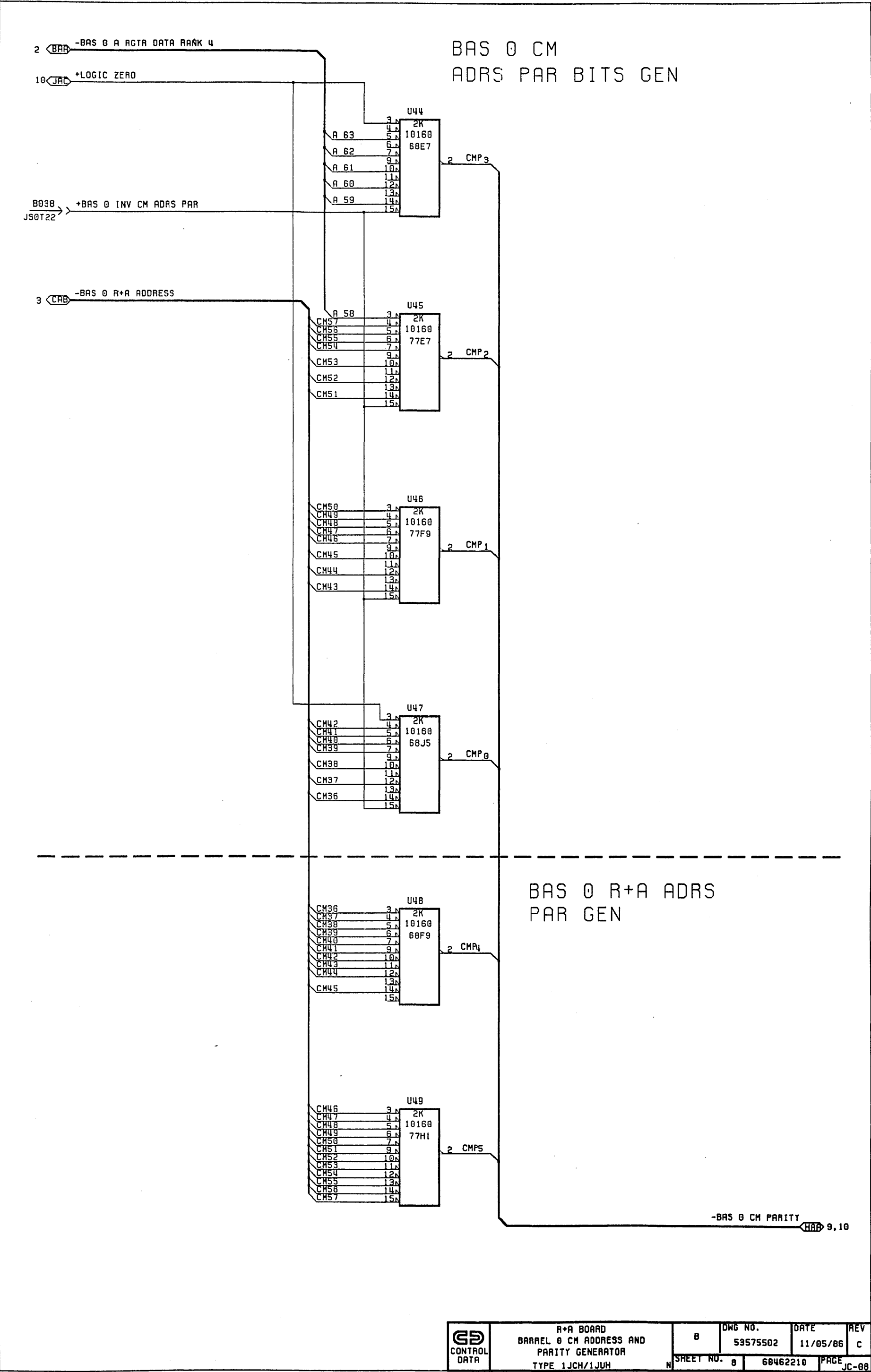
BAS 1 R RGTR RANK 0



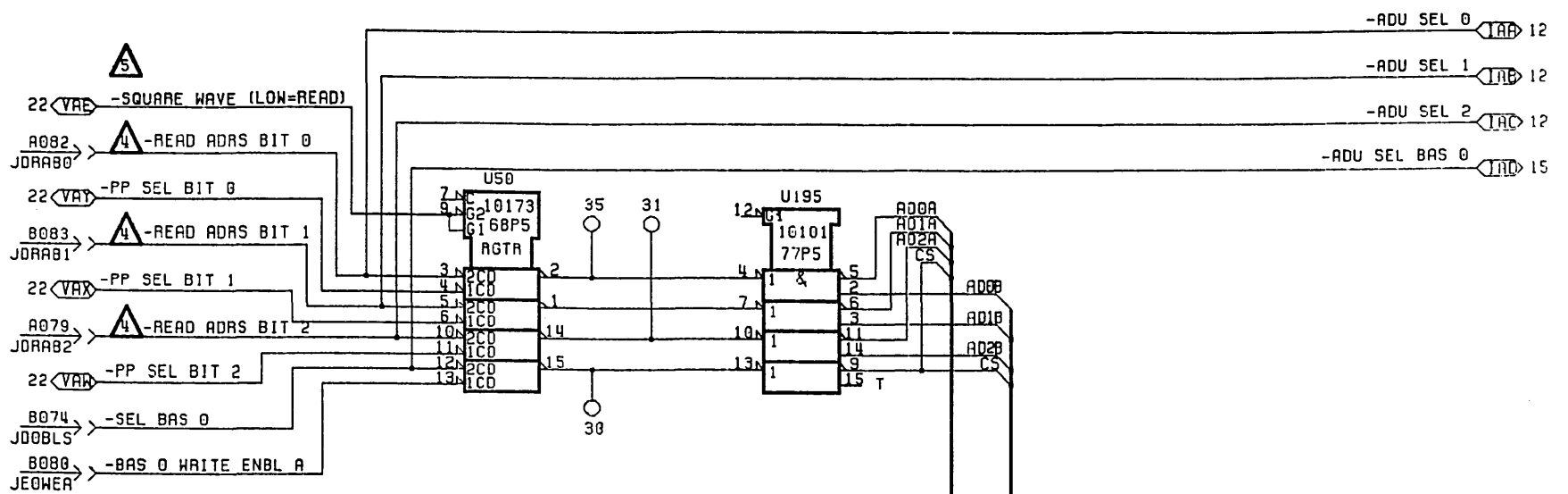
CD	R UPPER BITS
2	R36 - R50
1	R36 - R45

Δ GROUP TERMINATOR

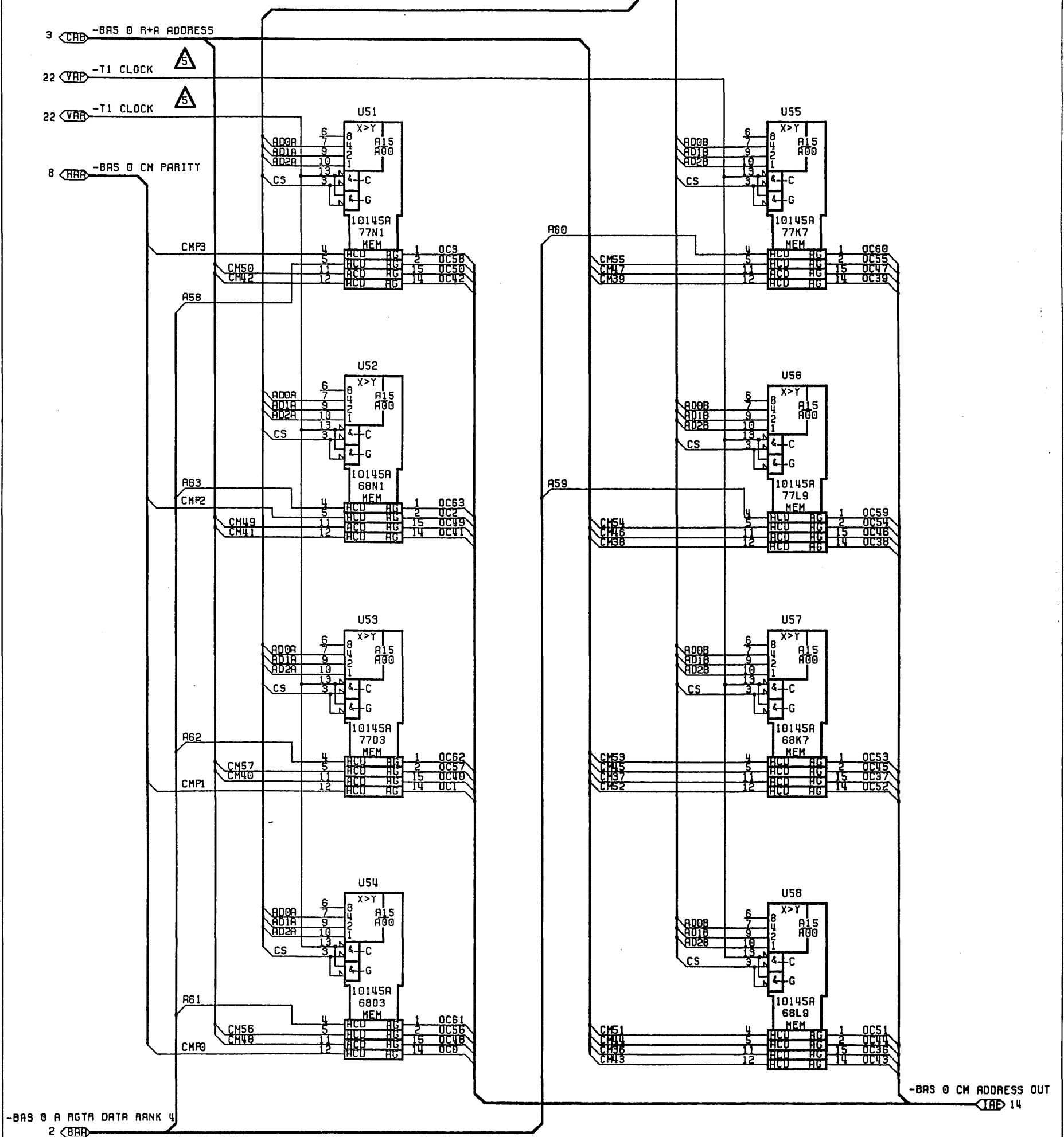
 CONTROL DATA	R+A BOARD BARREL 1, R REGISTER LOWER RANK AND R REGISTER UPPER RANK MUX TYPE 1JCH/1JUH				B	DWG NO. 53575502		DATE 11/05/86		REV C	
	SHEET NO. 7					60462210		PAGE		JC-07	




BAS 0 CM ADRS STORE CONTROL



BAS 0 CM ADRS STORE RAMS

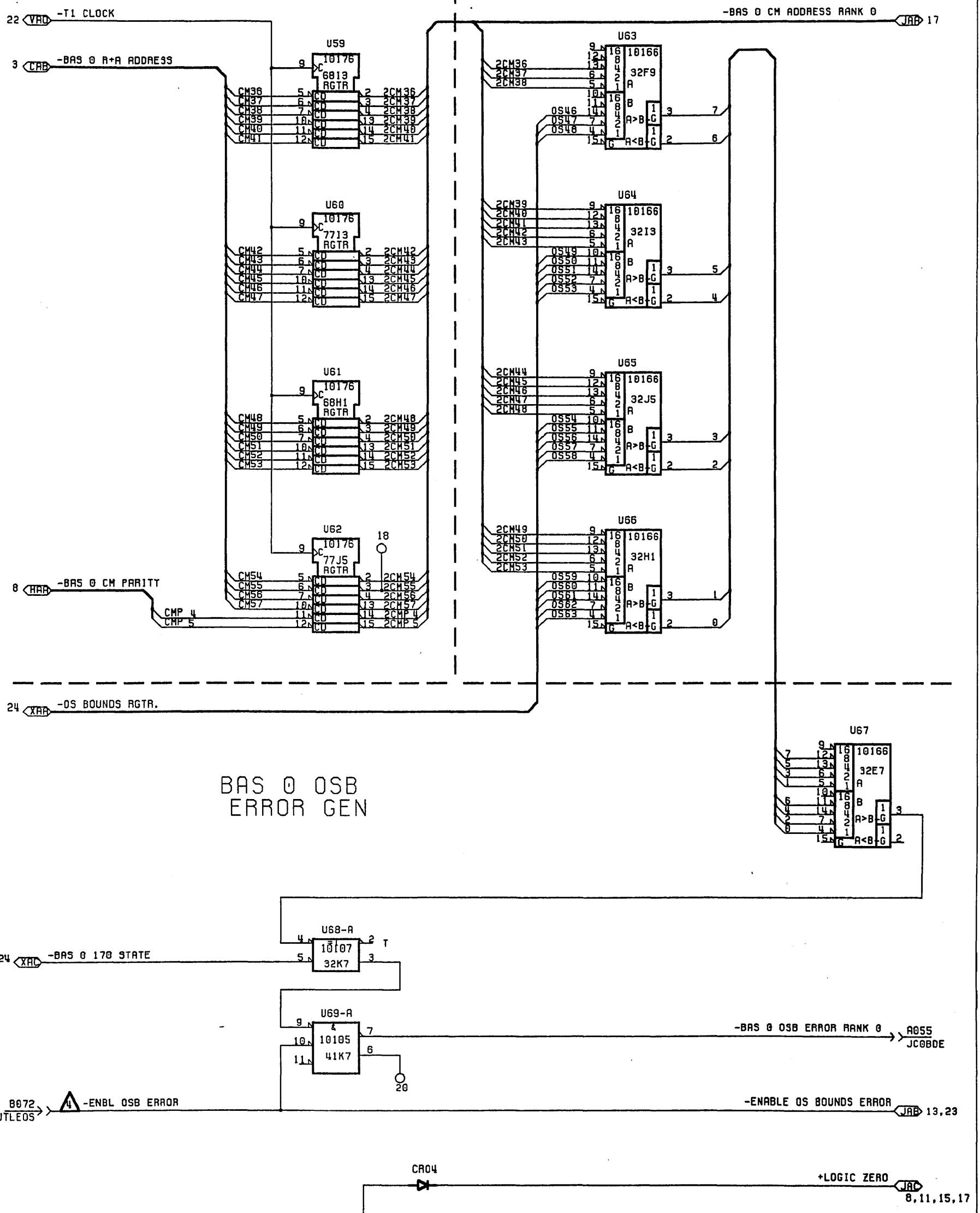


- GROUPED TERMINATORS
- LINE LENGTH NO LONGER THEN 12"


 CONTROL DATA	A+A BOARD BARREL 0 CM ADDRESS STORE CONTROL AND STORE TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV
			53575502	11/05/86	C
			SHEET NO. 9	60462210	PAGE JC-09

BAS 0 CM ADRS RANK 0

BAS 0 OSB ERROR CHECKER



GROUPED TERMINATORS

 CONTROL DATA	R+A BOARD BAS 0 CM ADDRESS RANK0 AND OS BOUNDS CHECK AND ERROR GEN TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV
			53575502	11/05/86	C
N		SHEET NO.	10	60462210	PAGE
					JC-10

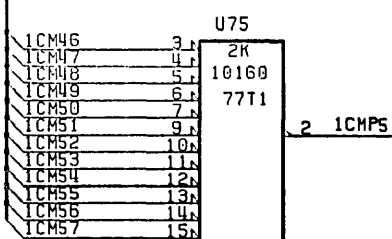
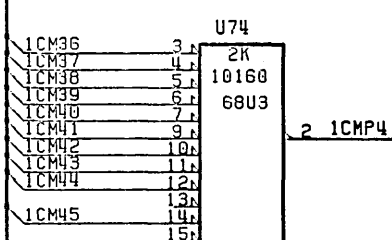
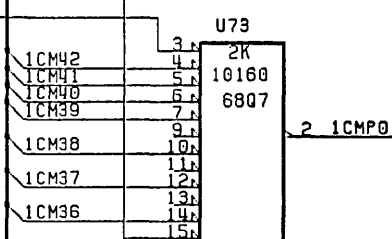
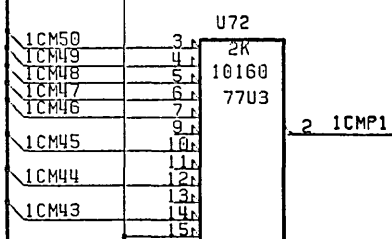
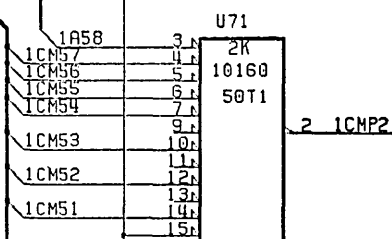
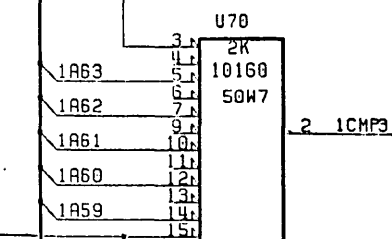
5 ~~FAB~~ -BAS 1 A RCTA DATA BANK 4

10 ~~JAC~~ +LOGIC ZERO

A093 +BAS 1 INV CM ADRS PAR
J51T22

6 ~~FAB~~ -BAS 1 R+A ADDRESS

BAS 1 CM ADRS
PAR BITS GEN

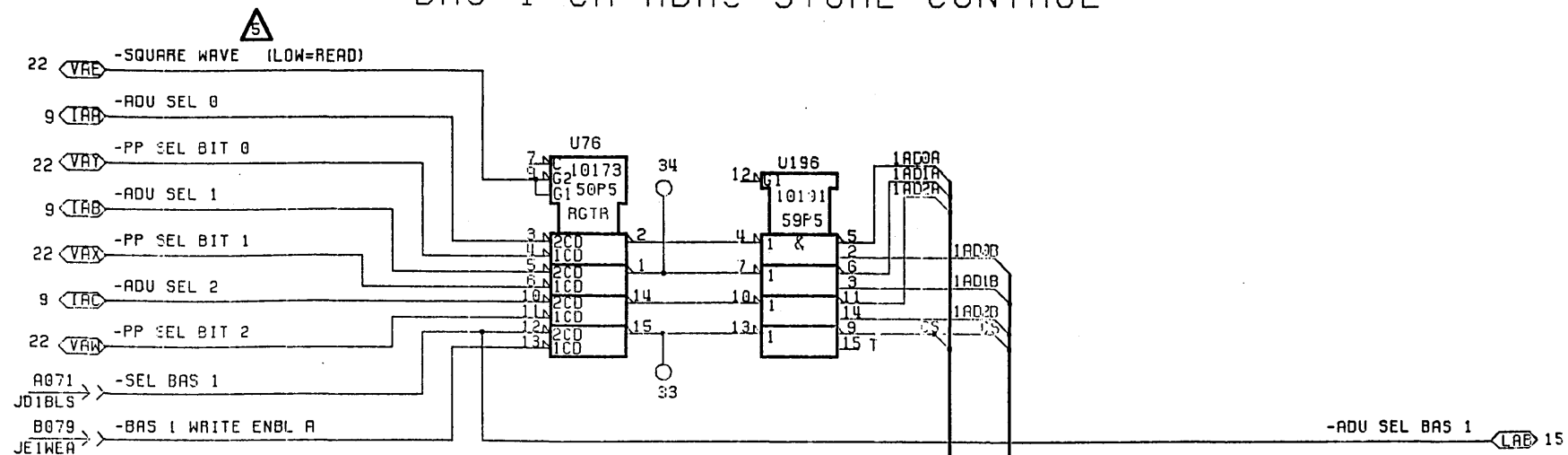


-BAS 1 CM PARITY ~~KAP~~ 12,13

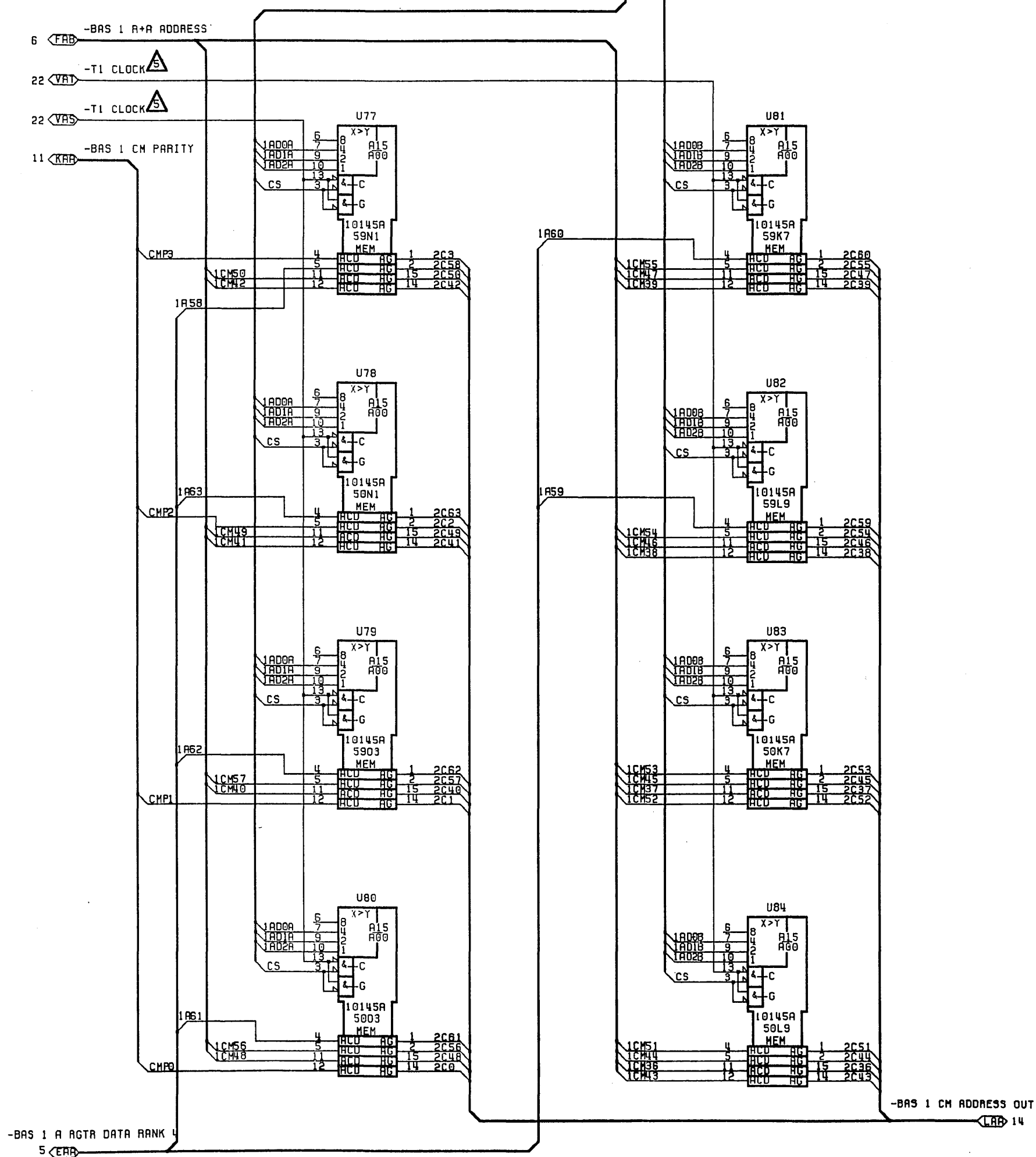
BAS 1 R+A ADRS
PAR GEN

GD CONTROL DATA	R+A BOARD BARREL 1 CM ADDRESS AND PARITY GENERATOR TYPE 1JCH/1JUH		B	DWG NO. 53575502	DATE 11/05/86	REV C
	N		SHEET NO. 11	60462210	PAGE	JC-11

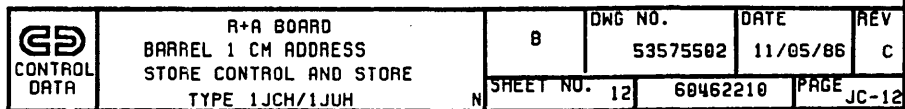
BAS 1 CM ADRS STORE CONTROL



BAS 1 CM ADRS STORE RAMS

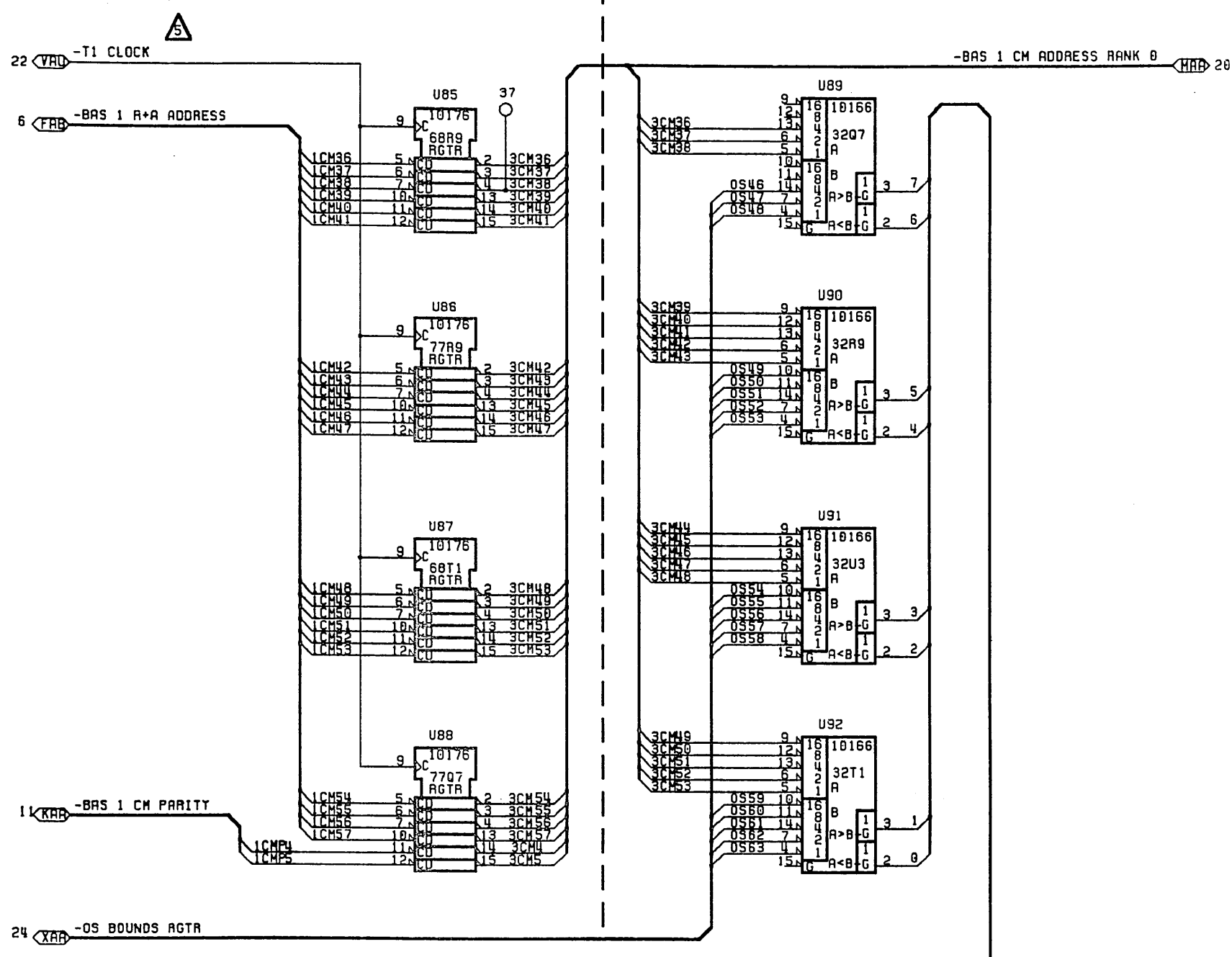


5 LINE LENGTH NO LONGER THEN 12"

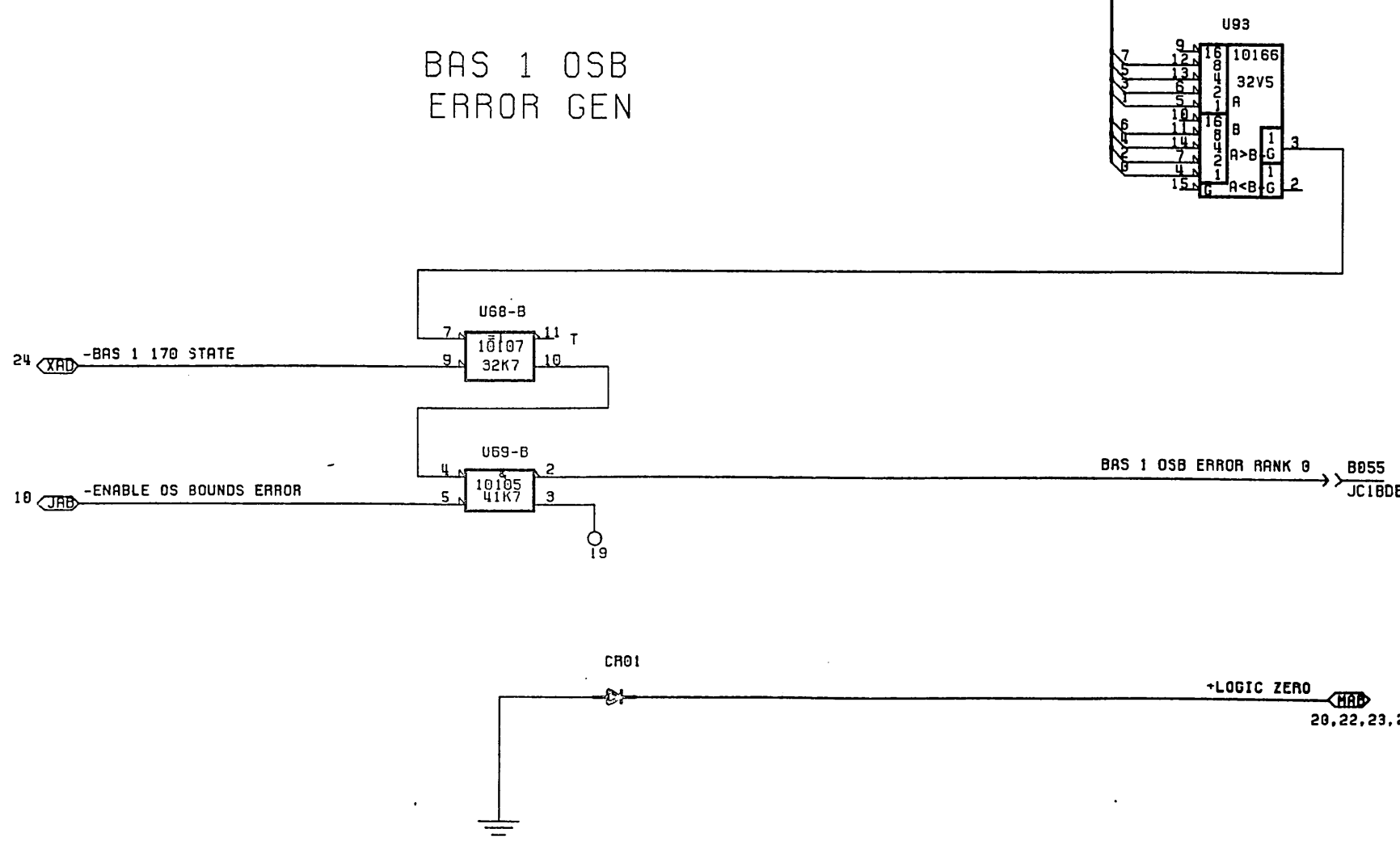


BAS 1 CM ADRS RANK 0


BAS 1 OSB ERROR CHECKER



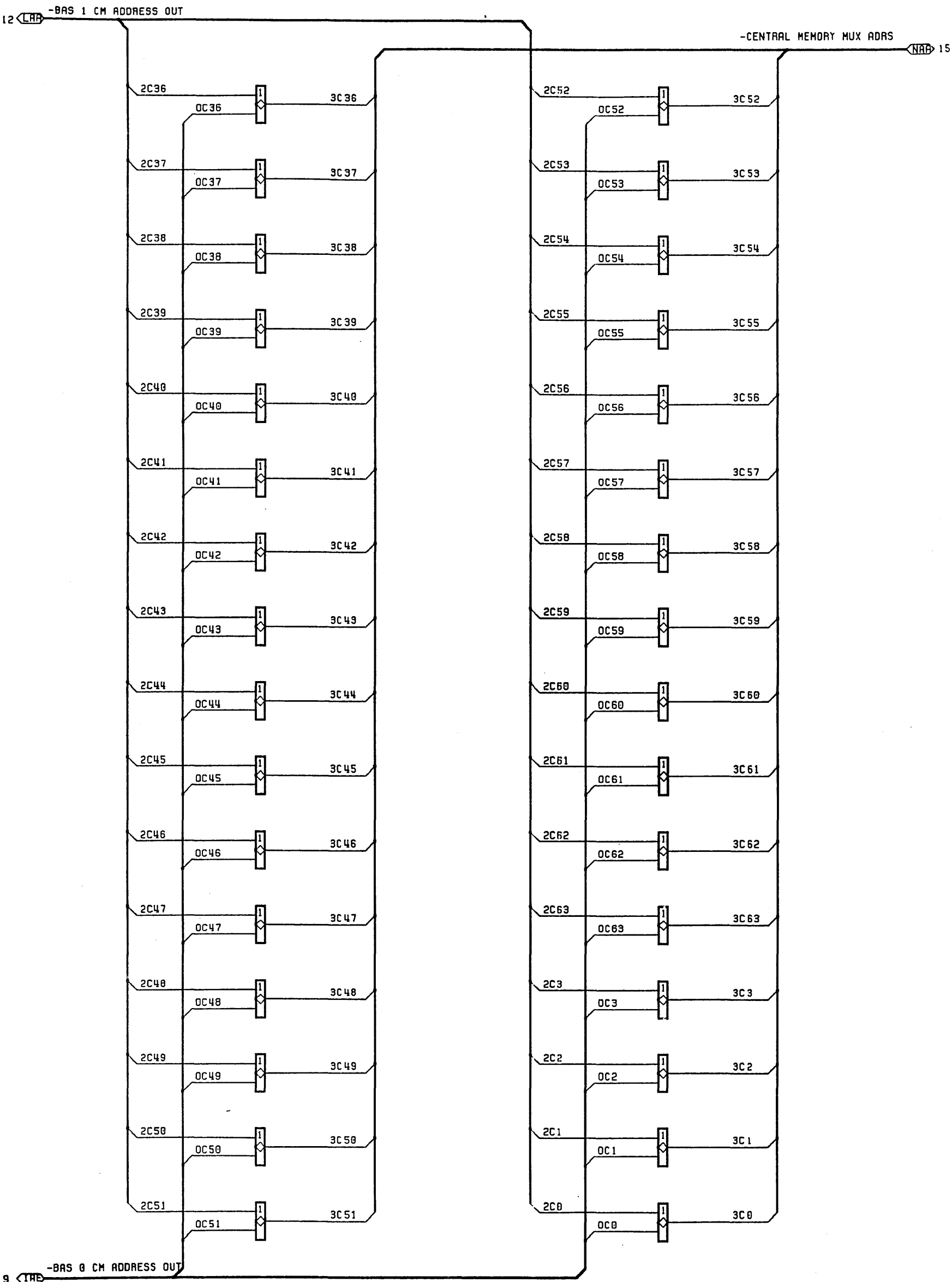
BAS 1 OSB
ERROR GEN



LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R+A BOARD		B	DWG NO.	DATE	REV
	BARREL 1 CM ADDRESS RANK 0 AND			53575502	11/05/86	C
	OS BOUNDS CHECK AND ERROR GEN					
TYPE 1JCH/1JUH		N	SHEET NO. 13		60462210	PAGE JC-13

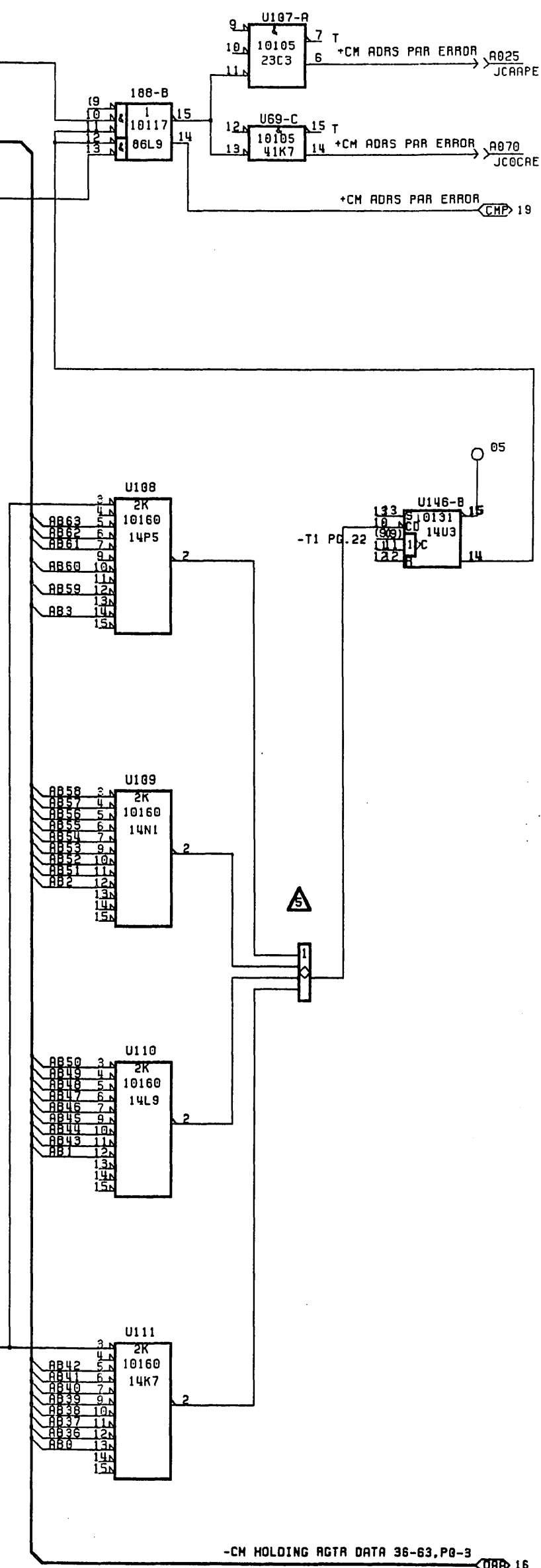
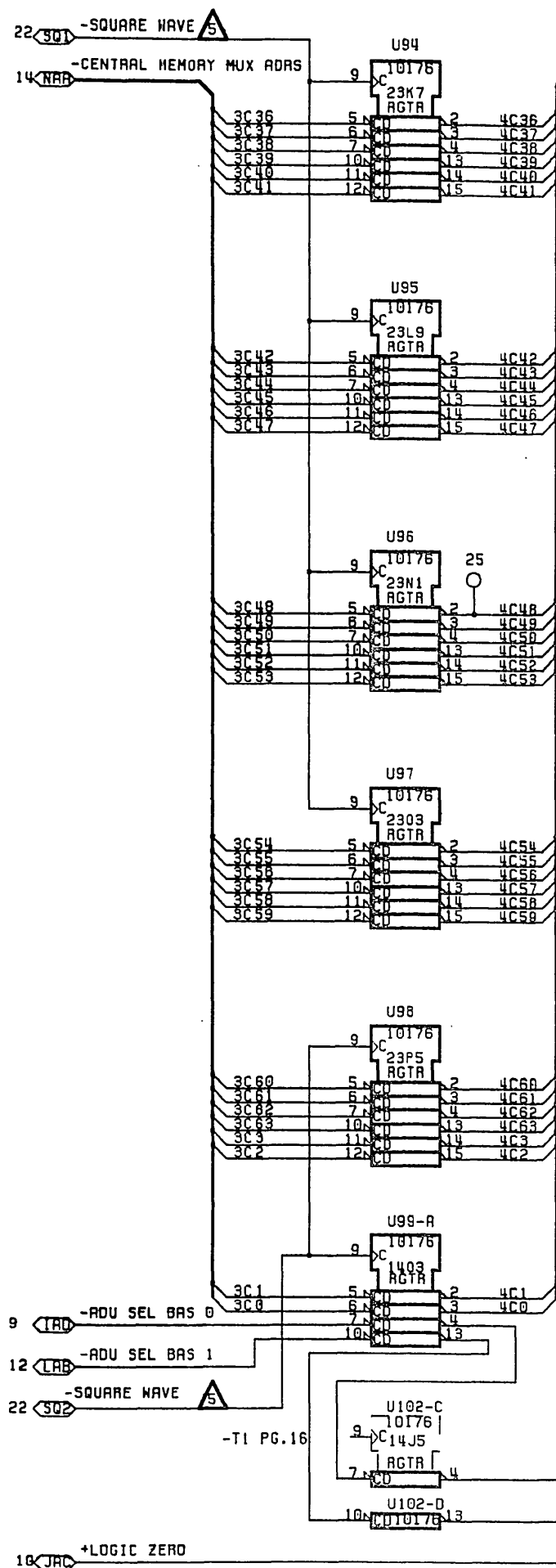
CM ADRS MUX




GD CONTROL DATA	R+A BOARD CENTRAL MEMORY ADDRESS OUTPUT DATA MUX TYPE 1JCH/1JUH		B	DWG NO.	DATE	REV
				59575502	11/05/86	C
				SHEET NO. 14	60462210	PAGE JC-14

CM ADRS HLDG RGTR

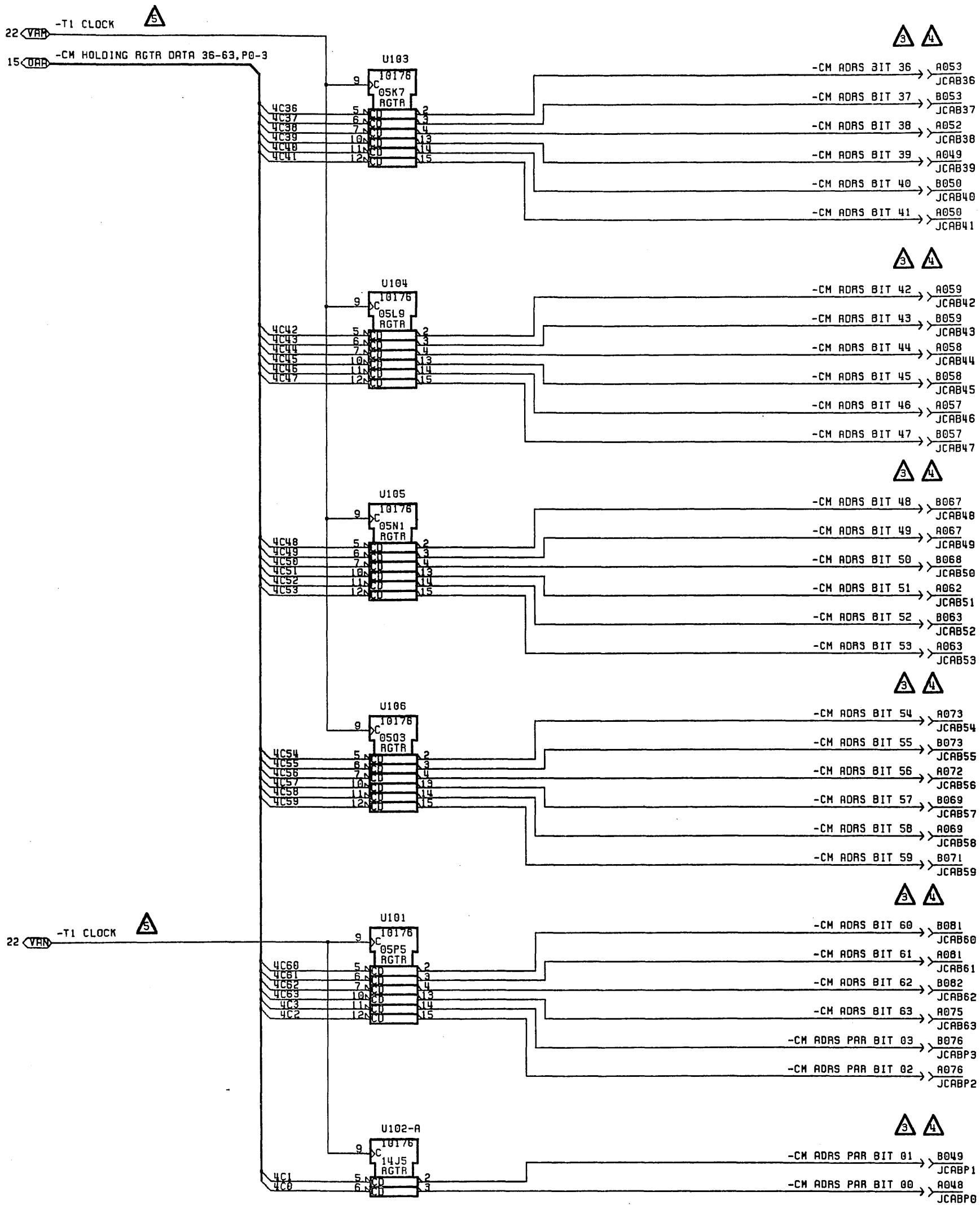
CM ADRS OUT PAR CHECK



S LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	A+A BOARD CM ADDRESS HOLDING REGISTER AND OUTPUT PARITY CHECK TYPE 1JCH/1JUH				B	DWG NO. 53575502	DATE 11/05/86	REV C	
	SHEET NO. 15					60462210	PAGE	JC-15	
	N								


CM ADRS REALIGNMENT RGTR



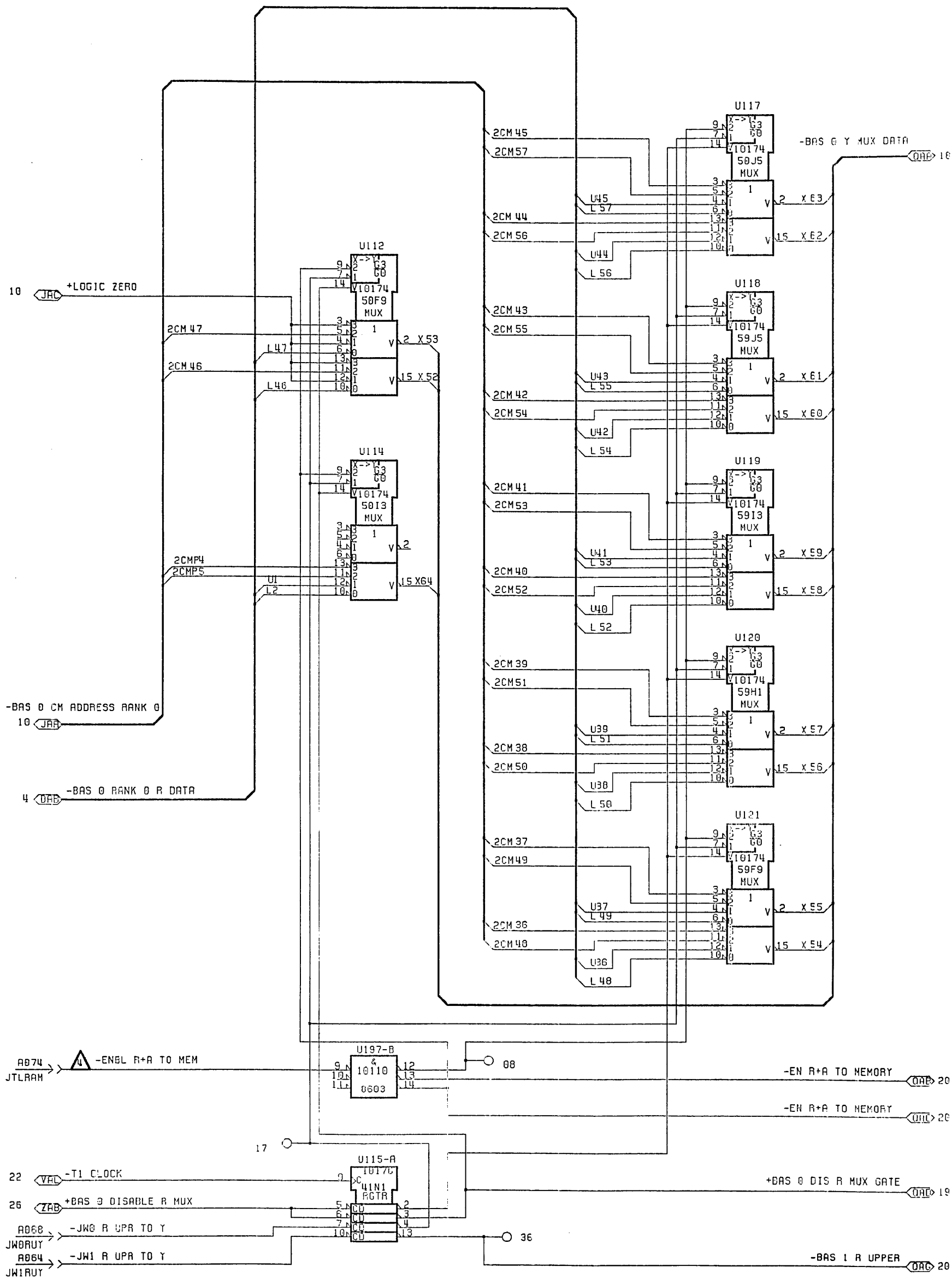
3 THESE OUTPUT PINS TERMINATED
ON THIS BOARD

4 GROUPED TERMINATORS

5 LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R+A BOARD CM ADDRESS REALIGNMENT RGTA AND OUTPUT TYPE 1JCH/1JUH	B	DWG NO. 53575502	DATE 11/05/86	REV C
	N		SHEET NO. 16	60462210	PAGE
			JC-16		

BAS 0 R TO Y MUX



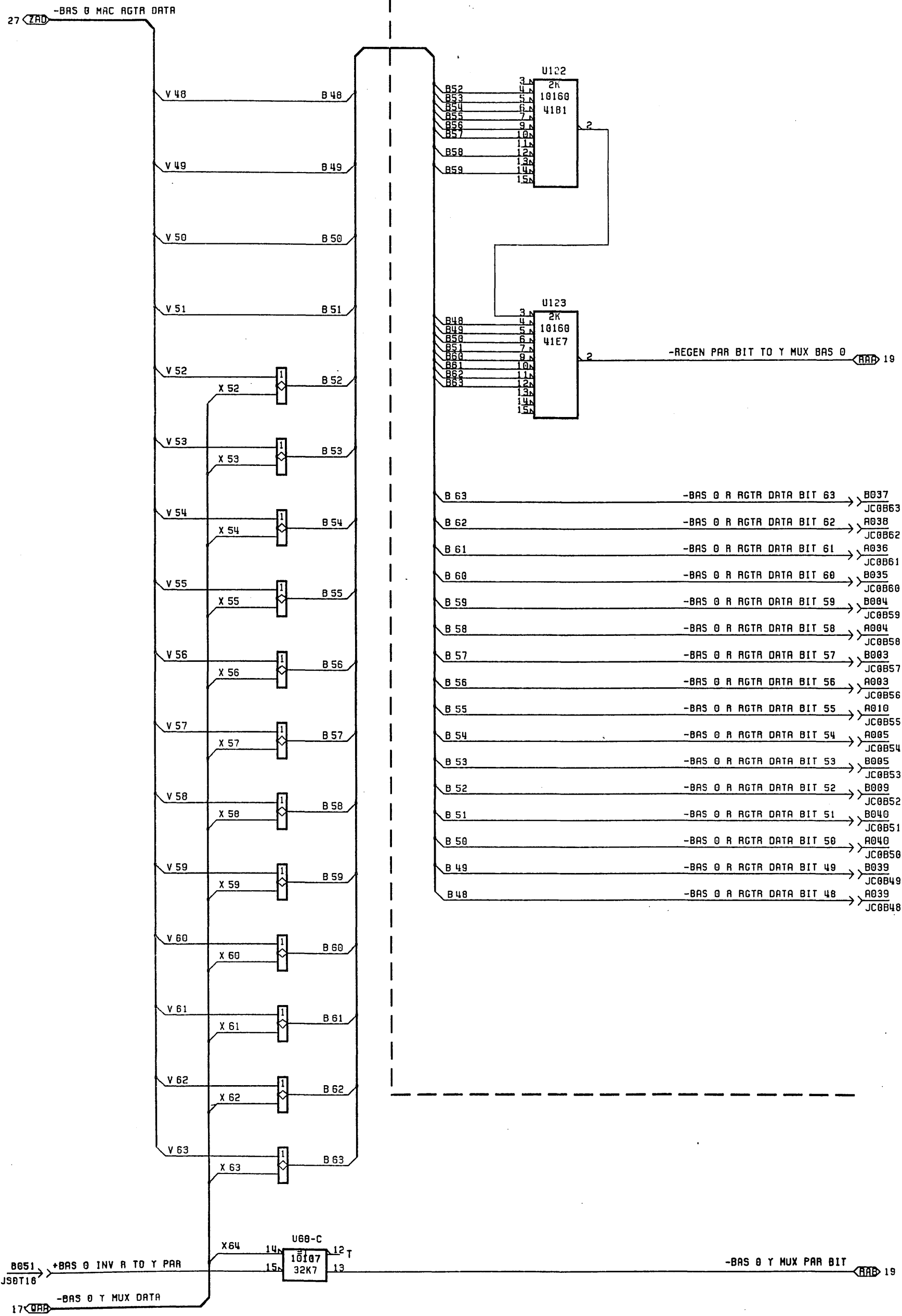
CD	MUX SELECT
0	R LOWER
1	R UPPER
2	R+A LOWER
3	R+A UPPER

GROUPED TERMINATORS

CONTROL DATA	R+A BOARD BARREL 0 R TO Y MUX TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV
			53575502	11/05/86	C
			SHEET NO. 17	60462210	PAGE JC-17

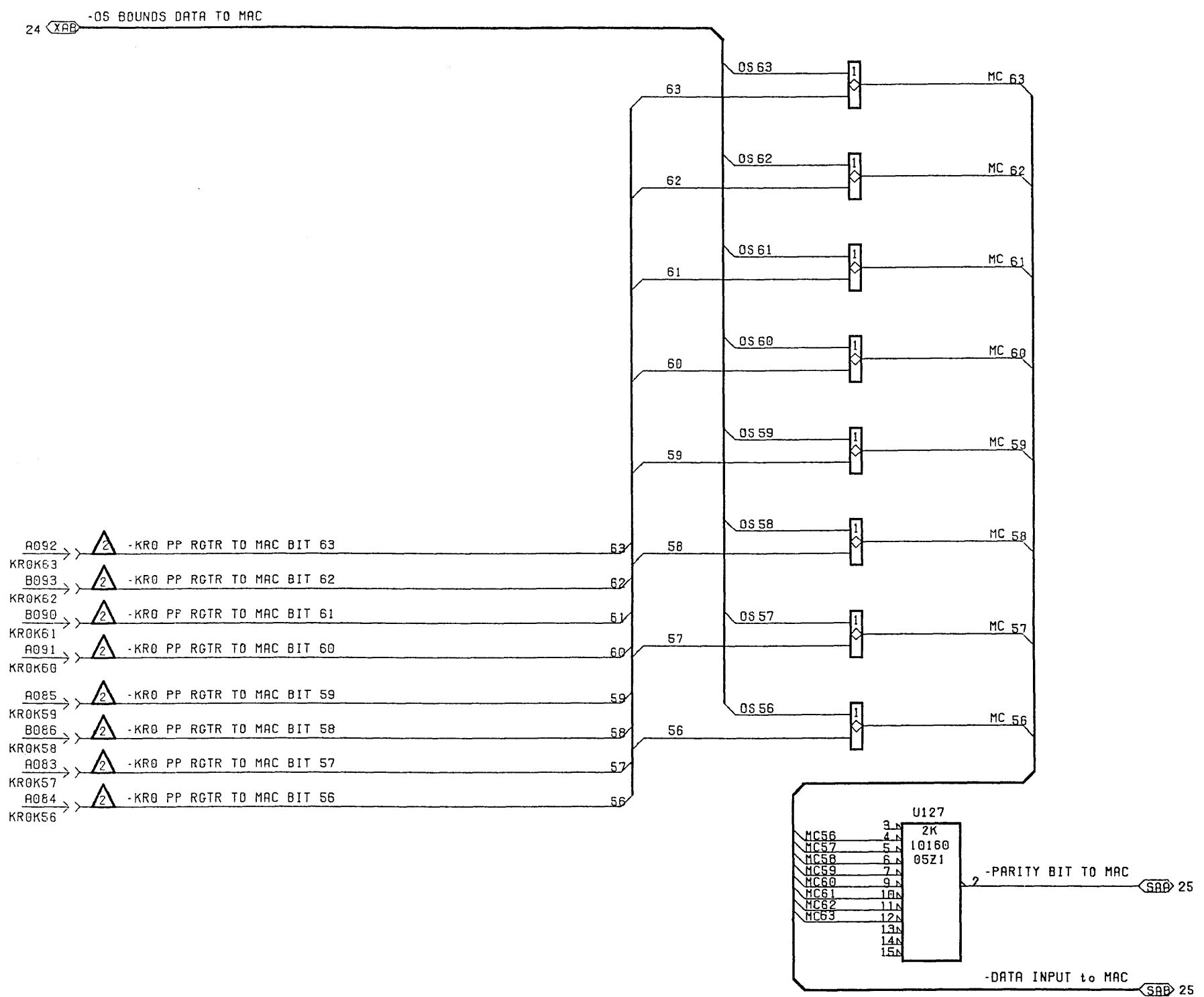
BAS 0 R TO Y DATA MUX

BAS 0 R TO Y DATA OUT

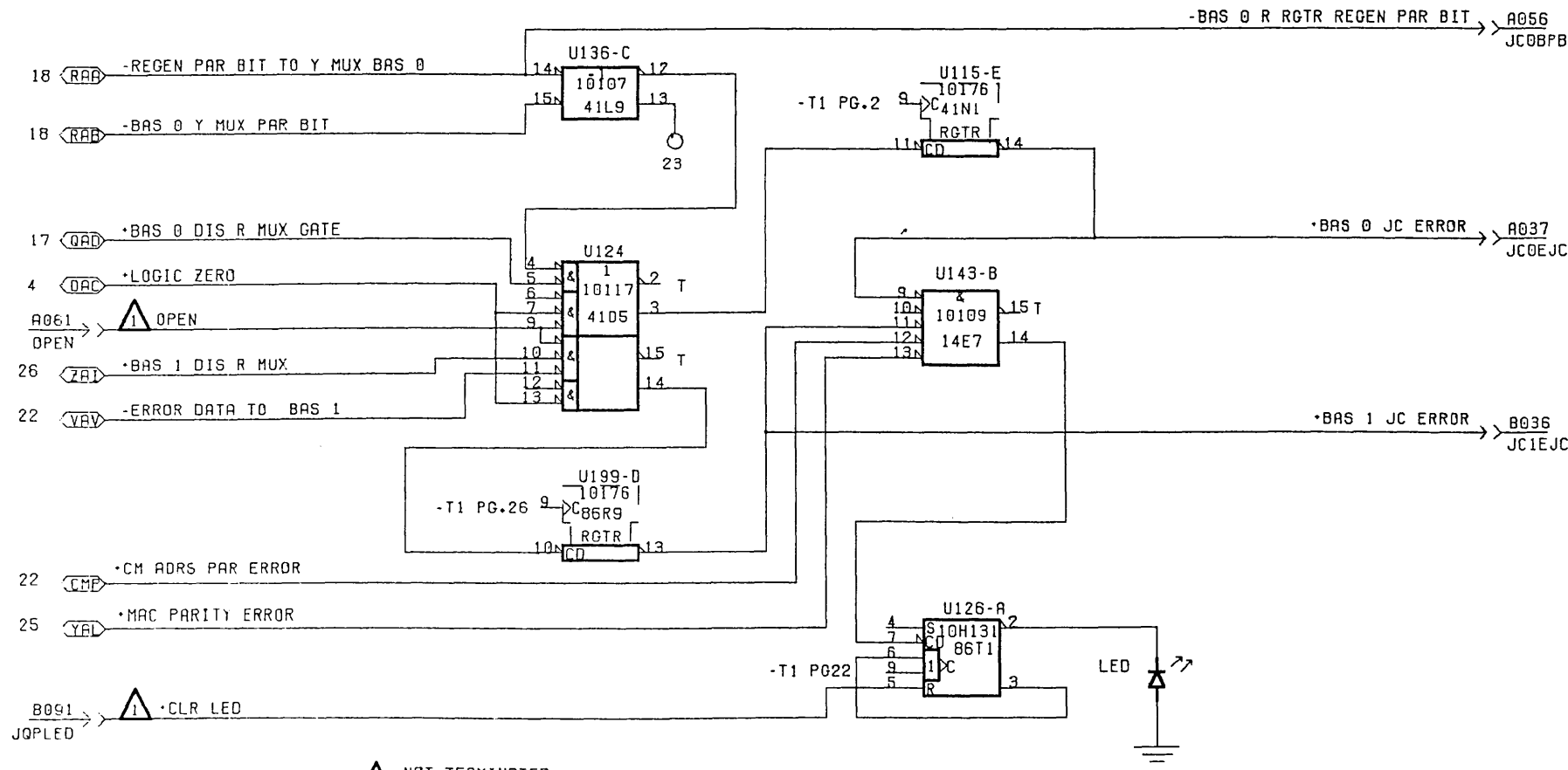


CONTROL DATA	R+A BOARD BARREL 0, R TO Y DATA MUX AND DATA OUTPUT TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV
			53575502	11/05/86	C
			SHEET NO. 18	60462210	PAGE JC-18


DATA TO MAC MUX



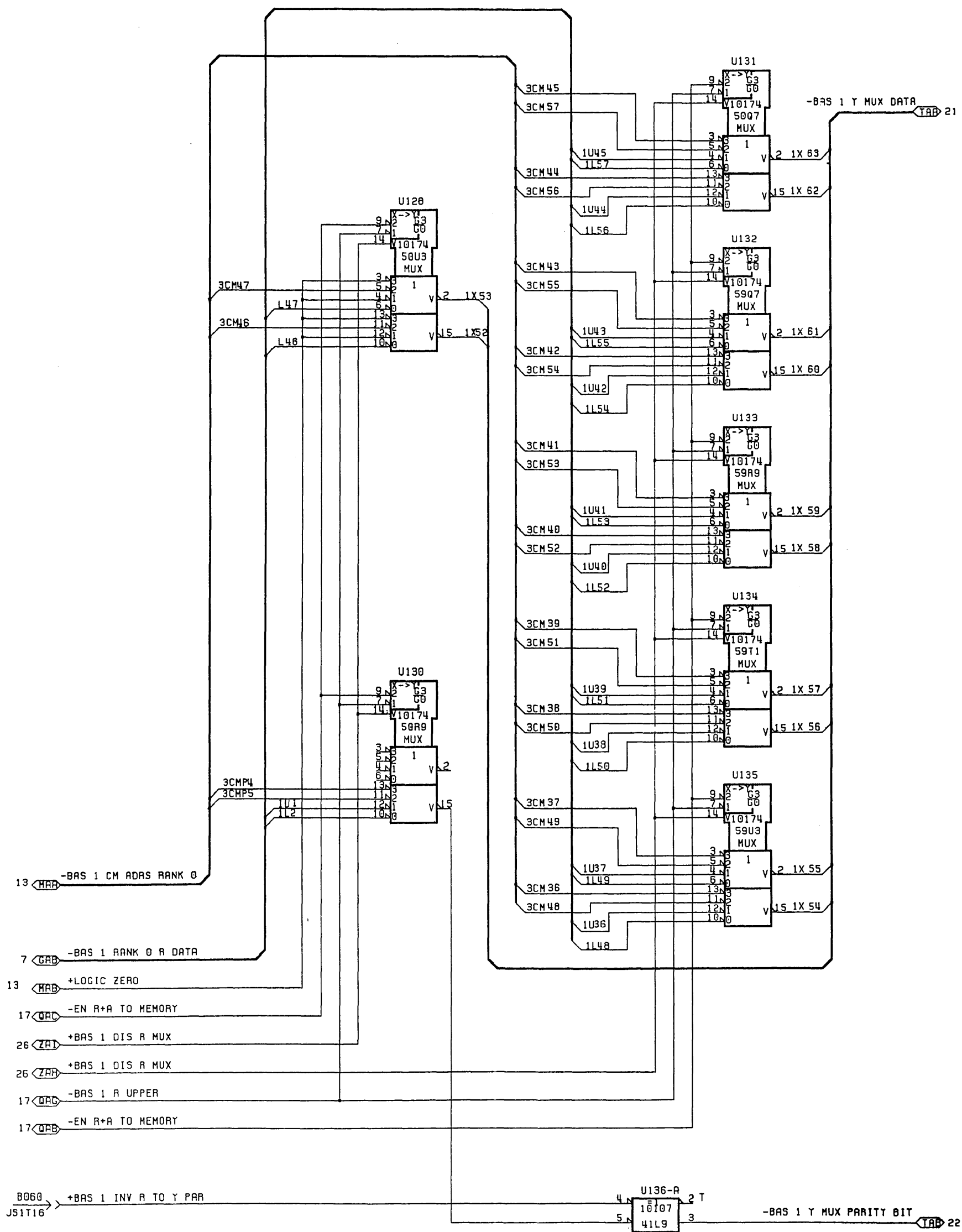
BOARD ERROR GEN



1 NOT TERMINATED
2 LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R-A BOARD DATA TO MAC MUX AND BOARD ERROR GENERATION TYPE 1JCH/1JUH		B	DWG NO. 53575502	DATE 08/21/87	REV D
				SHEET NO. 19	60462210	PAGE JC-19

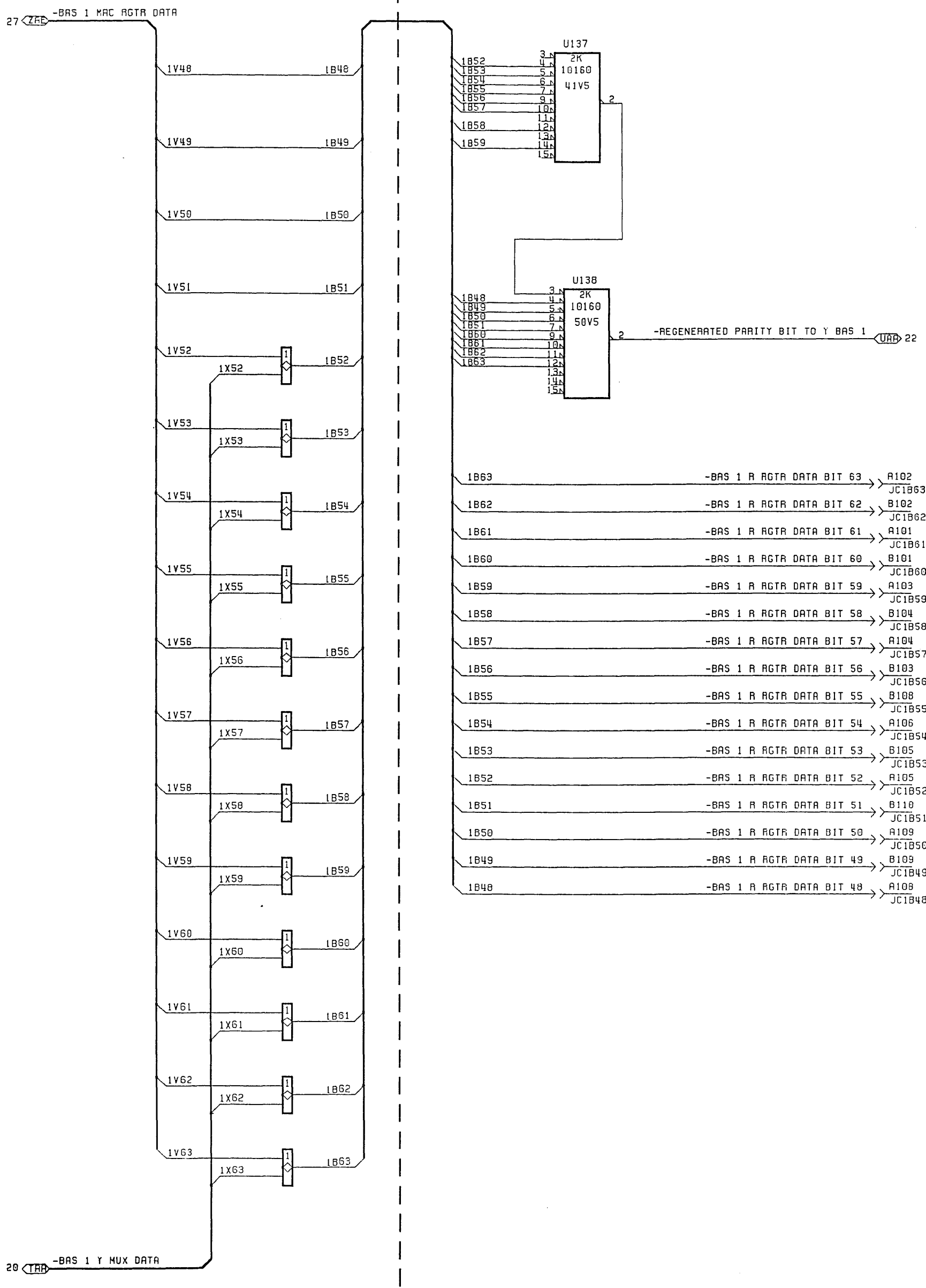
BAS 1 R TO Y MUX



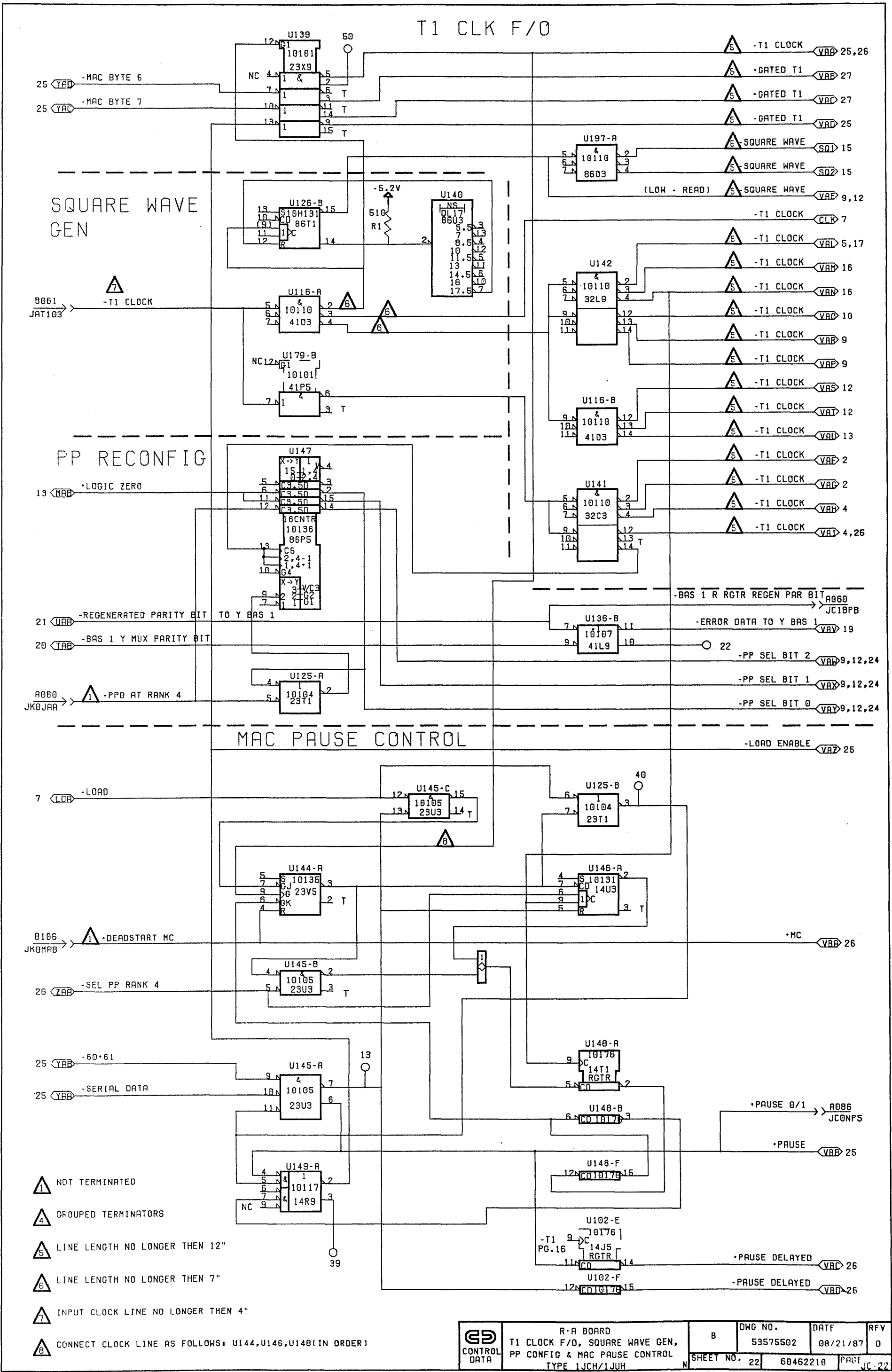
CD	MUX SELECT
0	R LOWER
1	R UPPER
2	R+A LOWER
3	R+A UPPER

BAS 1 R TO Y DATA MUX

BAS 1 R TO Y DATA OUT



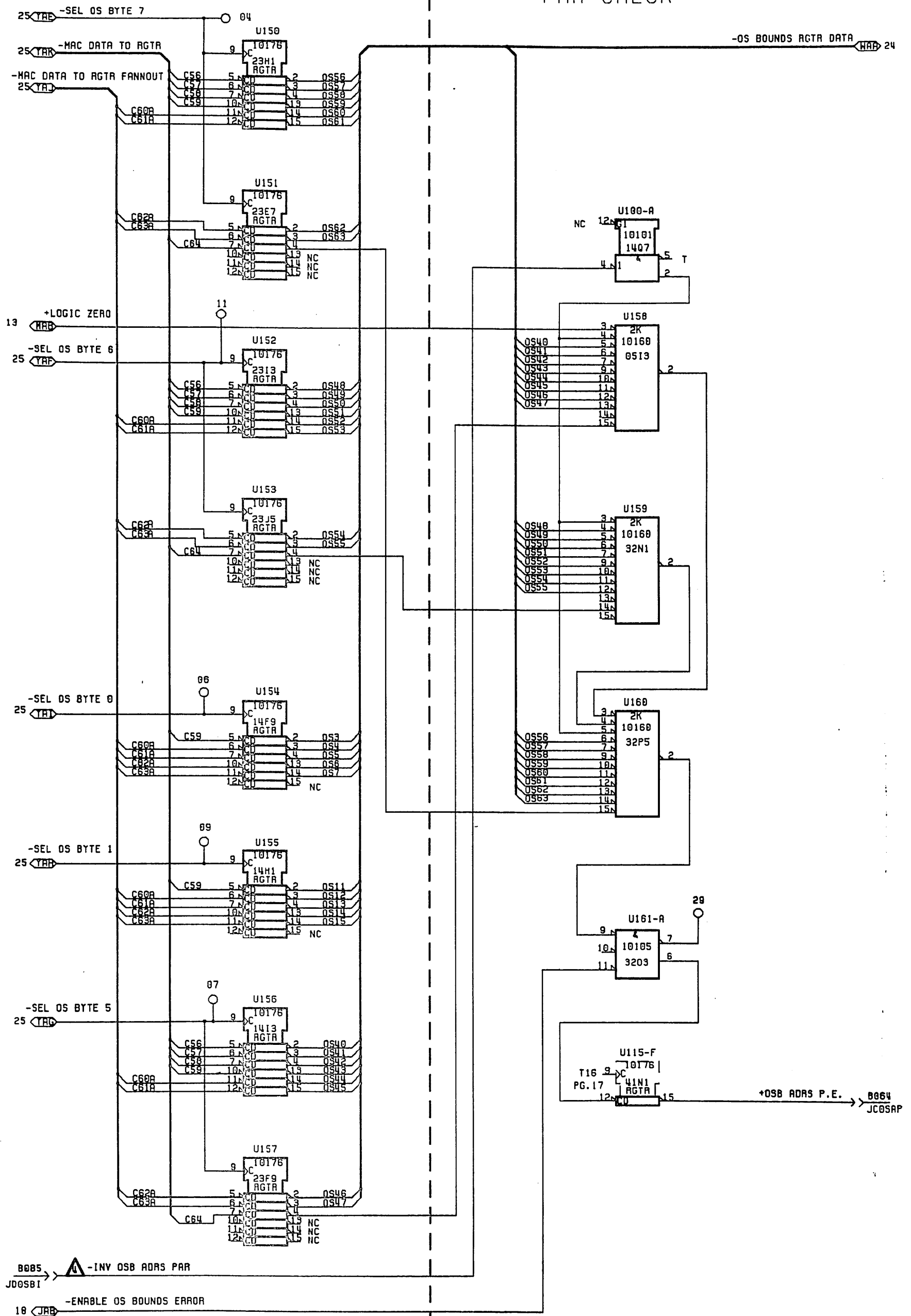
R+A BOARD CONTROL DATA	B	DWG NO.	DATE	REV
		53575502	11/05/86	C
		SHEET NO. 21	60462210	PAGE JC-21



<div> <div>GD</div> <div>CONTROL DATA</div> </div>	R-A BOARD		DWG NO.	DATE	REV
	T1 CLOCK F/O, SQUARE WAVE GEN, PP CONFIG & MAC PAUSE CONTROL		B 53575502	08/21/87	D
	TYPE 1JCH/1JUH		SHEET NO. 22	60462210	PAGE JC-22

OSB RGTR

OSB ADRS PAR CHECK

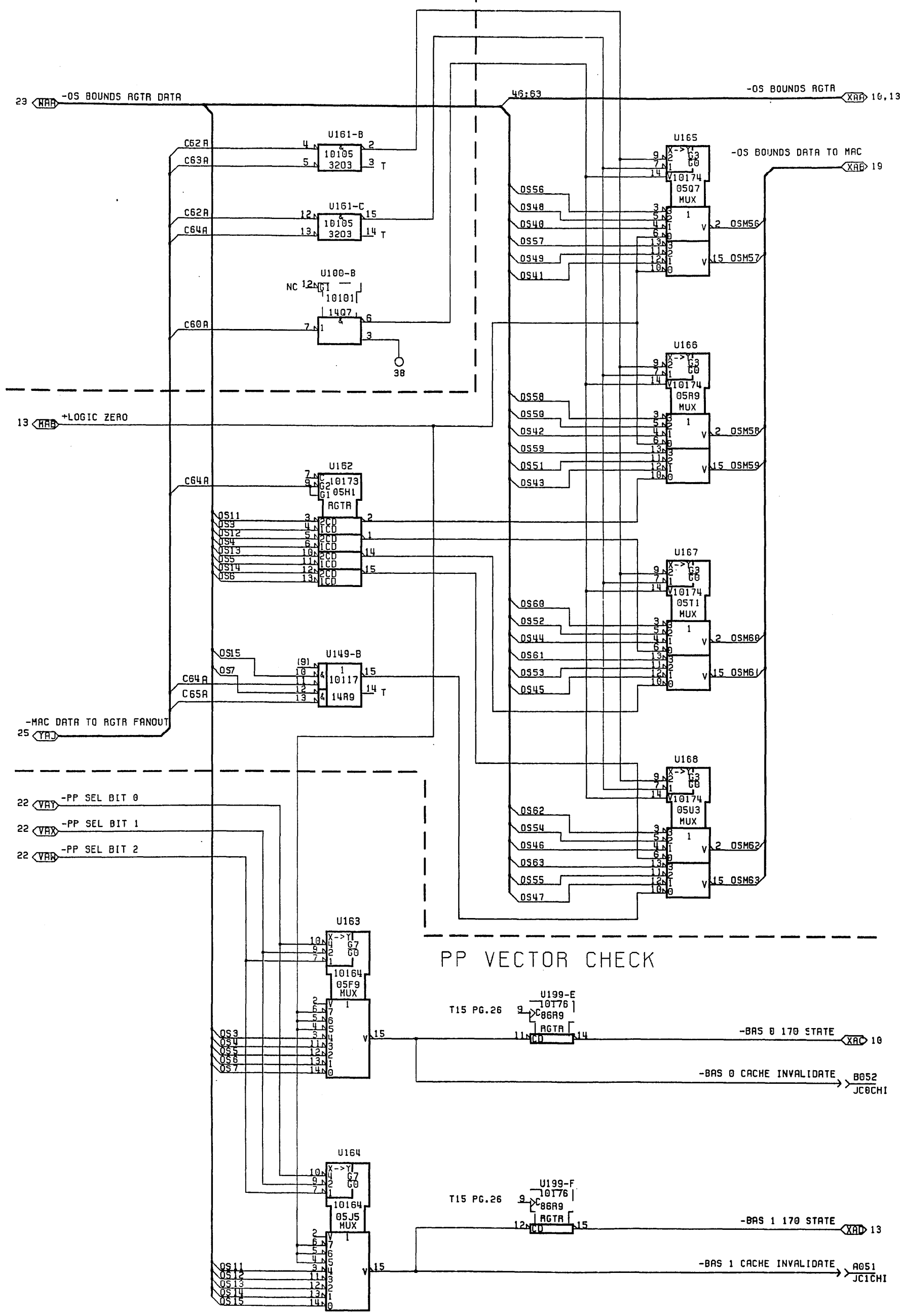



GROUPED TERMINATORS

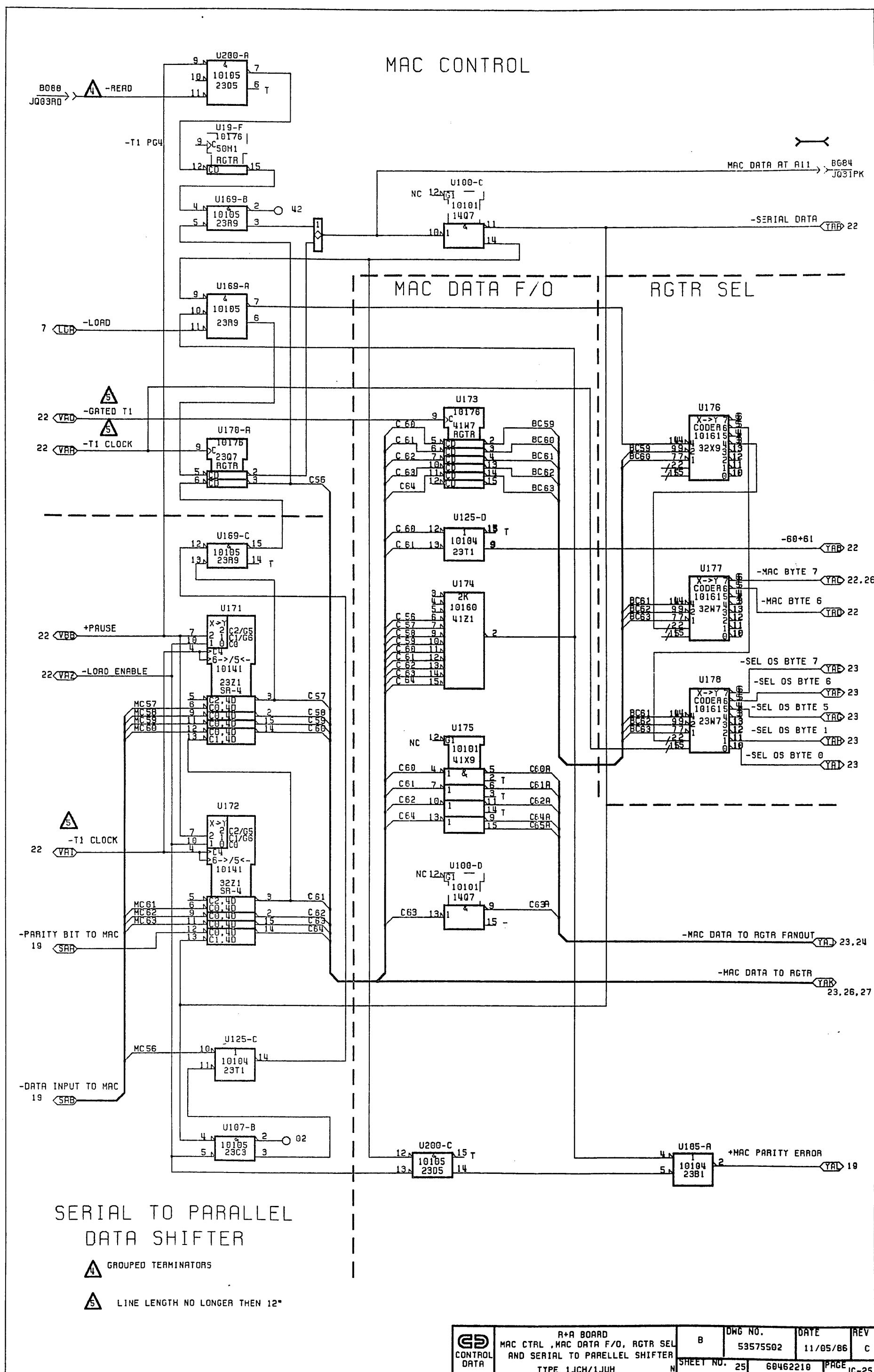
GD CONTROL DATA	R+A BOARD OS BOUNDS REGISTER AND ADDRESS PARITY CHECK TYPE 1JCH/1JUH		DWG NO. 59575502	DATE 11/85/86	REV C
	SHEET NO. 23	60462210	PAGE	JC-23	

OSB MUX CONTROL

OSB DATA MUX

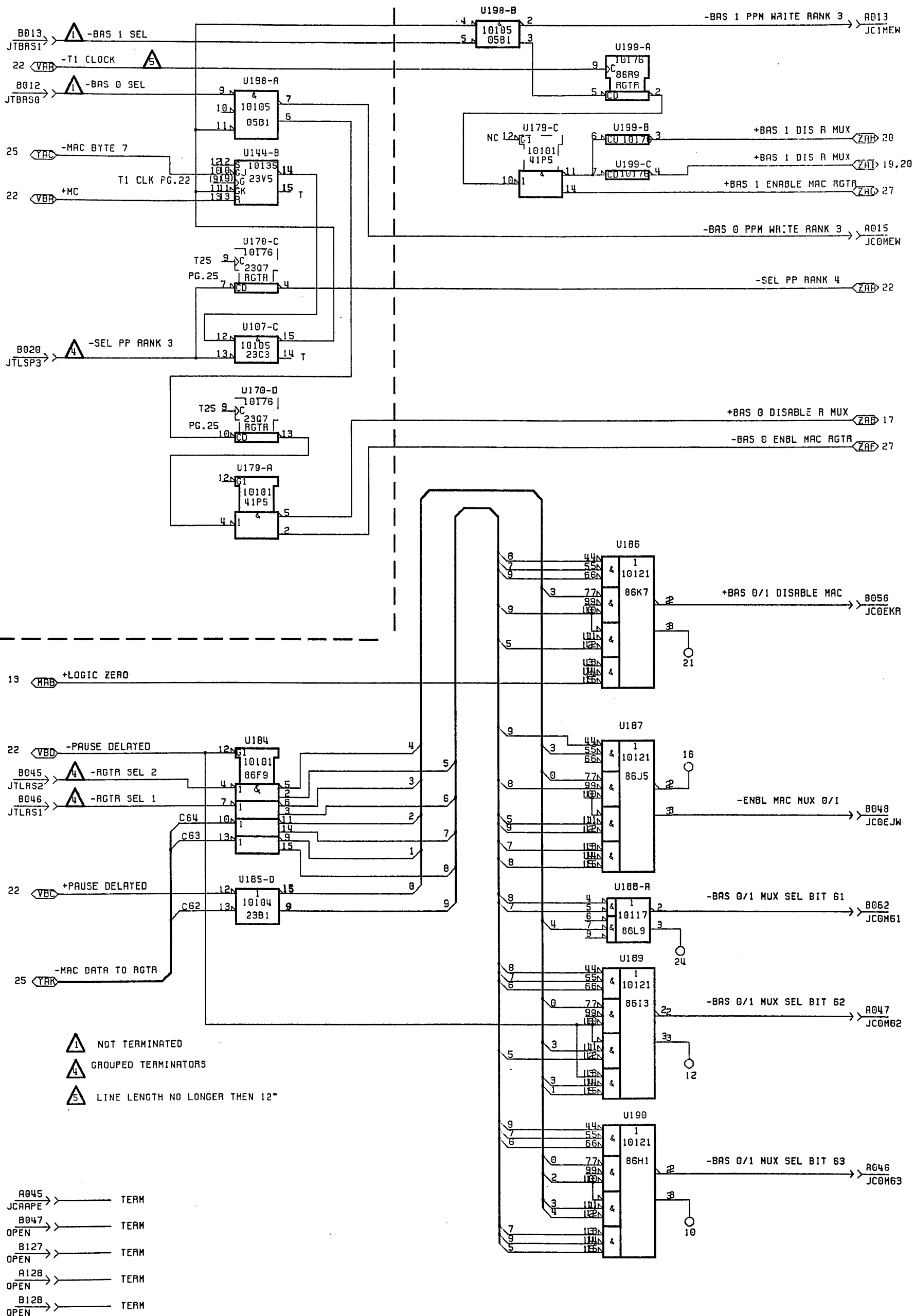



 CONTROL DATA	R+A BOARD		B	DWG NO.	DATE	REV
	OS BOUNDS MUX CONTROL, DATA MUX AND PP VECTOR CHECK			53575502	11/05/86	C
	TYPE 1JCH/1JUH					
			SHEET NO.	24	60462210	PAGE
			JC-24			



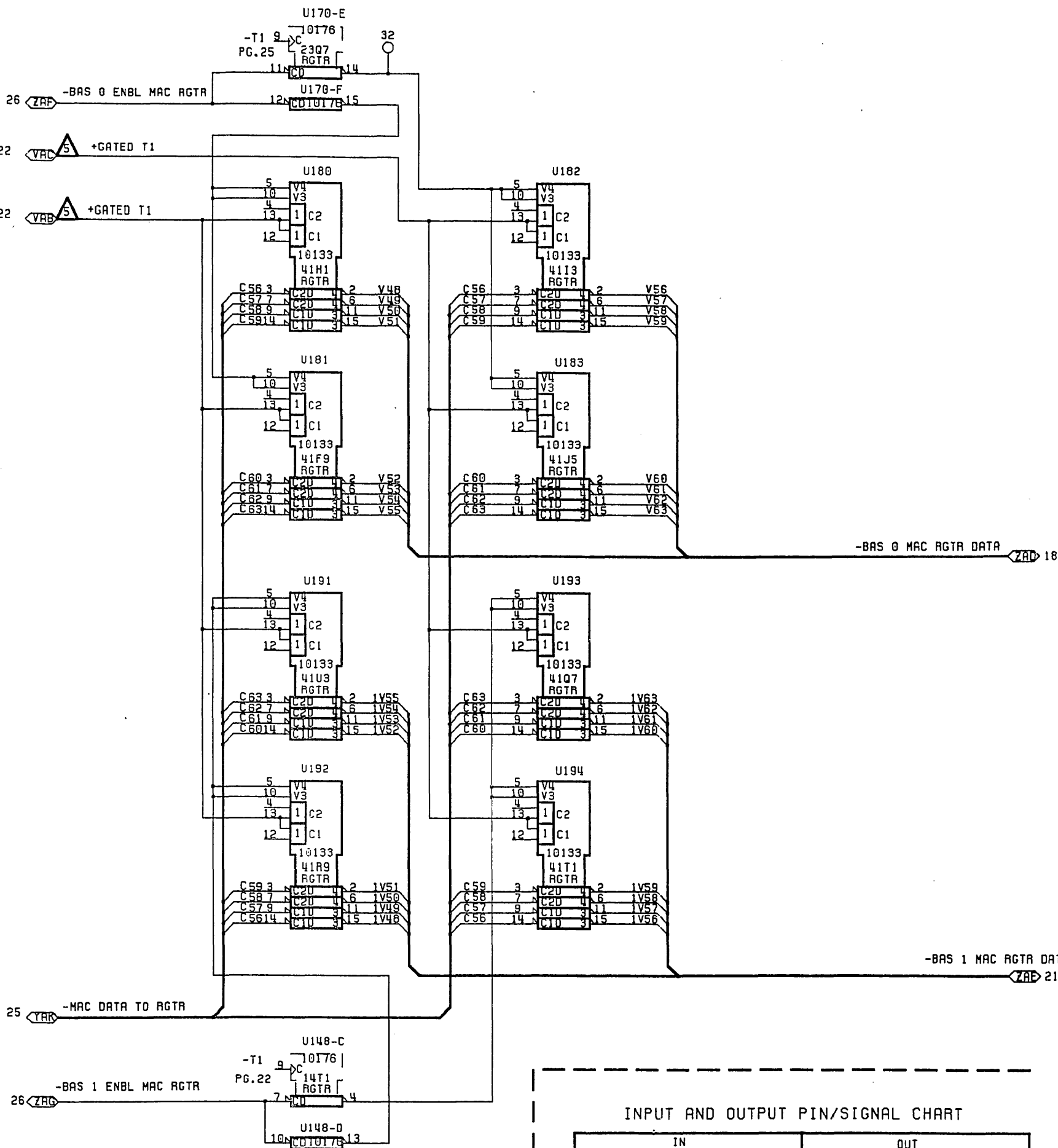
MAC CONTROL

JW AND KR PAK MAC CONTROL



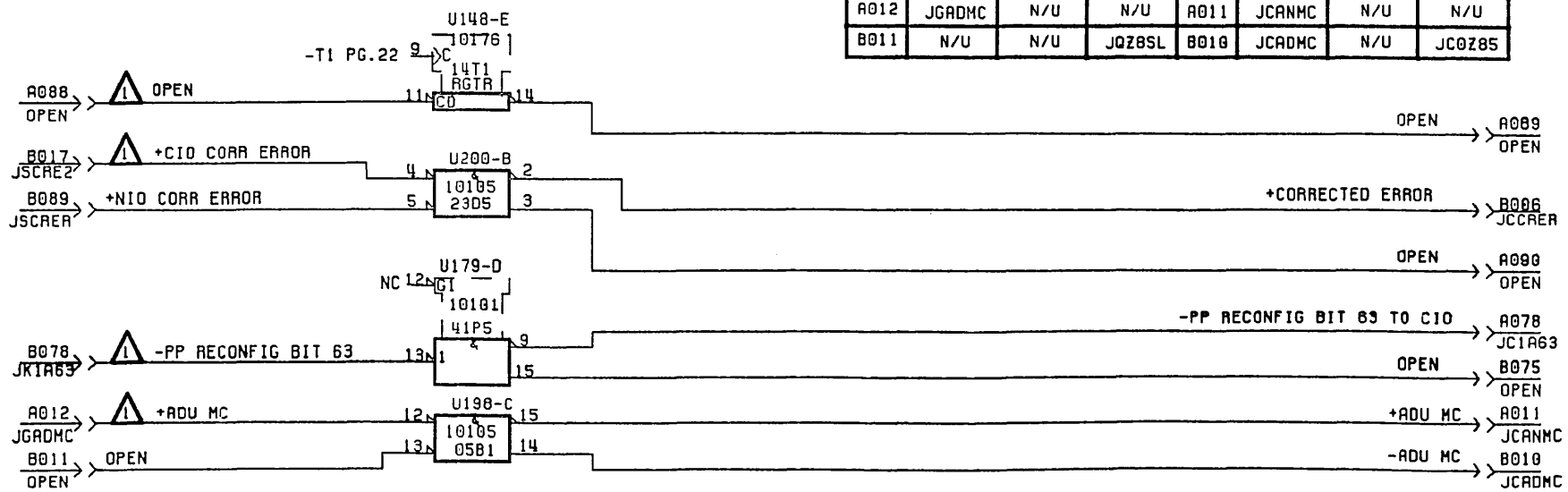
 CONTROL DATA	R+A BOARD MAC CONTROL AND JW & KR PAK MAC CONTROL TYPE 1JCH/1JUH	B	DWG NO. 53575502	DATE 11/05/86	REV C
			SHEET NO. 26	60462210	PAGE JC-26

MAC STORE RGTRS



INPUT AND OUTPUT PIN/SIGNAL CHART

IN				OUT			
PIN	A11	A10	A09	PIN	A11	A10	A09
A088	N/U	N/U	JQIUCE	A089	N/U	N/U	JCCLEA
B017	JSCRE2	N/U	N/U	B006	JCCRER	N/U	N/U
B089	JSCRER	N/U	N/U	A090	N/U	N/U	N/U
B078	JK1A63	N/U	JQADMC	A078	JC1A63	N/U	JCADMC
				B075	N/U	N/U	N/U
A012	JGADMC	N/U	N/U	A011	JCANMC	N/U	N/U
B011	N/U	N/U	JQZ8SL	B010	JCADMC	N/U	JC0Z8S



NOT TERMINATED

A LINE LENGTH NO LONGER THEN 12"



R+A BOARD
MAC STORE REGISTERS

TYPE 1JCH/1JUH

B	DWG NO. 53575
---	------------------


HEET NO. 27

DATE	REV
11/05/86	C

210 PAGE JC-27

TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	2	-BAS 0 R+A ENABLE	27		
02	25	-SERIAL DATA	28	2	-BAS 0 A BIT 63 RK4
03	2	-BAS 0 R BIT 57 RK4	29	23	-OS BDS ADRS P.E.
04	23	-SEL OSB BYTE 7	30	9	-BAS0 ADR ST CHIP SEL
05	15	+CM ADDRESS PE	31	9	-ADR STORE SEL BIT 2
06	23	-SEL OSB BYTE 0	32	27	+ENA MAC BAS 0
07	23	-SEL OSB BYTE 5	33	12	-BAS1 ADR ST CHIP SEL
08	17	-ENBL R+A TO MEM	34	12	-ADD STORE SEL BIT 1
09	23	-SEL OSB BYTE 1	35	9	-ADD STORE SEL BIT 0
10	26	+MUX SEL BIT 63	36	17	-BAS 1 R UPPER SEL
11	23	-SEL OSB BYTE 6	37	13	-BAS 1 CM ADR 38 RK0
12	26	+MUX SEL BIT 62	38	24	+ENABLE OS BDS MUX
13	22	-PAUSE	39	22	+LOAD ENABLE
14	4	-BAS0 RNK0 LW R BT56	40	22	-LOAD
15	4	-BAS0 RNK0 UP R BT44	41		
16	26	+ENA CP MAC MUX	42	25	-MAC READ
17	17	-BAS 0 R UPPER SEL	43		
18	10	-BAS0 CM ADRS 55 RK0	44		
19	13	+BAS1 OS BDS ERR RK0	45		
20	10	+BAS0 OS BDS ERR RK0	46		
21	26	+ENBL MAC MUX	47	7	-BAS 1 RK0 LW R BT47
22	22	+ERR DATA TO Y BAS 1	48	5	-BAS 1 R+A ENABLE
23	19	+BAS 0 ERR DATA TO Y	49	5	-BAS 1 A BIT 47 RK4
24	26	+MUX SEL BIT 61	50	22	+T1 CLOCK
25	15	-CM ADRS BIT 48	51	5	-BAS1 R BIT 36 RK4
26					

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [NOT USED]
TERM	A045,B047,B127,A128,B128
UNUSED	A061,B070,A074,B120

 CONTROL DATA	R+A BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JCH/1JUH		B	DWG NO. 53575502	DATE 11/05/86	REV C
	N			SHEET NO. 28	60462210	PAGE
						JC-28

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.


R + A BOARD

[illegible]

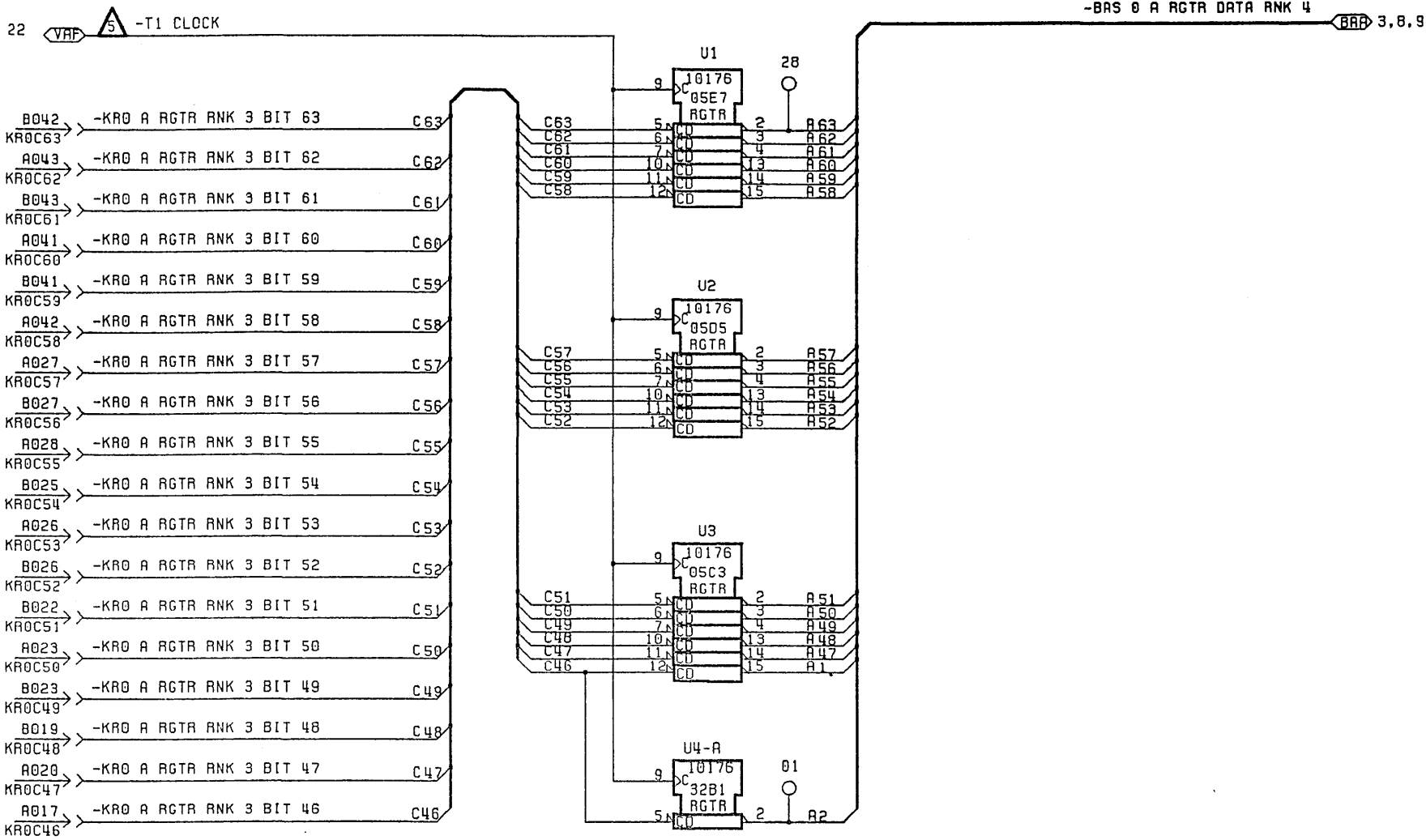
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

DWN	L H JOHNSON	02/21/86
CHKD	D R FORD	03/26/86
ENG	D R FORD	03/26/86
PUBS	R K BONDE	03/26/86
APP	D R FORD	03/26/86

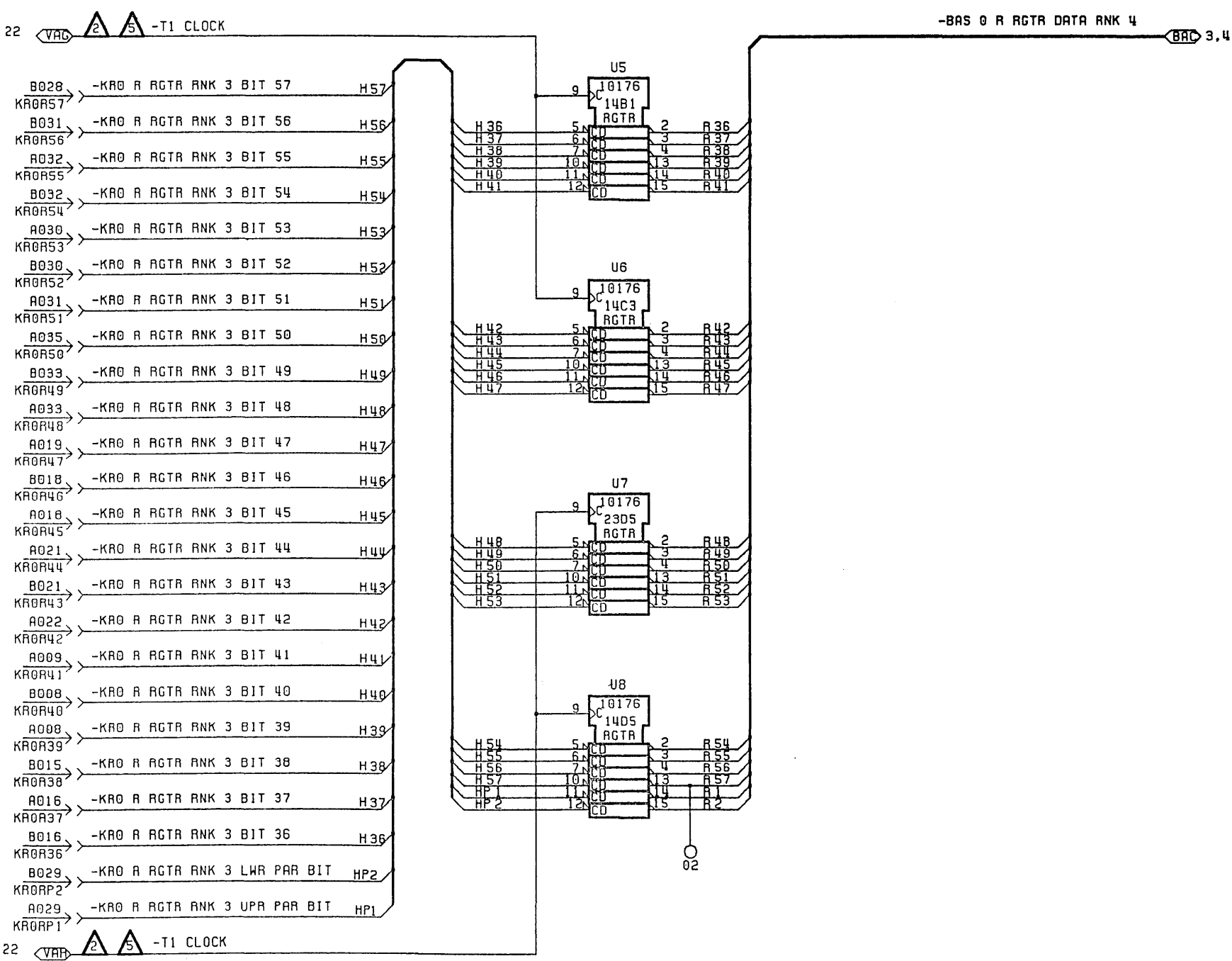
LOC: A11, A10, A09

 CONTROL DATA	REVISION HISTORY		B	DWG NO. 22105671	DATE 06/15/88	REV D
	TYPE 1JCH/1JUH _____ N		SHEET NO. 1	60462210	PAGE	JC-01

BAS 0 A RGTR RNK 4



BAS 0 R RGTR RNK 4

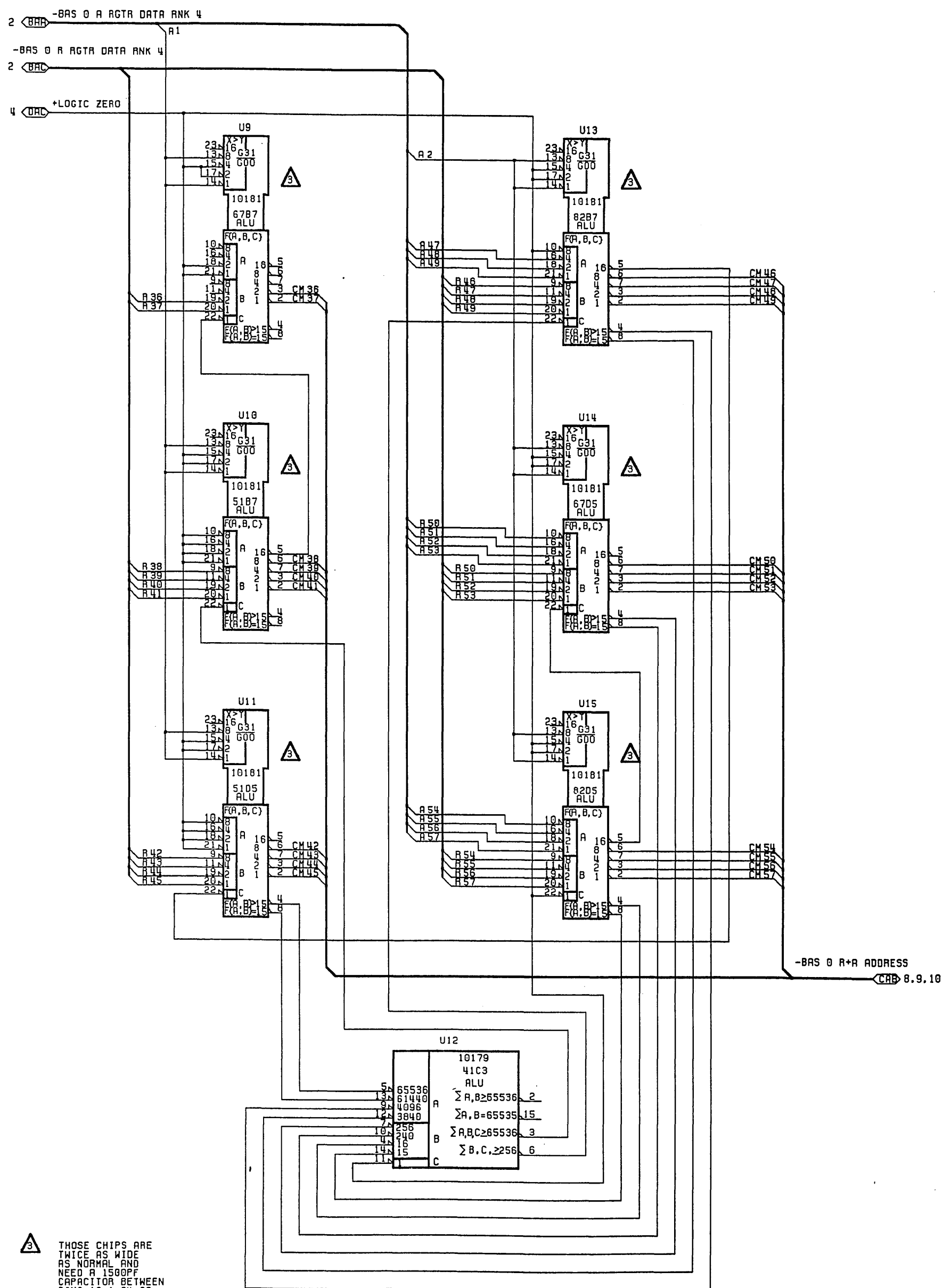


ROUTE CLOCK LINE TO THESE CHIPS LAST

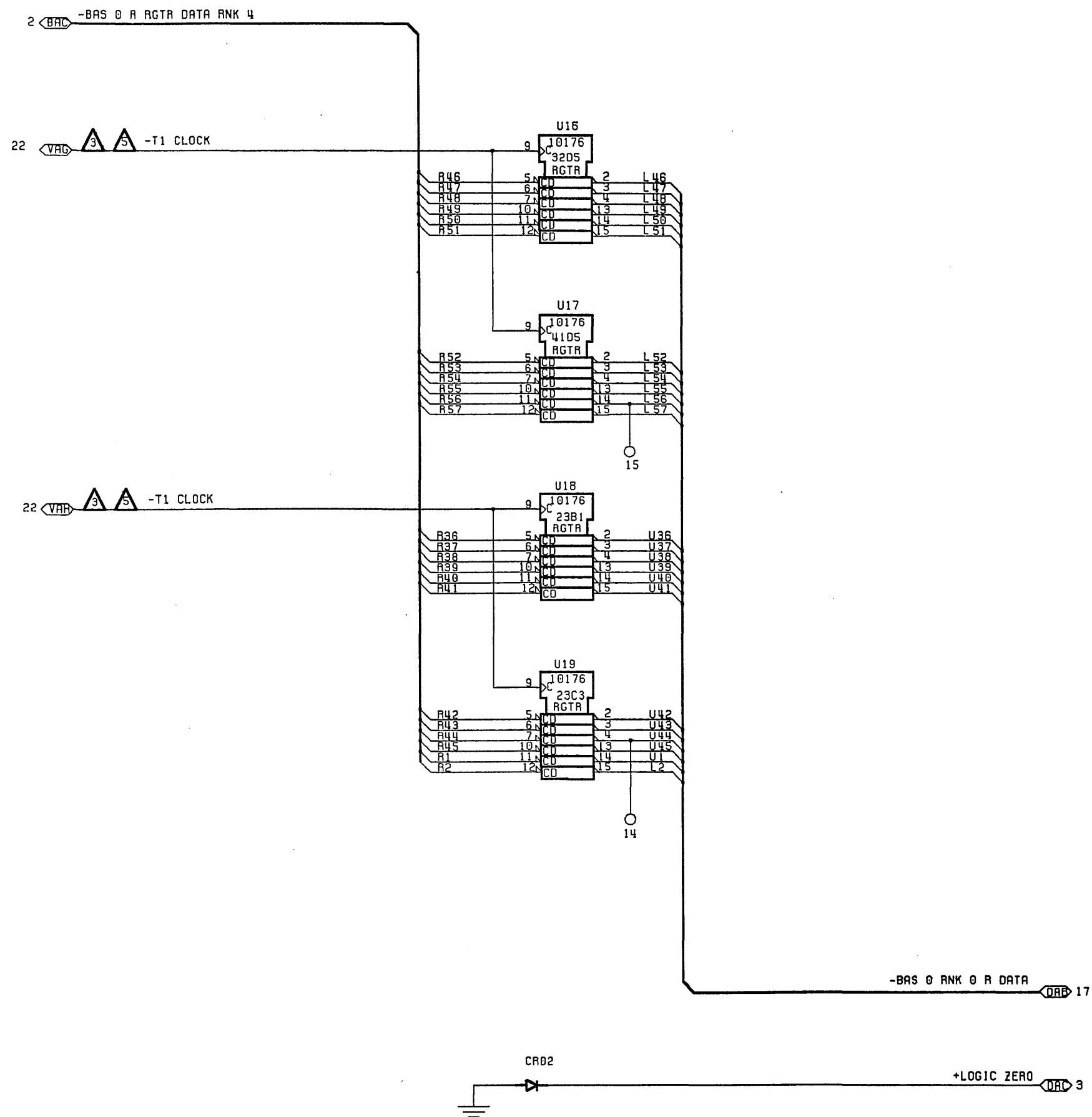
TOTAL LINE LENGTH NO LONGER THEN 12 INCHES

	R+A BOARD BARREL 0 A AND R REGISTERS, RNK 4 TYPE 1JCH/1JUH	8	OWG NO.	DATE	REV
			22105671	02/21/86	A
			SHEET NO. 2	60462210	PAGE JC-02

BAS 0 R+A ADRS



BAS 0 R RGTR RNK 0

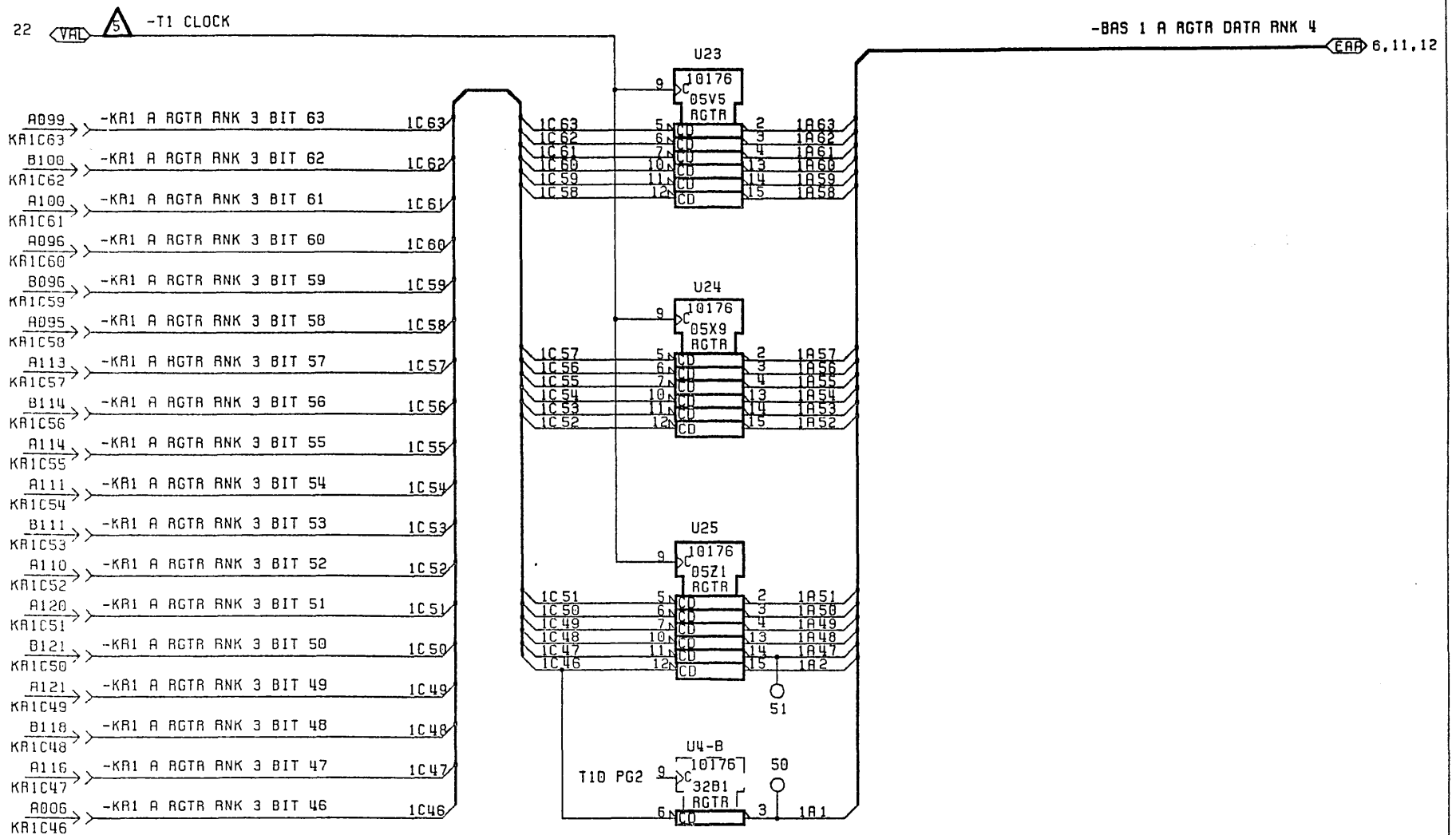


CD	R UPPER BITS
2	R36 - R50
1	R36 - R45

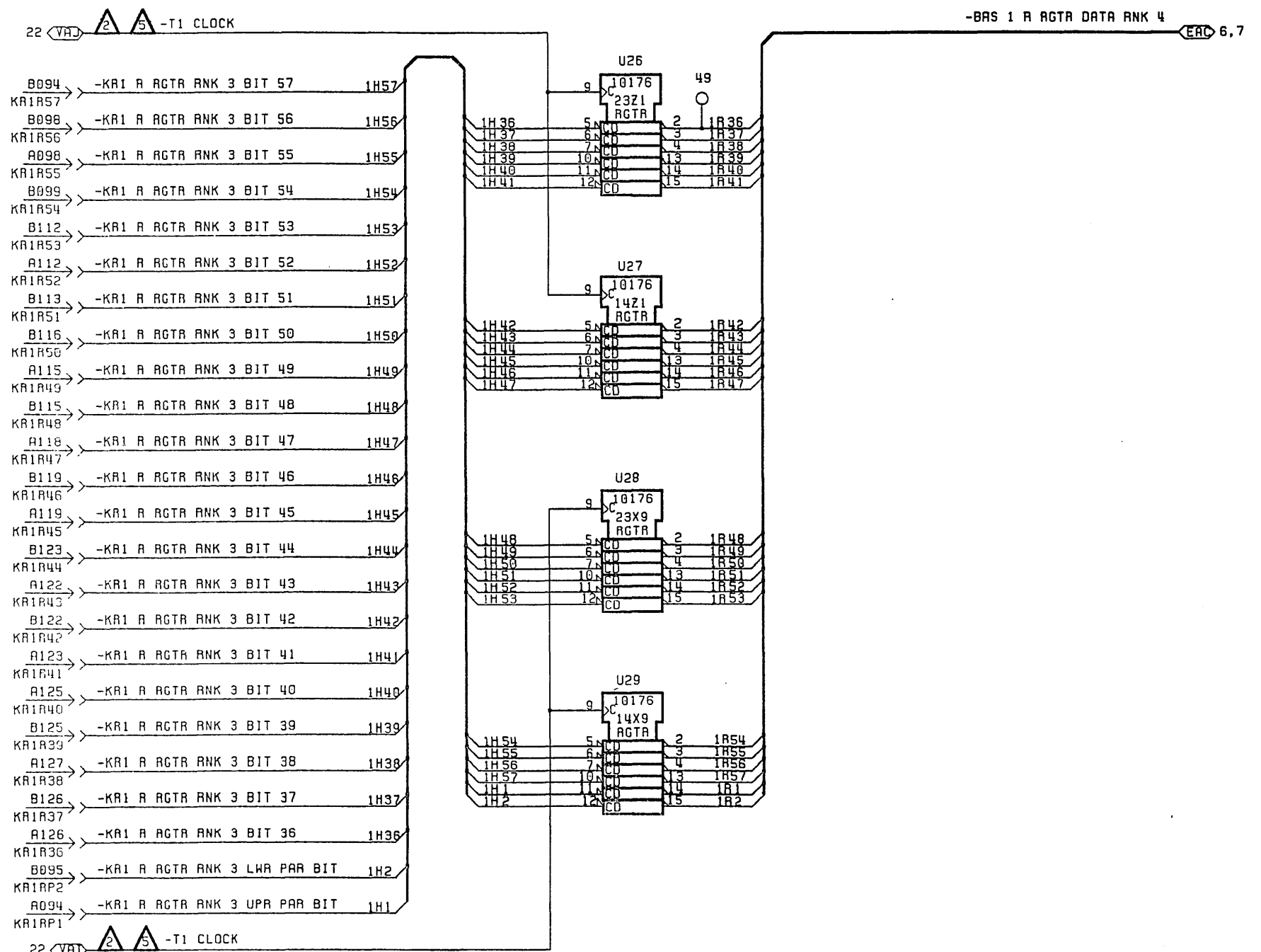
- 3 ROUTE CLOCK LINE TO THESE CHIPS FIRST
- 5 TOTAL LINE LENGTH NO LONGER THEN 12"

CONTROL DATA	R+A BOARD BARREL 0, R REGISTER RNK 0 TYPE 1JCH/1JUH	8	DWG NO. 22105671	DATE 02/21/86	REV A
			SHEET NO. 4	60462210	PAGE JC-04

BAS 1 A RGTR RNK 4




BAS 1 R RGTR RNK 4

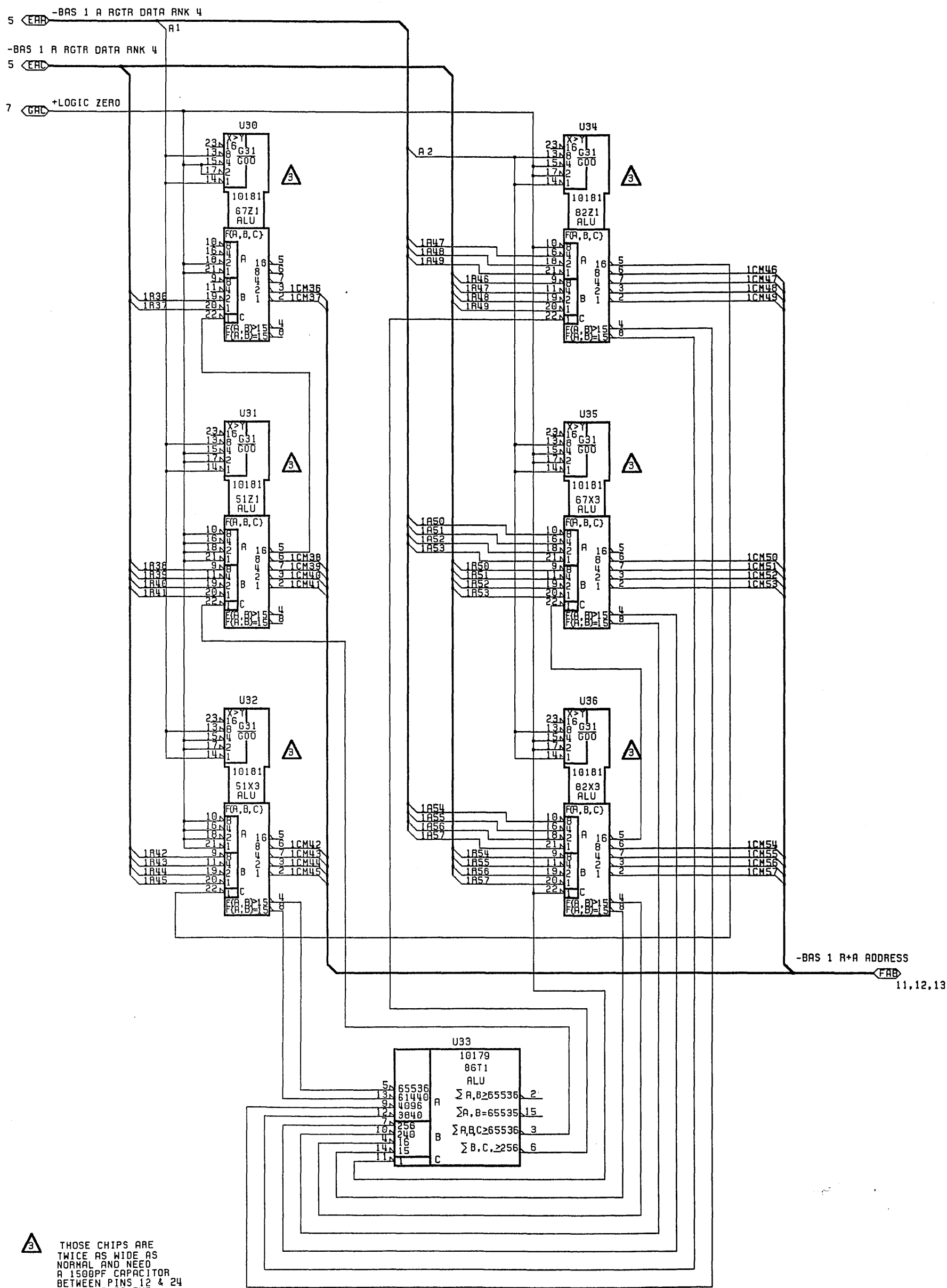


2 ROUTE CLOCK TO THESE LOCATIONS LAST

5 TOTAL LENGTH NO LONGER THEN 12"

 CONTROL DATA	A+A BOARD BARREL 1 A AGTA AND A AGTA ANK 4 TYPE 1JCH/1JUH	B	DWG NO. 22105671	DATE 02/21/86	REV A
			SHEET NO. 5	60462210	PAGE JC-05

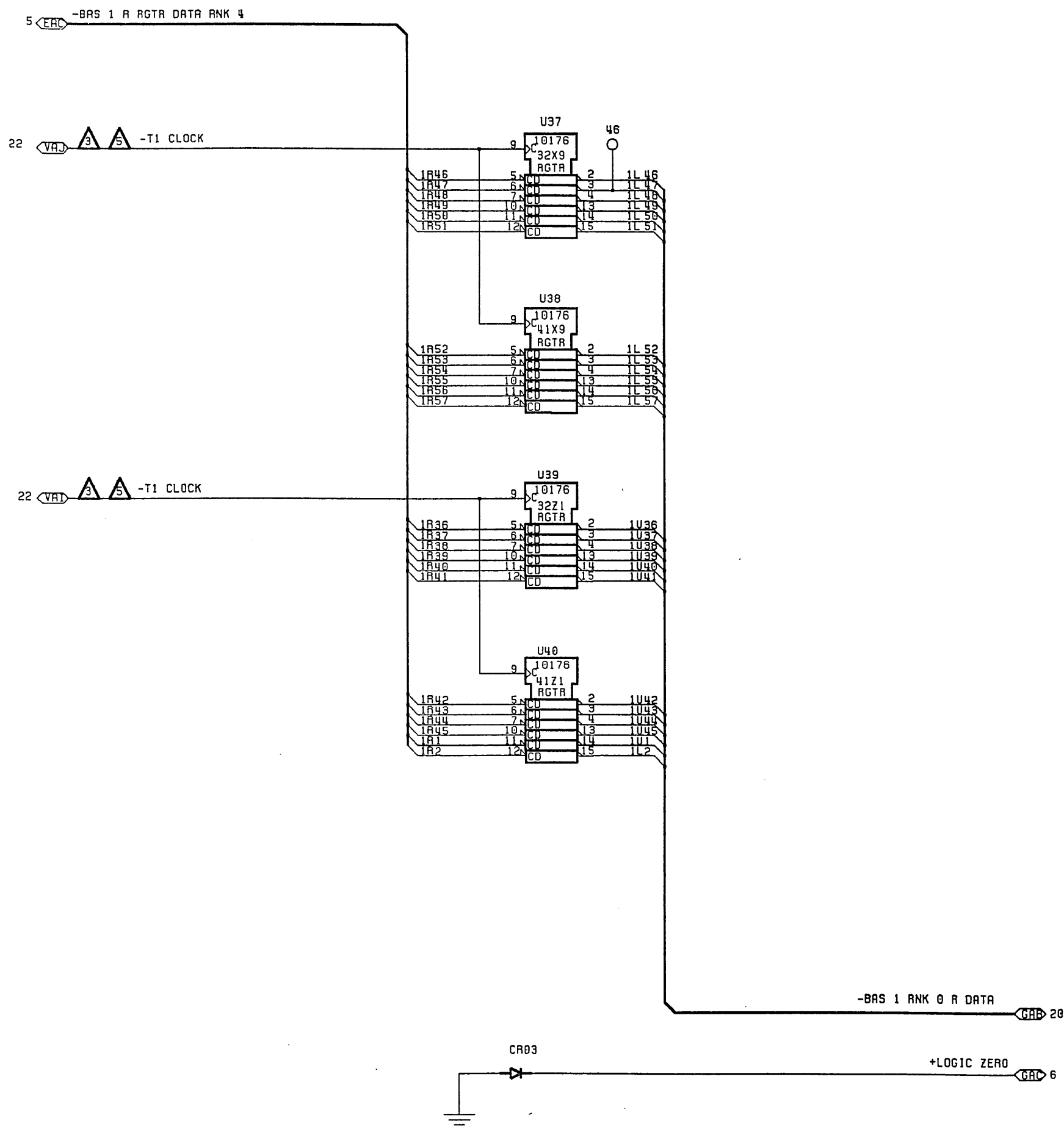
BAS 1 R+A ADRS



R+A BOARD
BARREL 1 R+A ADDRESS
TYPE 1JCH/1JUH


8	DWG NO. 22105671	DATE 02/21/86	REV A
N	SHEET NO. 6	60462210	PAGE JC-06

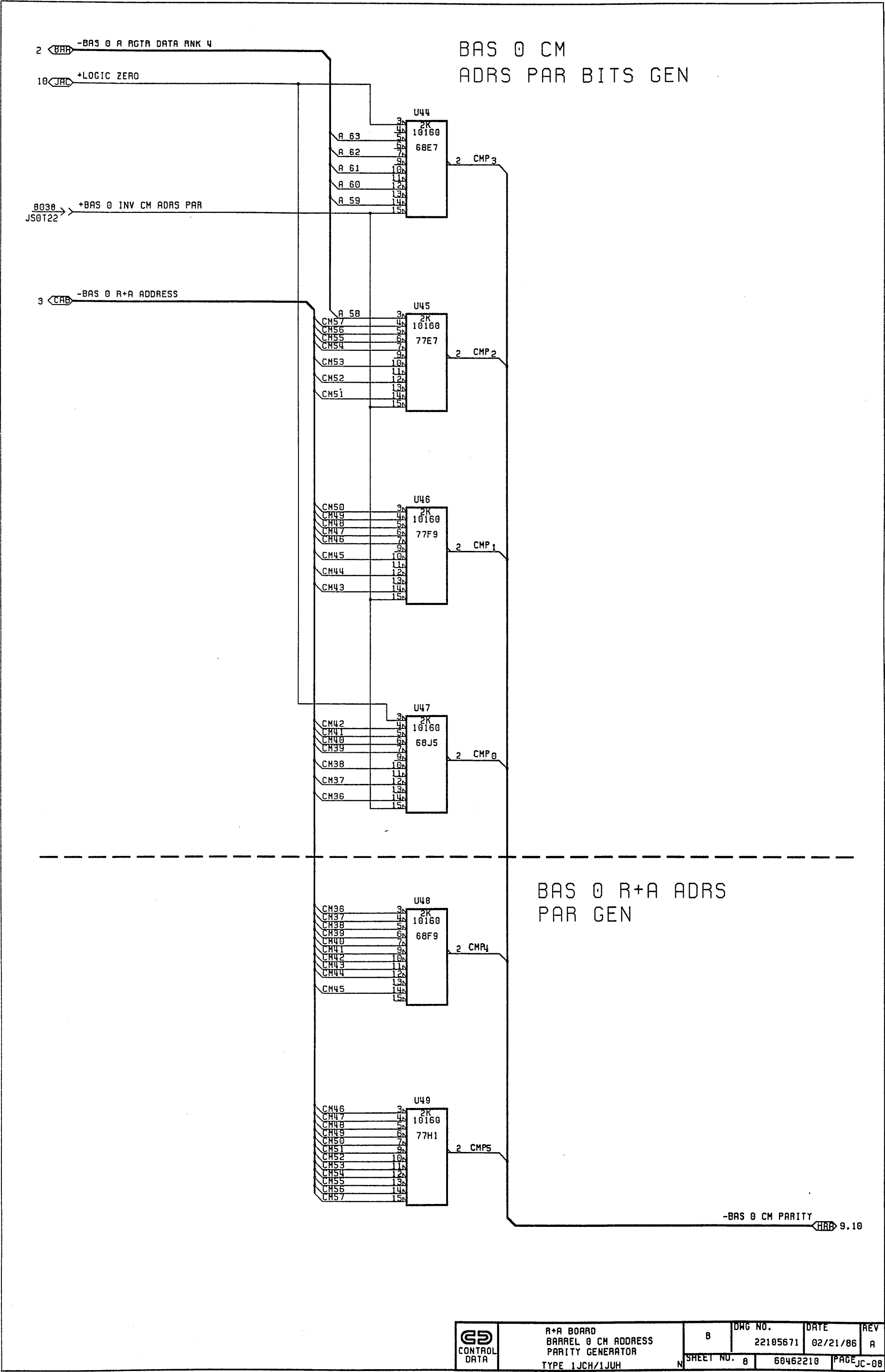
BAS 1 R RGTR RNK 0

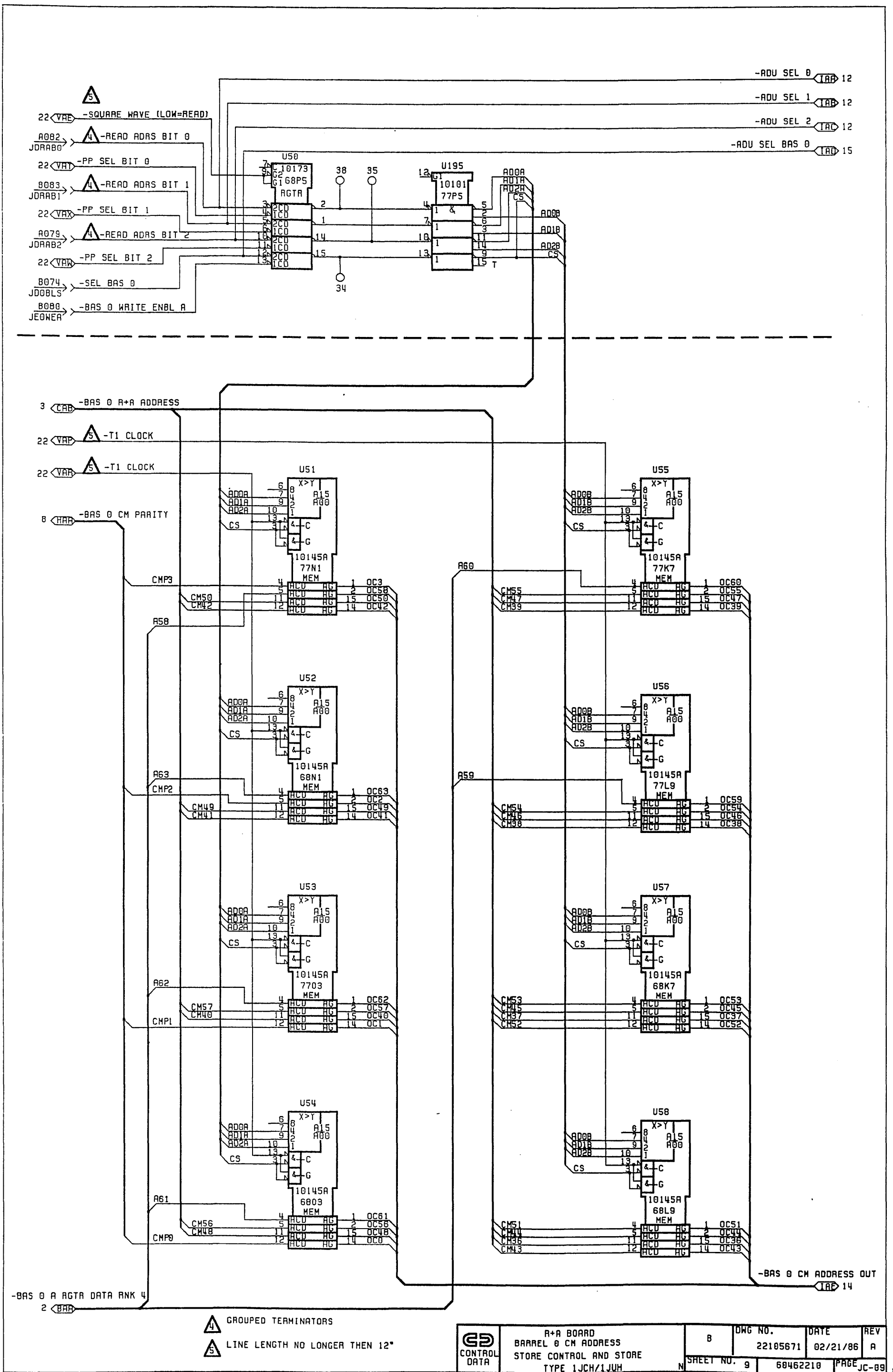


CD	R UPPER BITS
2	R36 - R50
1	R36 - R45

- △ ROUTE CLOCK TO THESE LOCATIONS FIRST
- △ THESE LINES ARE NO LONGER THEN 12 "

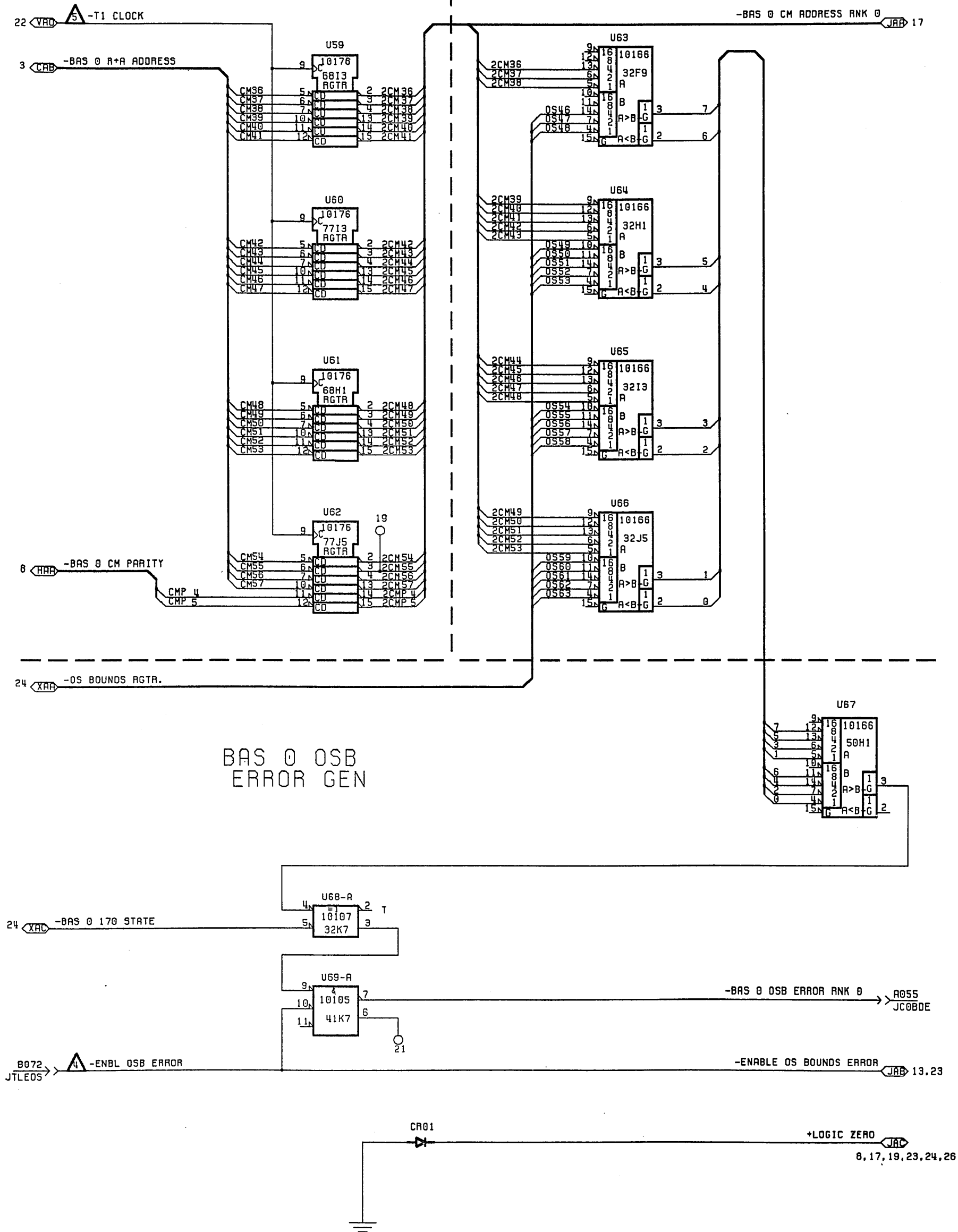
 CONTROL DATA	A+A BOARD	B	DWG NO.	DATE	REV
	BARREL 1, A REGISTER RNK 0		22105671	02/21/86	A
	TYPE 1JCH/1JUH	N	SHEET NO. 7	60462210	PAGE JC-07





BAS 0 CM ADRS RNK 0


BAS 0 OSB ERROR CHECKER



BAS 0 OSB
ERROR GEN

\triangle GROUPED TERMINATORS

\triangle LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R-A BOARD BAS 0 CM ADDRESS RNK 0 AND OS BOUNDS CHECK AND ERROR GEN TYPE 1JCH/1JUH		B	DWG NO. 22105671	DATE 02/21/86	REV A
	SHEET NO. 18		60462210		PAGE JC-10	
	N					

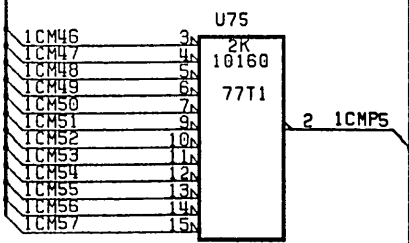
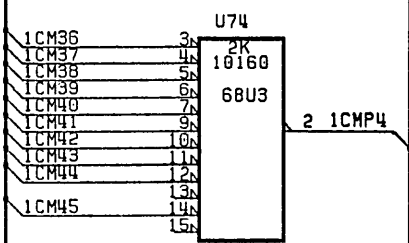
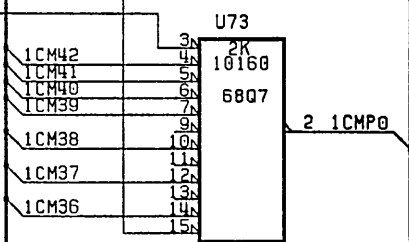
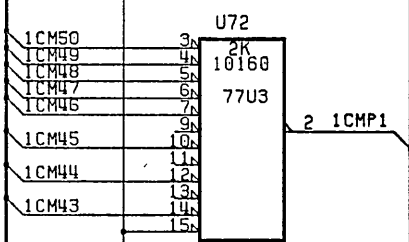
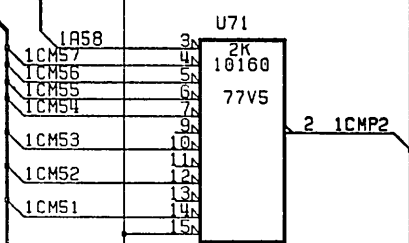
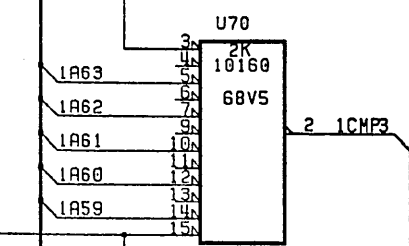
5 -BAS 1 A RCTA DATA ANK 4

13 +LOGIC ZERO

A093 JS1T22 → +BAS 1 INV CM ADRS PAR

6 -BAS 1 R+A ADDRESS

BAS 1 CM ADRS
PAR BITS GEN



-BAS 1 CM PARITY 12.13

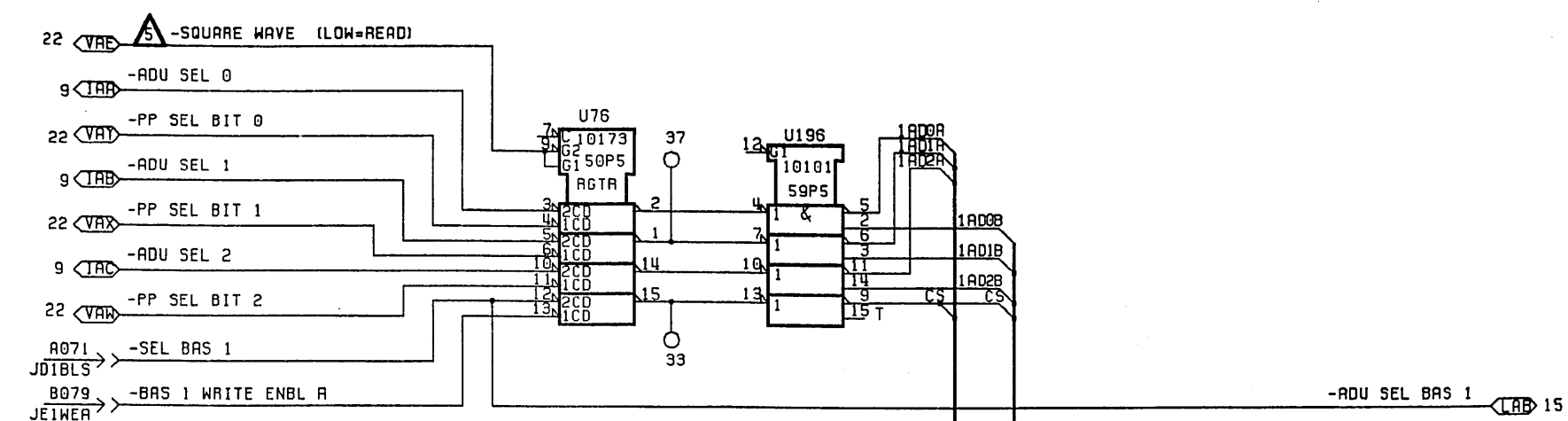
BAS 1 R+A ADRS
PAR GEN



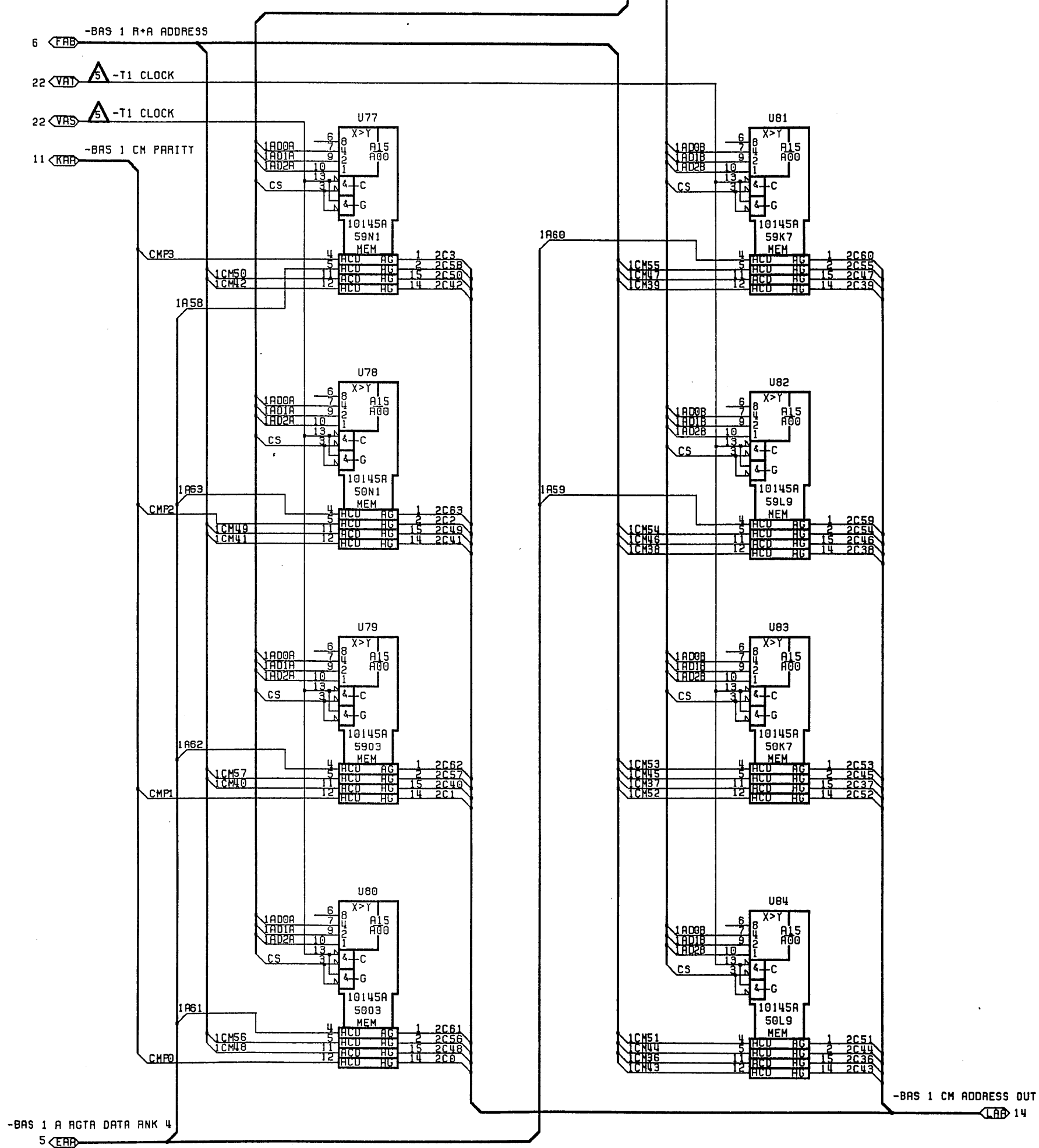
R+A BOARD
BARREL 1 CM ADDRESS
PARITY GENERATOR
TYPE 1JCH/1JUH

B	DWG NO. 22105671	DATE 02/21/86	REV A
SHEET NO. 11		60462210	PAGE JC-11


BAS 1 CM ADRS STORE CONTROL



BAS 1 CM ADRS STORE RAMS

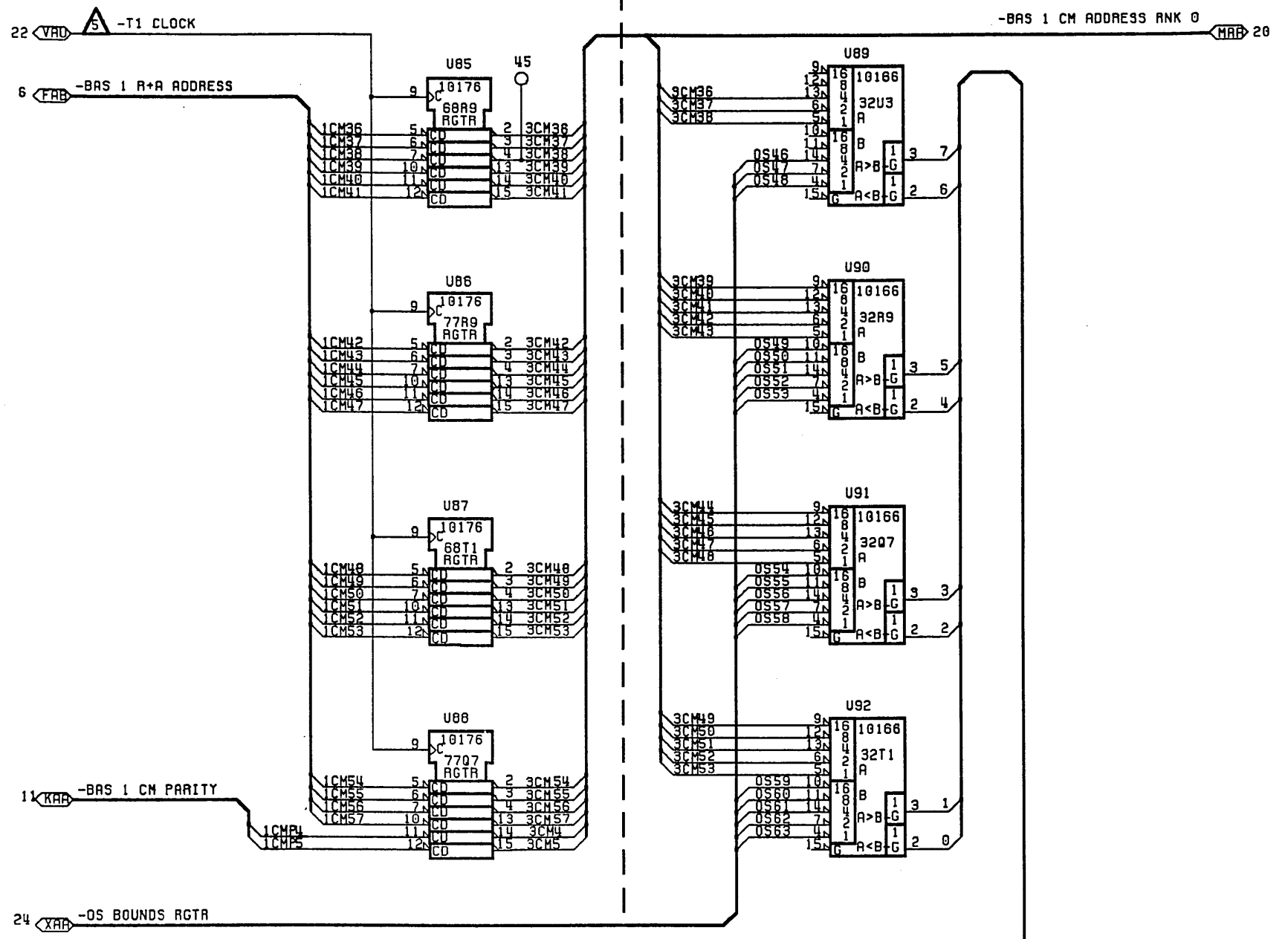


5 LINE LENGTH NO LONGER THEN 12"

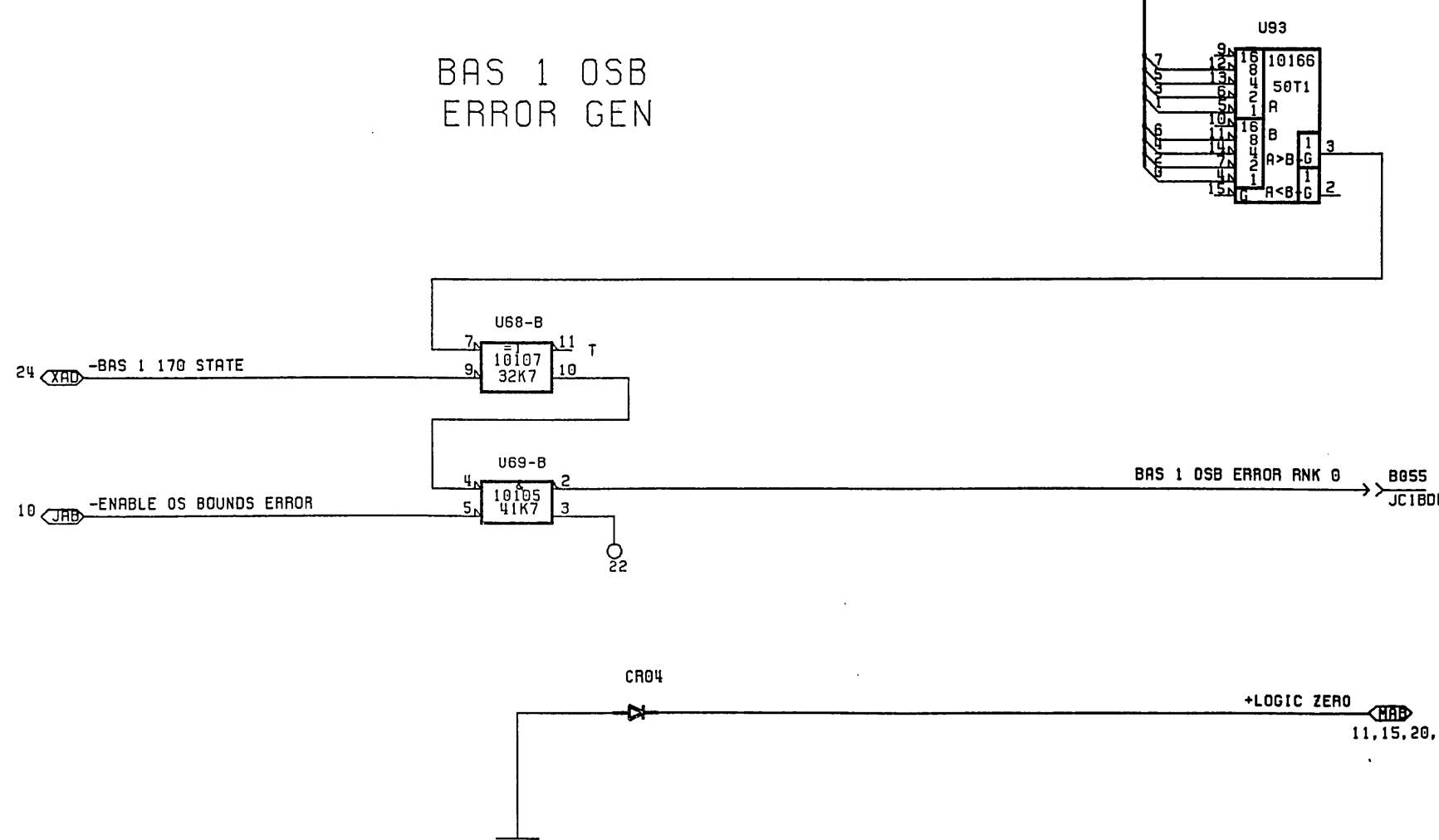
 CONTROL DATA	A+A BOARD BARREL 1 CM ADDRESS STORE CONTROL AND STORE TYPE 1JCH/1JUH	B	DWG NO. 22105671	DATE 02/21/86	REV A
		SHEET NO. 12	60462210	PAGE	JC-12

BAS 1 CM ADRS RNK 0


BAS 1 OSB ERROR CHECKER



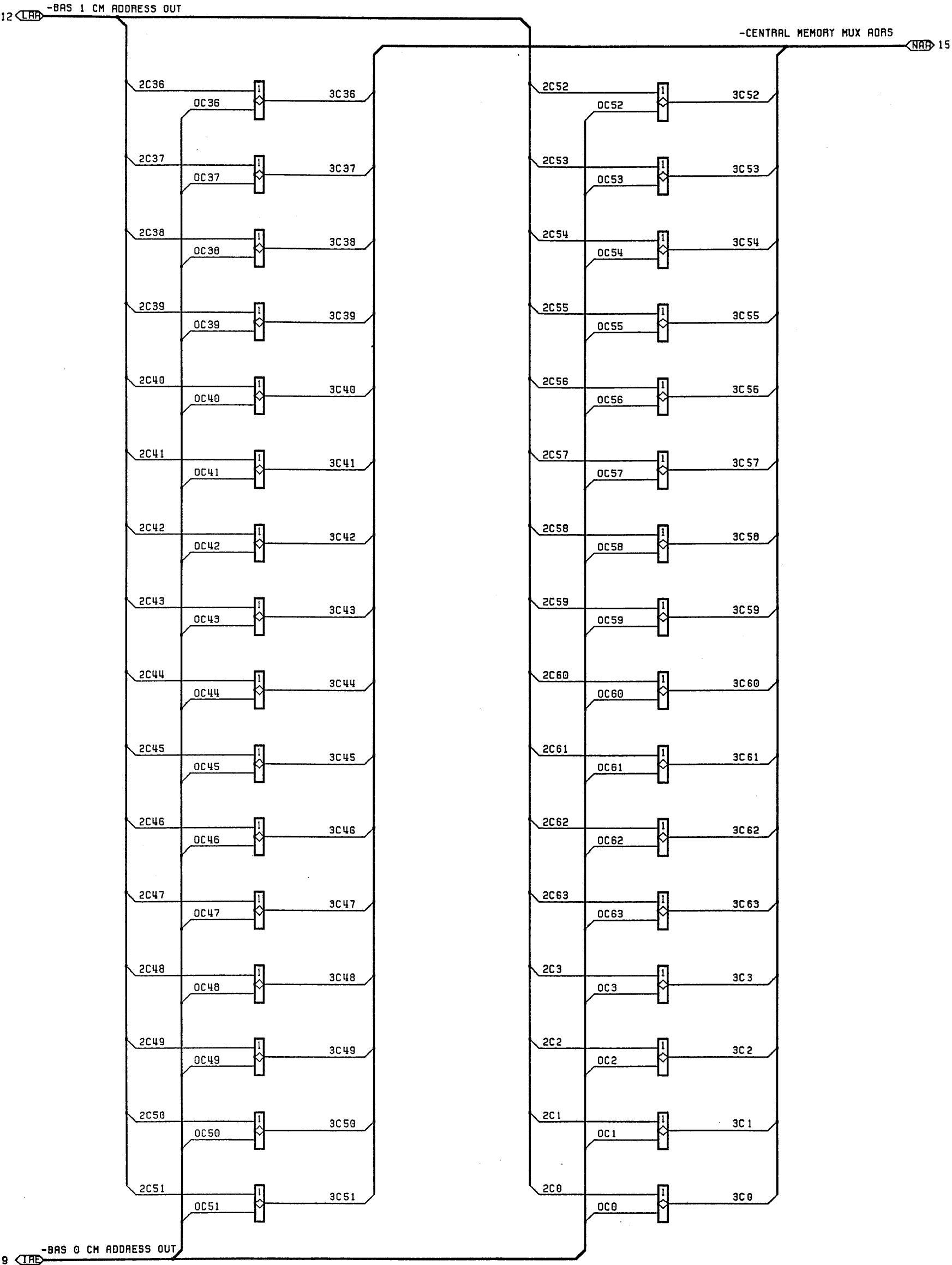
BAS 1 OSB
ERROR GEN




LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R+A BOARD BARREL 1 CM ADDRESS RNK 0 AND OS BOUNDS CHECK AND ERROR GEN TYPE 1JCH/1JUH				B	DWG NO. 22105671		DATE 02/21/86		REV A		
						SHEET NO. 13		60462210			PAGE	
											JC-13	

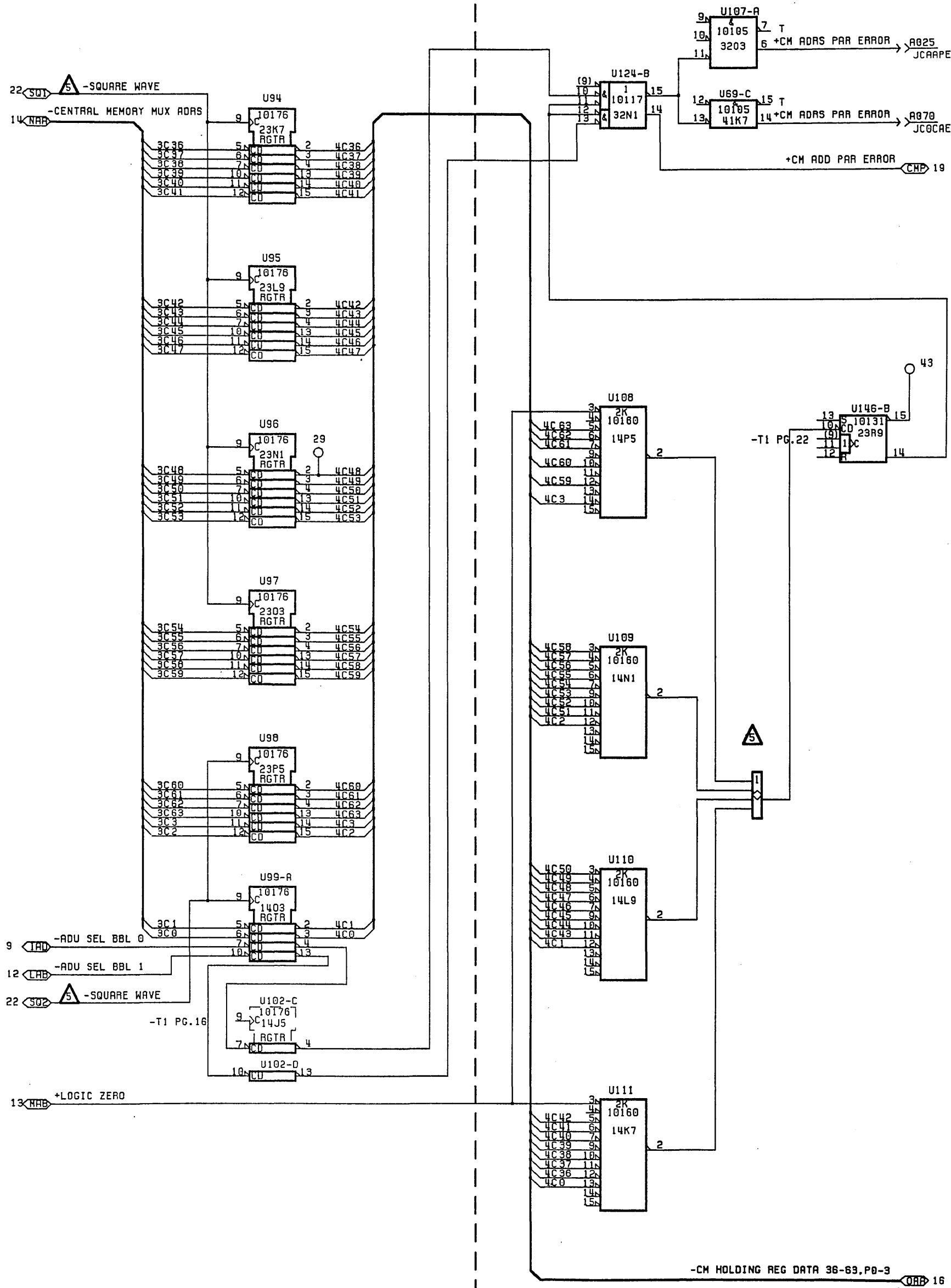
CM ADRS MUX




 CONTROL DATA	A+A BOARD CENTRAL MEMORY ADDRESS OUTPUT DATA MUX TYPE 1JCH/1JUH		B	DWG NO. 22105671	DATE 02/21/86	REV A
	N			SHEET NO. 14	60462210	PAGE JC-14

CM ADRS HLDG RGTR

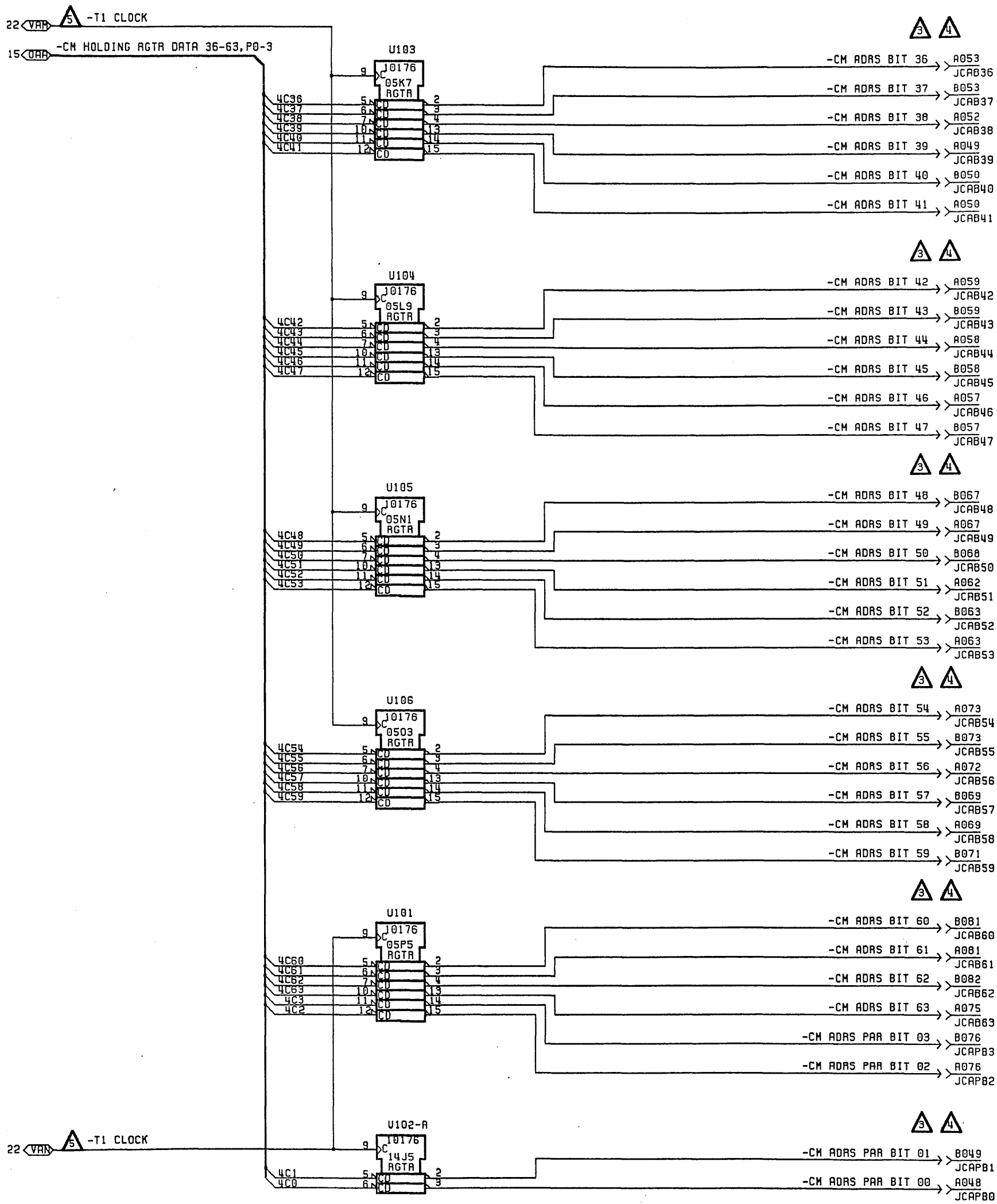
CM ADRS OUT PAR CHECK




△ LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R+A BOARD CM ADDRESS HOLDING REGISTER AND OUTPUT PARITY CHECK TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV	
			22105671	02/21/86	A	
		SHEET NO.	15	60462210	PAGE	JC-15

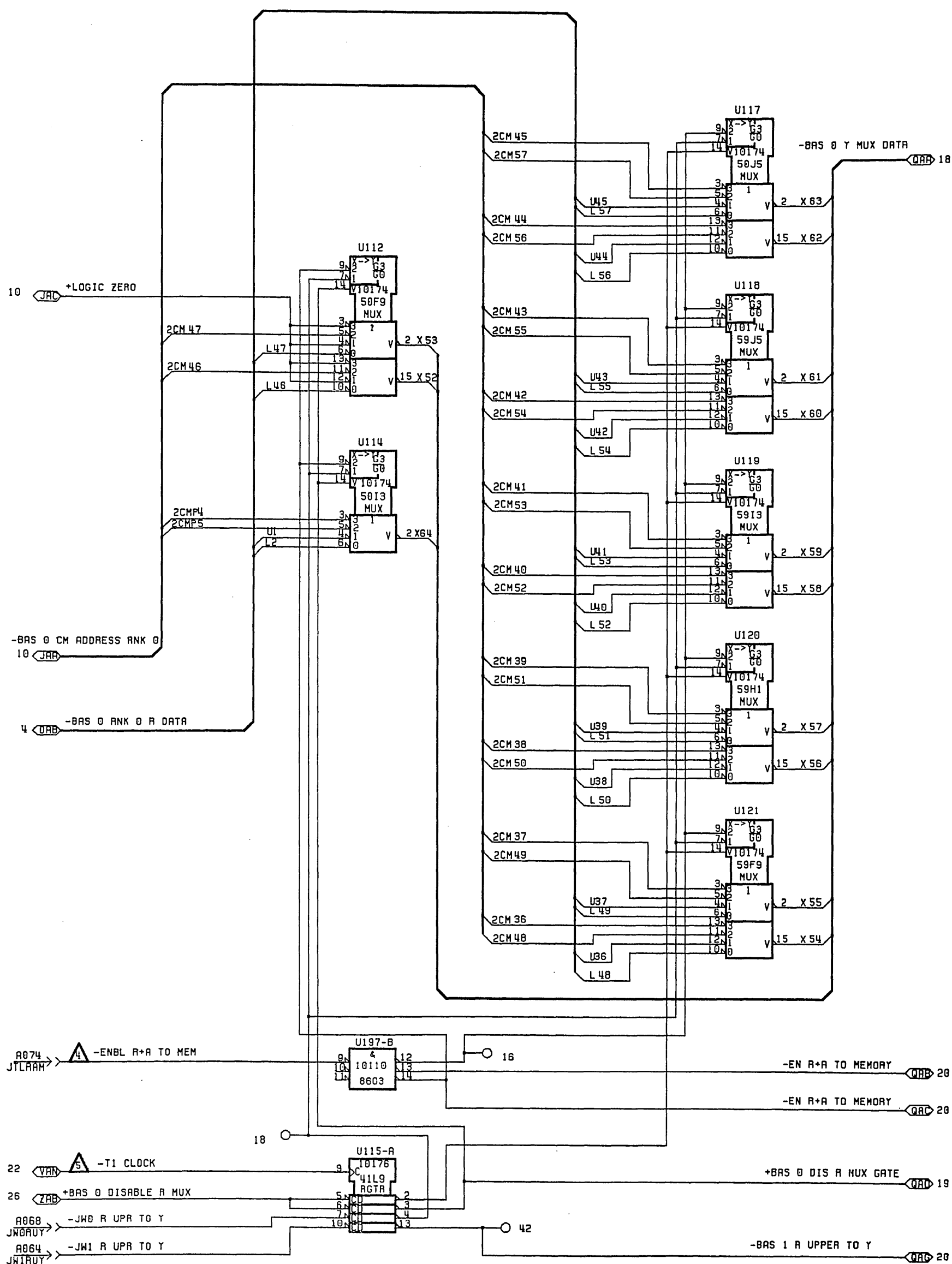
CM ADRS REALIGNMENT RGTR



- △ THESE OUTPUT PINS TERMINATED ON THIS BOARD
- △ GROUPED TERMINATORS
- △ LINE LENGTH NO LONGER THEN 12"

 CONTROL DATA	R+A BOARD CM ADDRESS REALIGNMENT RGTR AND OUTPUT		B	DWG NO. 22105671	DATE 02/21/86	REV A
	TYPE 1JCH/1JUH			SHEET NO. 16	60462210	PAGE JC-16

BAS 0 R TO Y MUX



CD	MUX SELECT
0	R LOWER
1	R UPPER
2	R+A LOWER
3	R+A UPPER

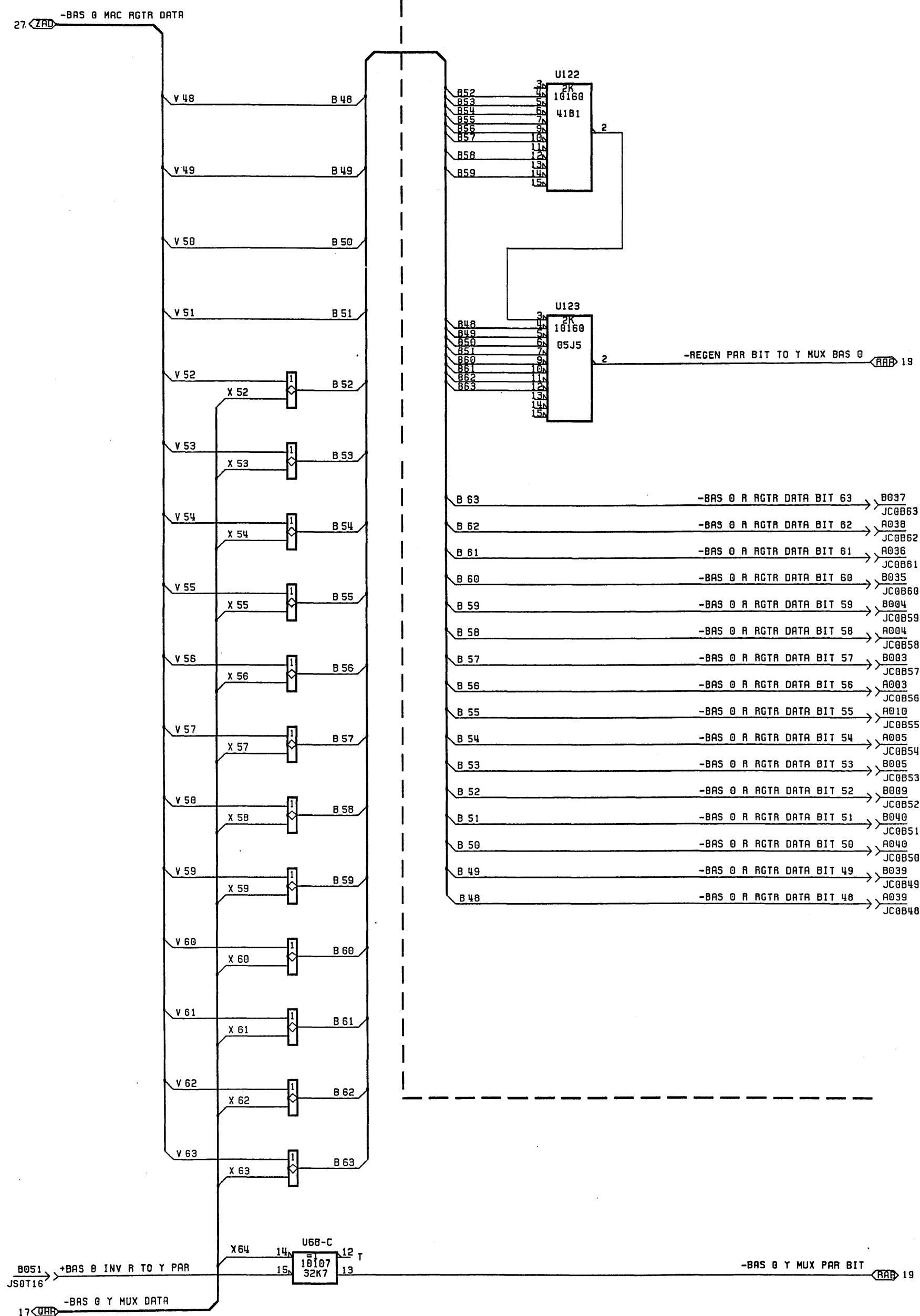
GROUPED TERMINATORS

LINE LENGTH NO LONGER THEN 12"

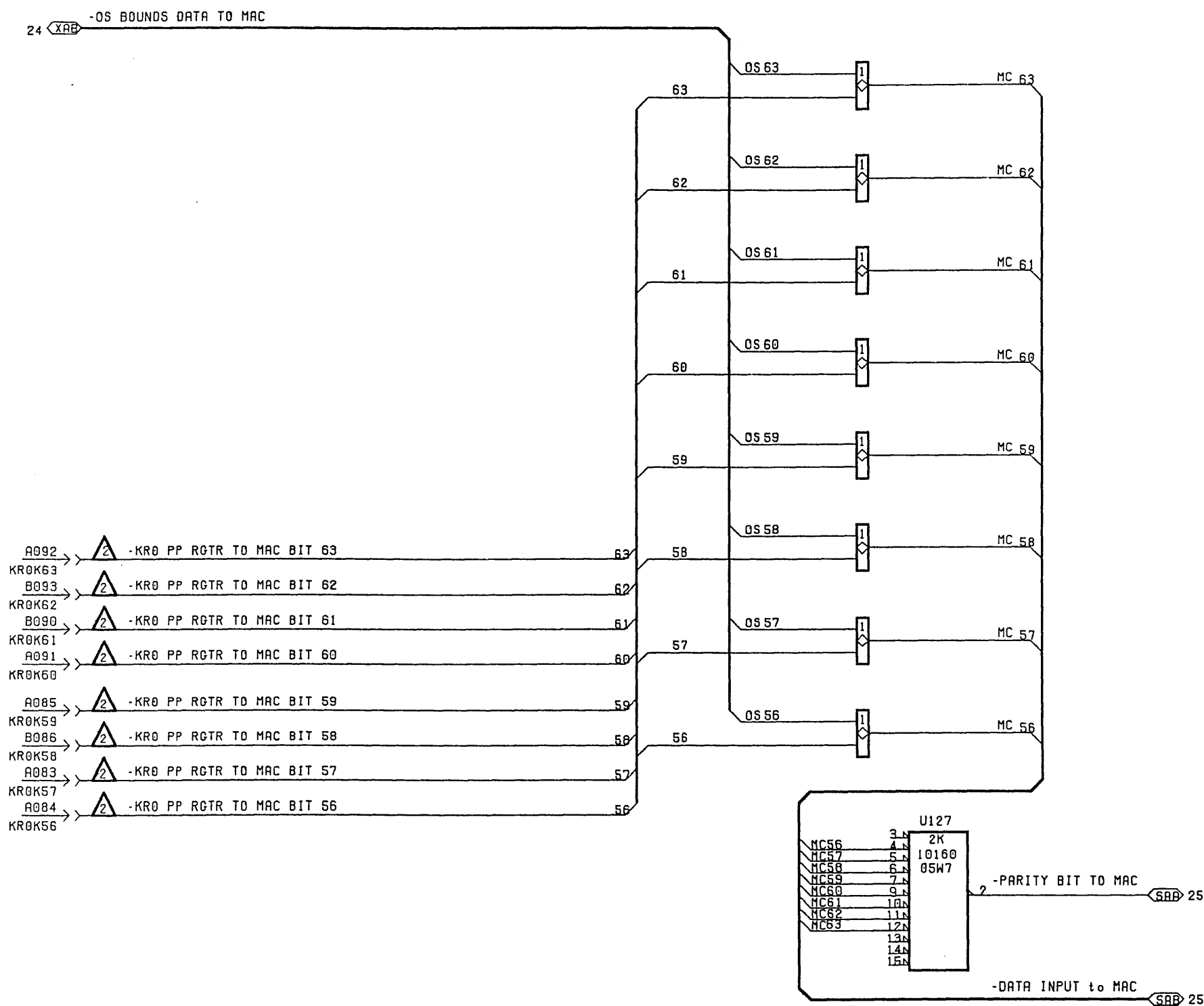
 CONTROL DATA	R+A BOARD BARREL 0 R TO Y MUX		B	DWG NO.	DATE	REV
	TYPE 1JCH/1JUH			22105671	02/21/86	A
	N		SHEET NO. 17	60462210	PAGE	JC-17

BAS 0 R TO Y DATA MUX

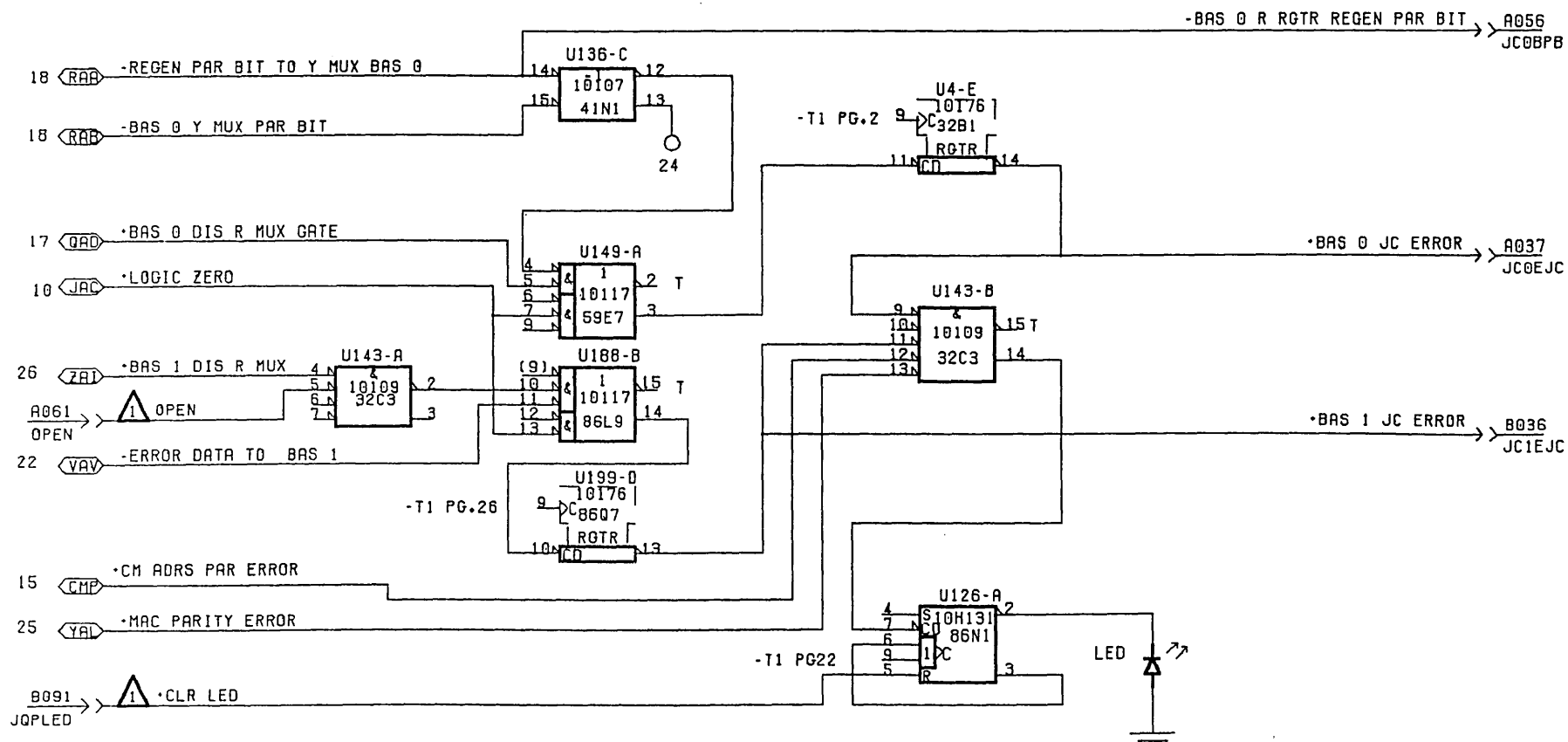
BAS 0 R TO Y DATA OUT



DATA TO MAC MUX



BOARD ERROR GEN



1 NOT TERMINATED

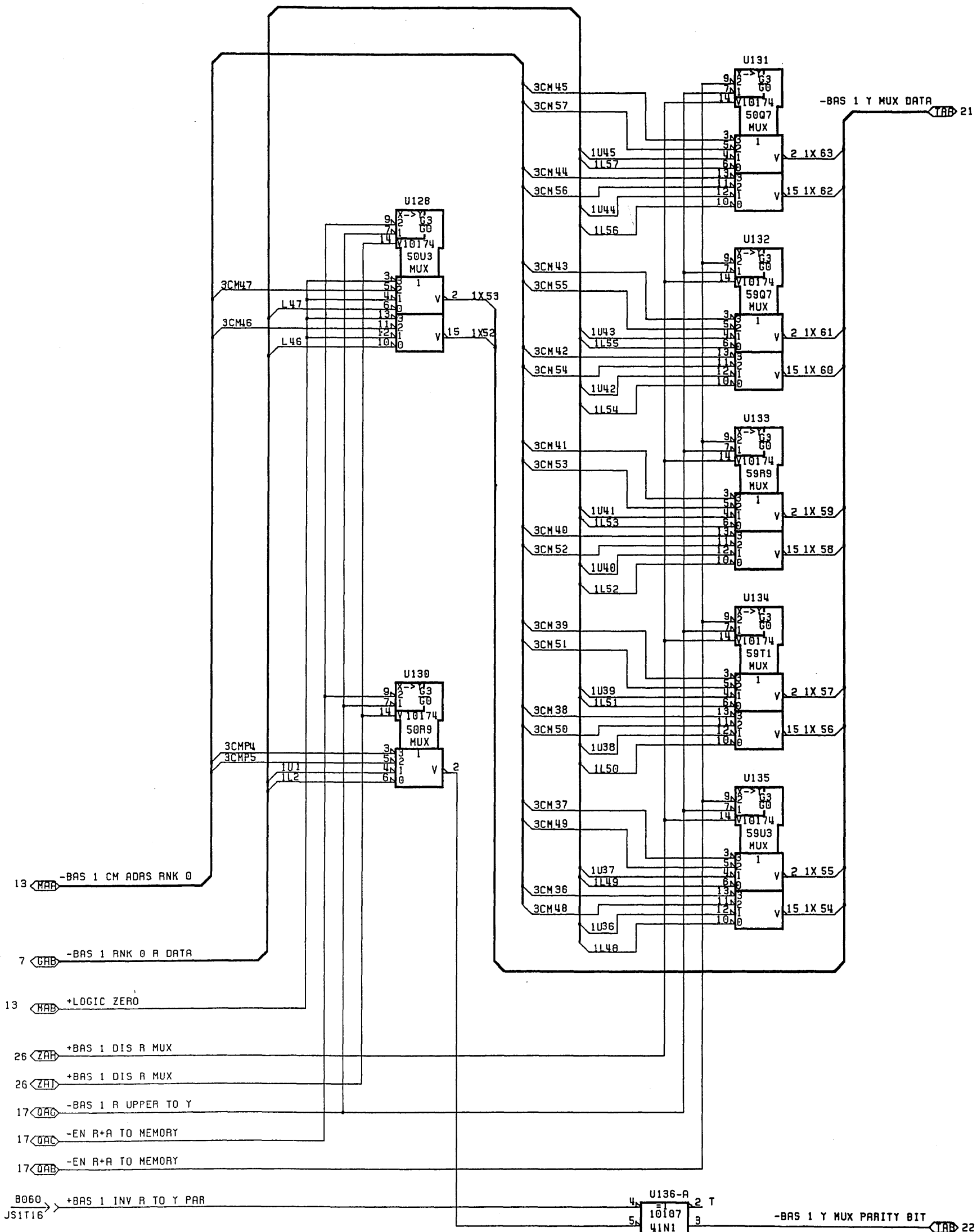
2 LINE LENGTH NO LONGER THEN 12"



R-A BOARD
DATA TO MAC MUX AND
BOARD ERROR GENERATION
TYPE 1JCH/1JUH

DWG NO.	DATE	REV
B	22105671	06/15/88
SHEET NO. 19	60462210	PAGE JC-19


BAS 1 R TO Y MUX

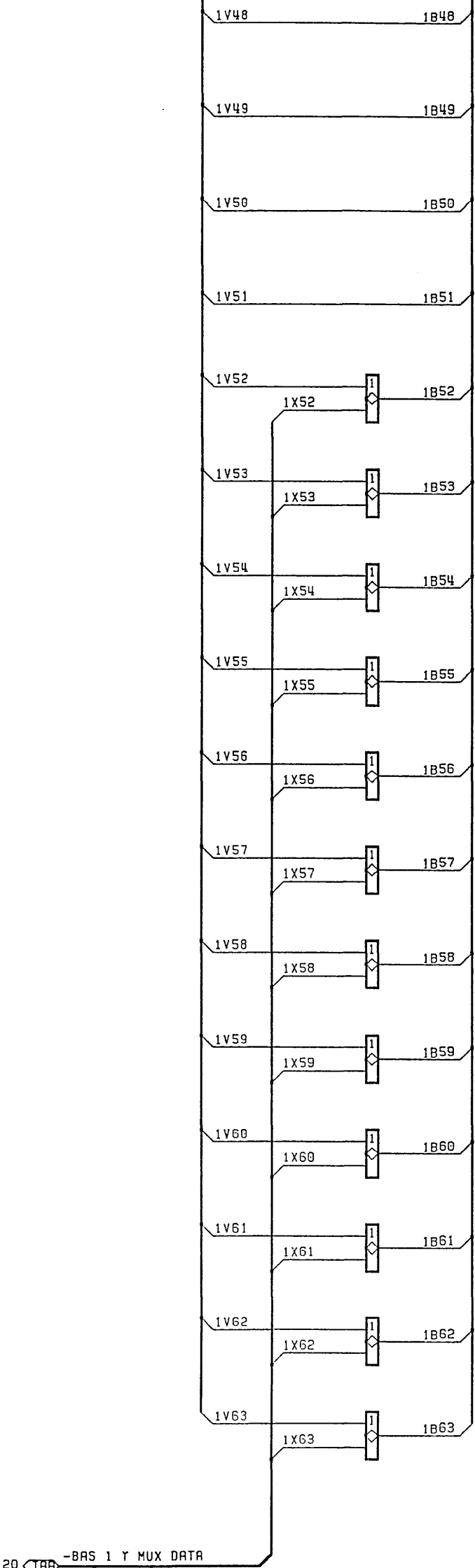



CD	MUX SELECT
0	R LOWER
1	R UPPER
2	R+A LOWER
3	R+A UPPER

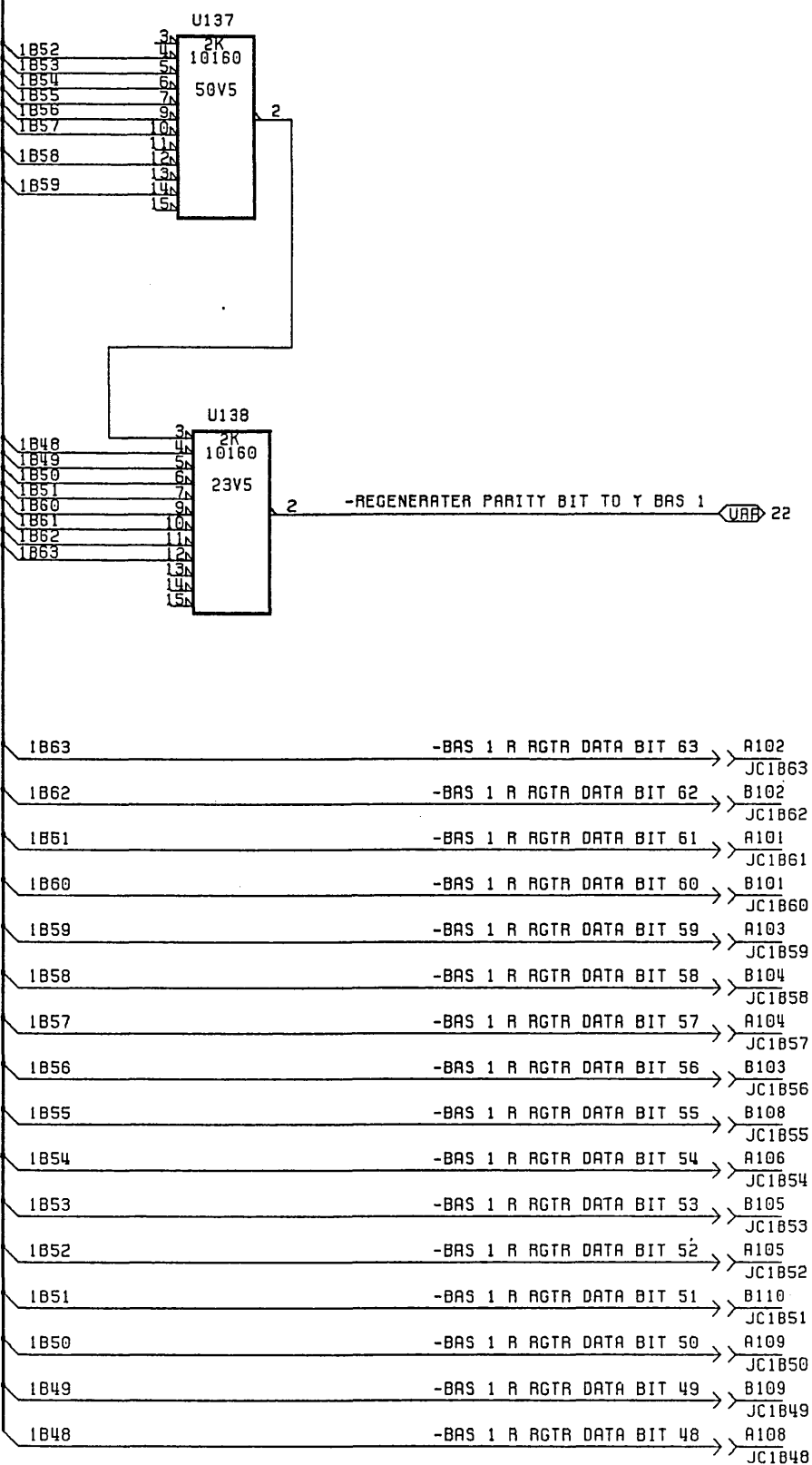
BAS 1 R TO Y DATA MUX


BAS 1 R TO Y DATA OUT

27  -BAS 1 MAC AGTR DATA



20  -BAS 1 Y MUX DATA



 CONTROL DATA	R+A BOARD BARREL 1, R TO Y DATA MUX AND DATA OUTPUT TYPE 1JCH/1JUH		B	DWG NO. 22105671	DATE 02/21/86	REV A
	N		SHEET NO. 21	60462210	PAGE	JC-21



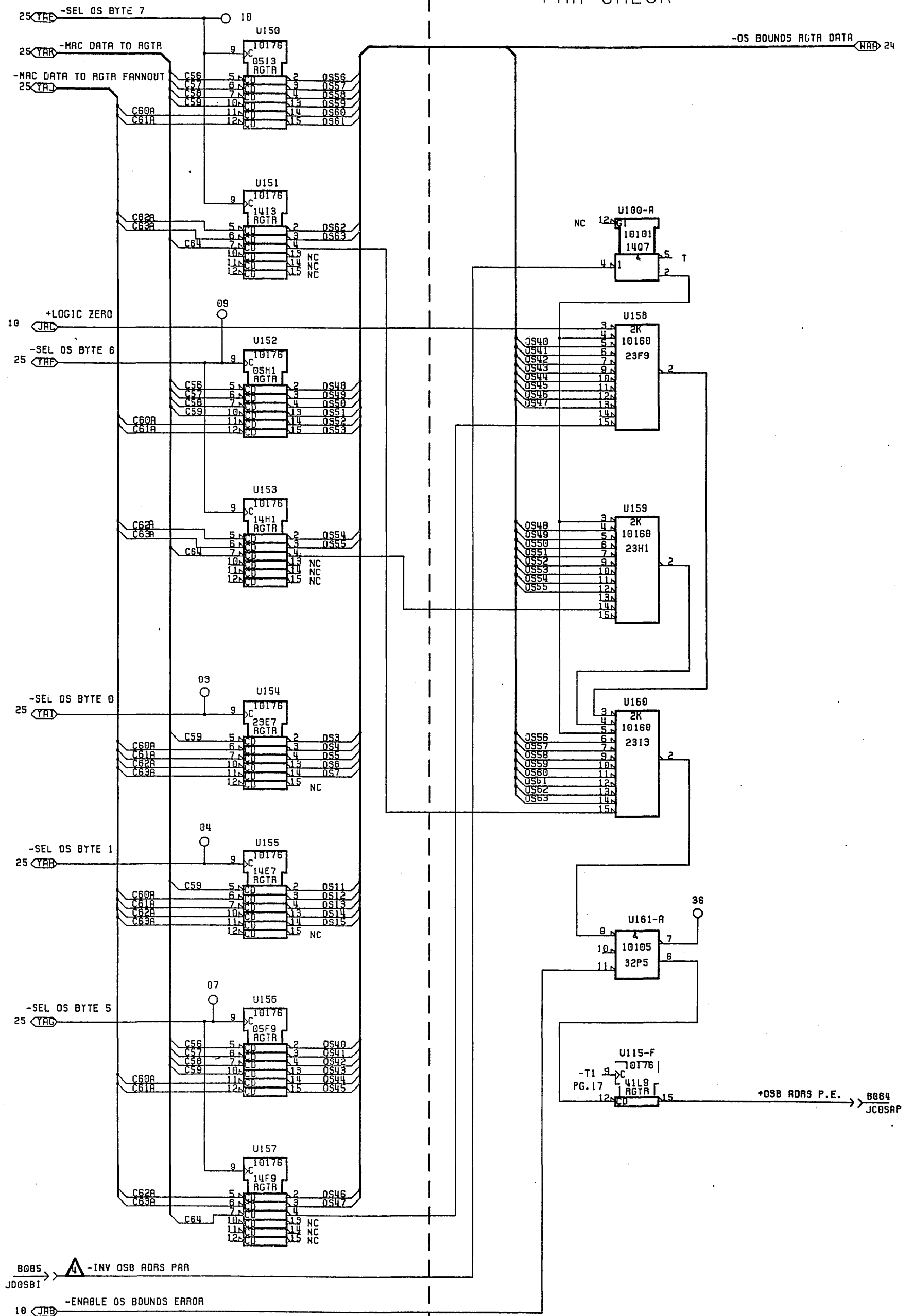
B
SHEET

DATE	08/2
0671	08/2
0462210	

REV	
C	/87
JC-2	PAGE

OSB RGTR

OSB ADRS PAR CHECK



GROUPED TERMINATORS

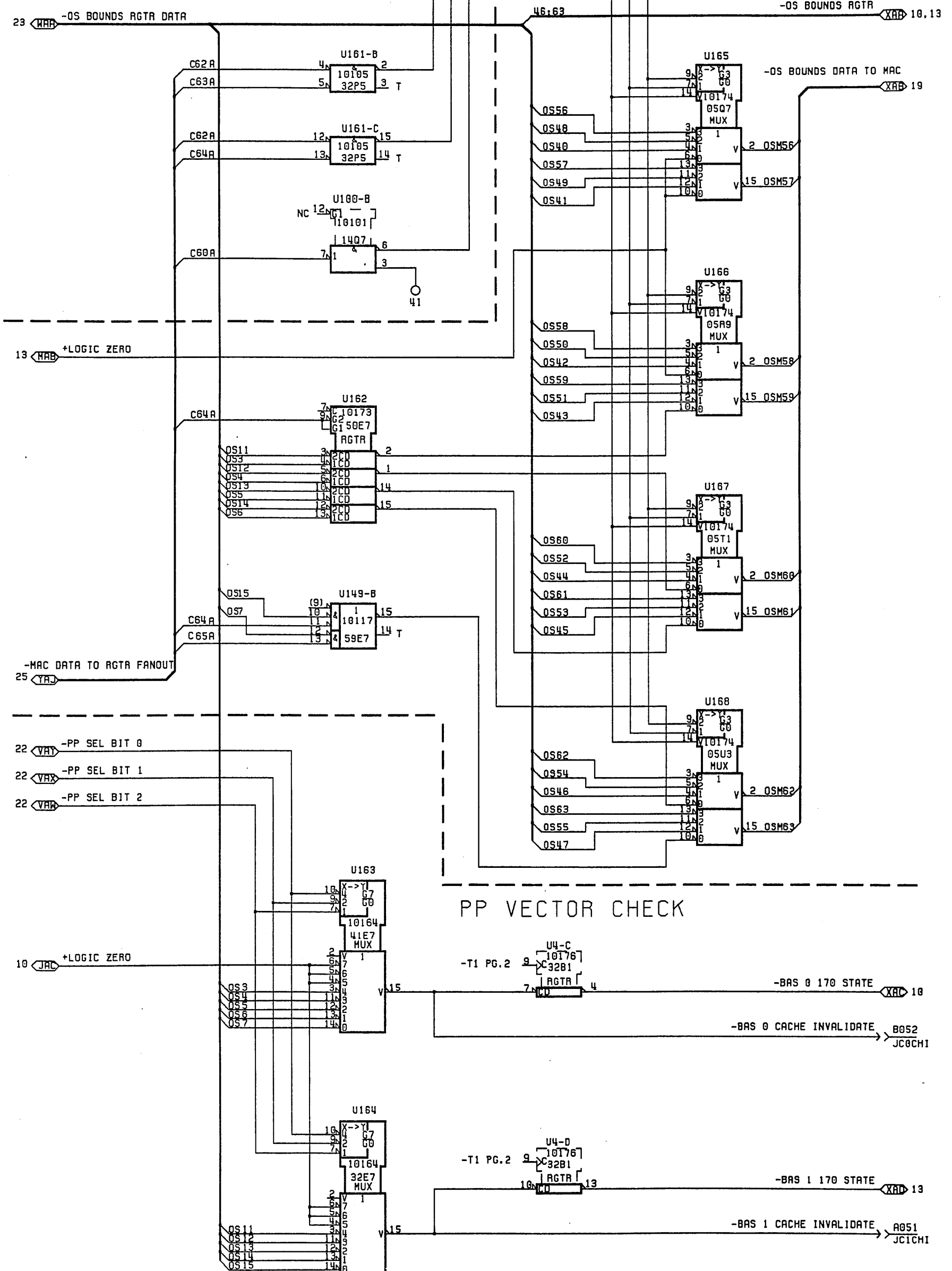



R+A BOARD
OS BOUNDS REGISTER AND
ADDRESS PARITY CHECK
TYPE 1JCH/1JUH

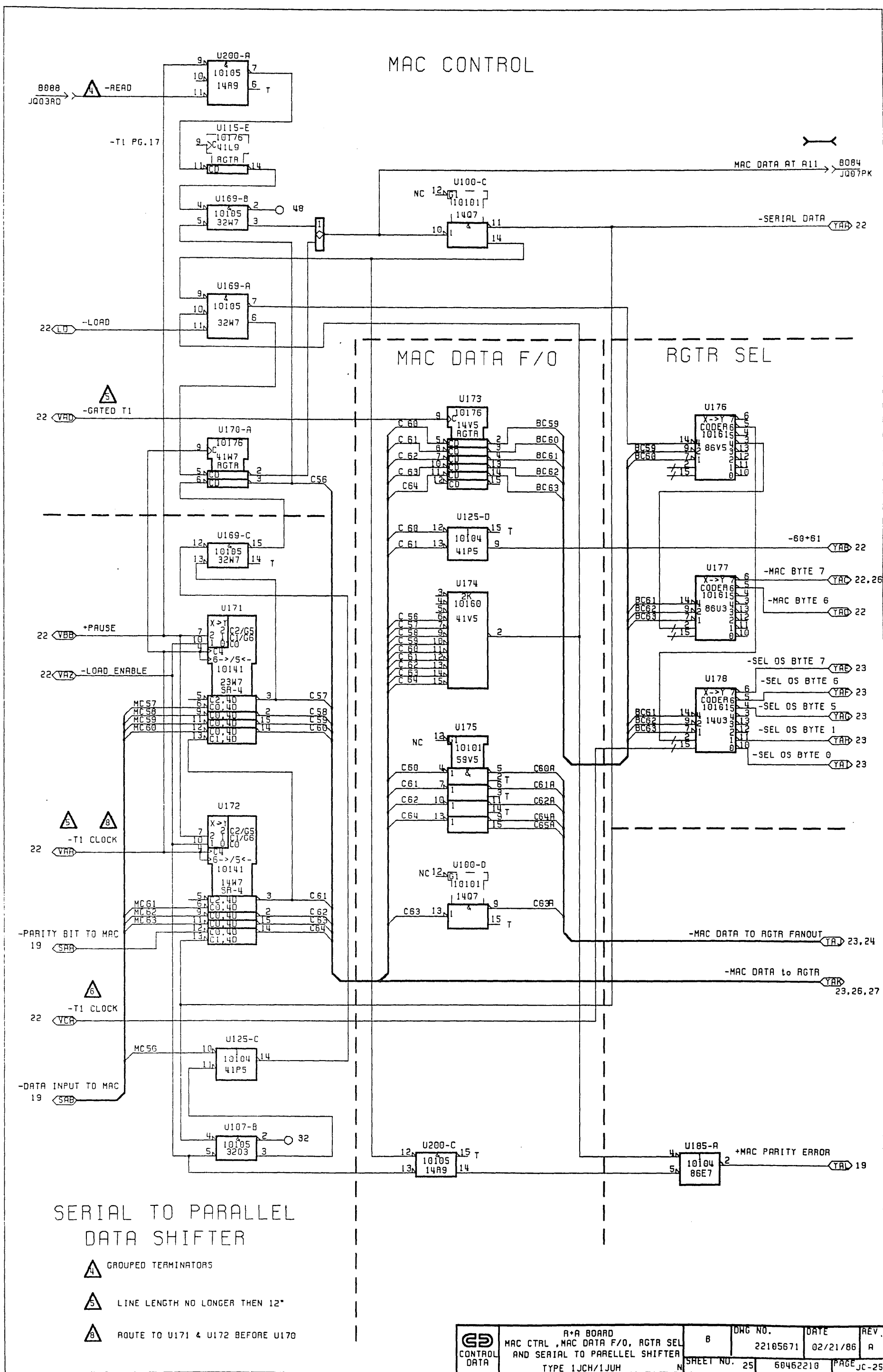
DWG NO.	DATE	REV
B	22105671	11/85/86
SHEET NO. 23	60462210	PAGE JC-23

OSB MUX CONTROL

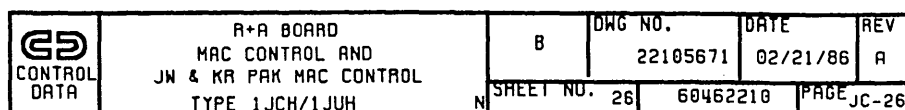
OSB DATA MUX



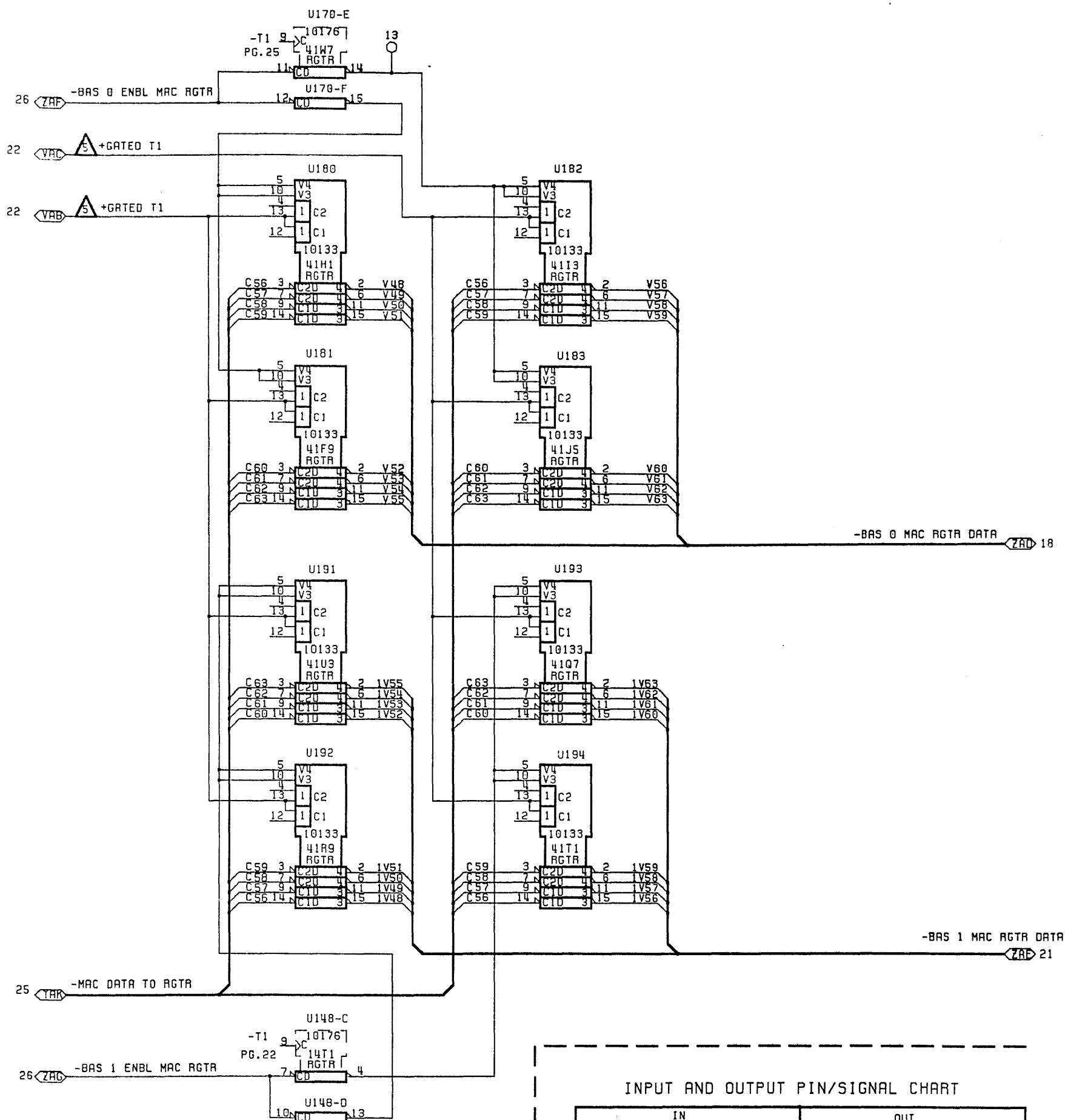
 CONTROL DATA	A+A BOARD 05 BOUNDS MUX CONTROL. DATA MUX AND PP VECTOR CHECK TYPE 1JCH/1JUH	B	DWG NO.	DATE	REV.
			22105671	02/21/86	A
			SHEET NO. 24		60462210



JW AND KR PAK
MAC CONTROL

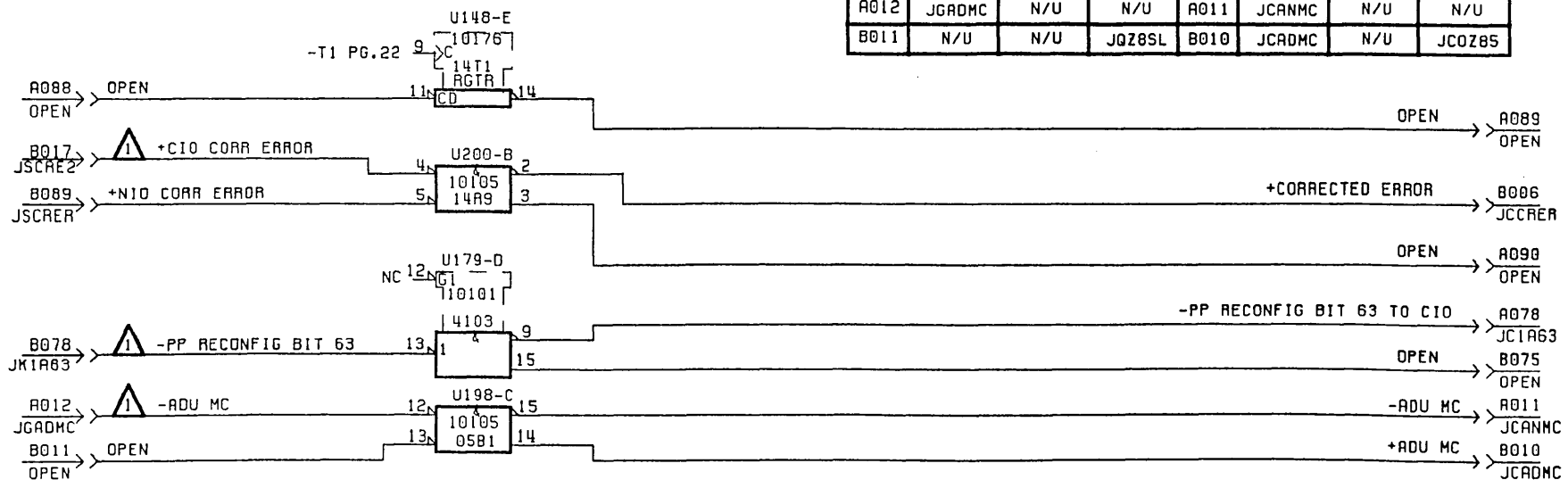


MAC STORE RGTRS



INPUT AND OUTPUT PIN/SIGNAL CHART

IN				OUT			
PIN	A11	A10	A09	PIN	A11	A10	A09
A088	N/U	N/U	N/U	A089	N/U	N/U	N/U
B017	JSCRE2	N/U	JQIUCE	B006	JCCRER	N/U	JCCLRE
B089	JSCRER	N/U	N/U	A090	N/U	N/U	N/U
B078	JK1A63	N/U	JQADMC	A078	JC1A63	N/U	JCADMC
				B075	N/U	N/U	N/U
A012	JGADMC	N/U	N/U	A011	JCANMC	N/U	N/U
B011	N/U	N/U	JQZ8SL	B010	JCADMC	N/U	JCOZ85



NOT TERMINATED

LINE LENGTH NO LONGER THEN 12"




R+A BOARD
MAC STORE REGISTERS
TYPE 1JCH/1JUH

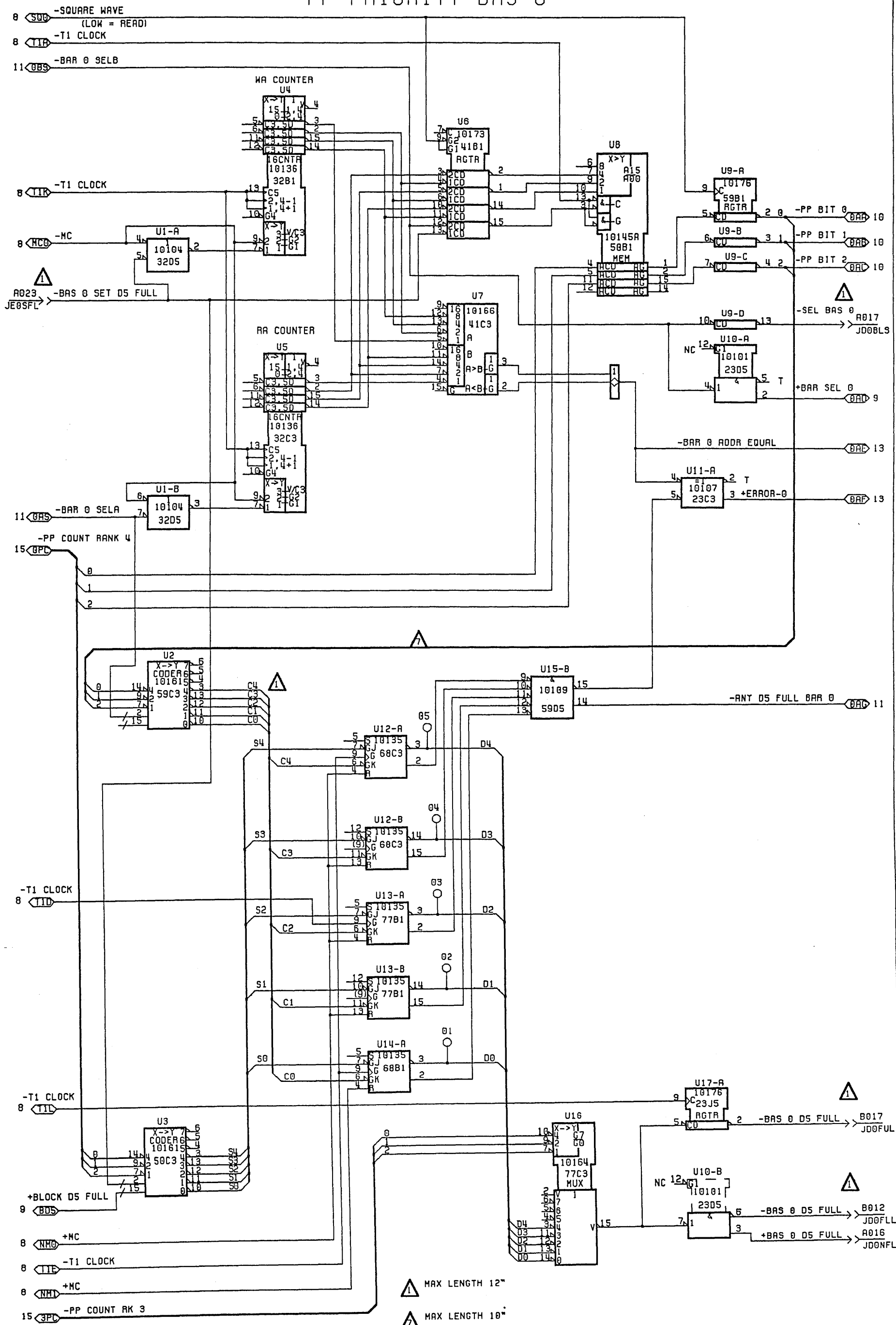
B DMC NO. 22105671 DATE 02/21/86 REV A
SHEET NO. 27 60462210 PAGE JC-27

TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	2	-BBLO R+A ENABLE	27		
32	25	-SERIAL DATA	28	2	-BBLO A BIT 63 RK4
02	2	BBLO R BIT 57 RK4	36	23	-OS BDS ADDR P.E.
10	23	-SEL OSB BYTE 7	34	9	-BBLO ADD ST CHIP SEL
43	15	+CM ADDRESS PE	35	9	-ADD STORE SEL BIT 2
03	23	-SEL OSB BYTE 0	13	27	+ENA MAC BBLO
07	23	SEL OSB BYTE 5	33	12	-BBL1 ADD ST CHIP SEL
16	17	-EN R+A TO MEM	37	12	-ADD STORE SEL BIT 1
04	23	-SEL OSB BYTE 1	38	9	-ADD STORE SEL BIT 0
08	26	+MUX SEL BIT 63	42	17	-BBL1 R UPPER SEL
09	23	-SEL OSB BYTE 6	45	13	-BBL1 CM ADDR 38 RK0
12	26	+MUX SEL BIT 62	41	24	+ENABLE OS BDS MUX
44	22	-PAUSE	06	22	+LOAD ENABLE
15	4	-BBLO RK0 LW R BT56	05	22	-LOAD
14	4	-BBLO RK0 UP R BT62	30		
17	26	+ENA CP MAC MUX	48	25	-MAC READ
18	17	-BBLO R UPPER SEL	31		
19	10	-BBLO CM ADDR 55 RK0	11		
22	13	+BBL1 OS BDS ERR RK0	39		
21	10	+BBLO OS BDS ERR RK0	40		
20	26	+ENA CR MAC MUX	46	7	-BBL1 RK0 LW R BT47
25	22	+ERR DATA TO Y BBL1	50	5	-BBL1 R+A ENABLE
24	19	+BBLO ERR DATA TO Y	51	5	-BBL1 A BIT 47 RK4
23	26	+MUX SEL BIT 61	47	22	+T1 CLOCK
29	15	-CM ADDR BIT 48	49	5	-BBL1 R BIT 36 RK4
26					

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B070 [NOT USED]
TERM	B047, B127, A128, B128, A045
UNUSED	B120

 CONTROL DATA	A+A BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JCH/1JUH	B	DWG NO. 22105671	DATE 11/05/86	REV B
		SHEET NO. 28		60462210	PAGE 028

PP PRIORITY BAS 0

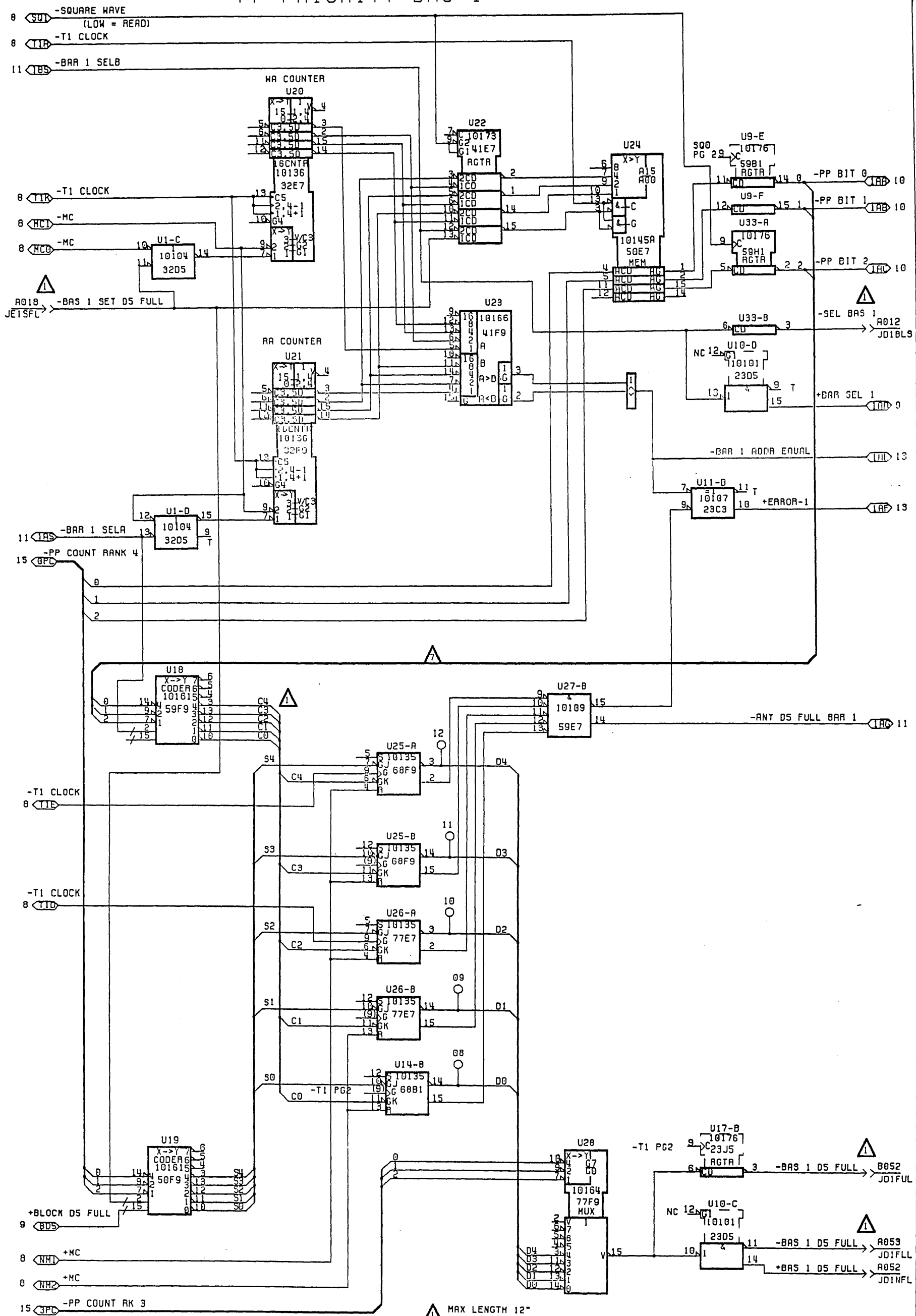


MAX LENGTH 12"

MAX LENGTH 10"


 CONTROL DATA	ADU CONTROL BOARD PP PRIORITY BAS 0		B	DWG NO.	DATE	REV
				53575503	11/01/85	A
	TYPE 1JDH			SHEET NO. 2		60462210

PP PRIORITY BAS 1

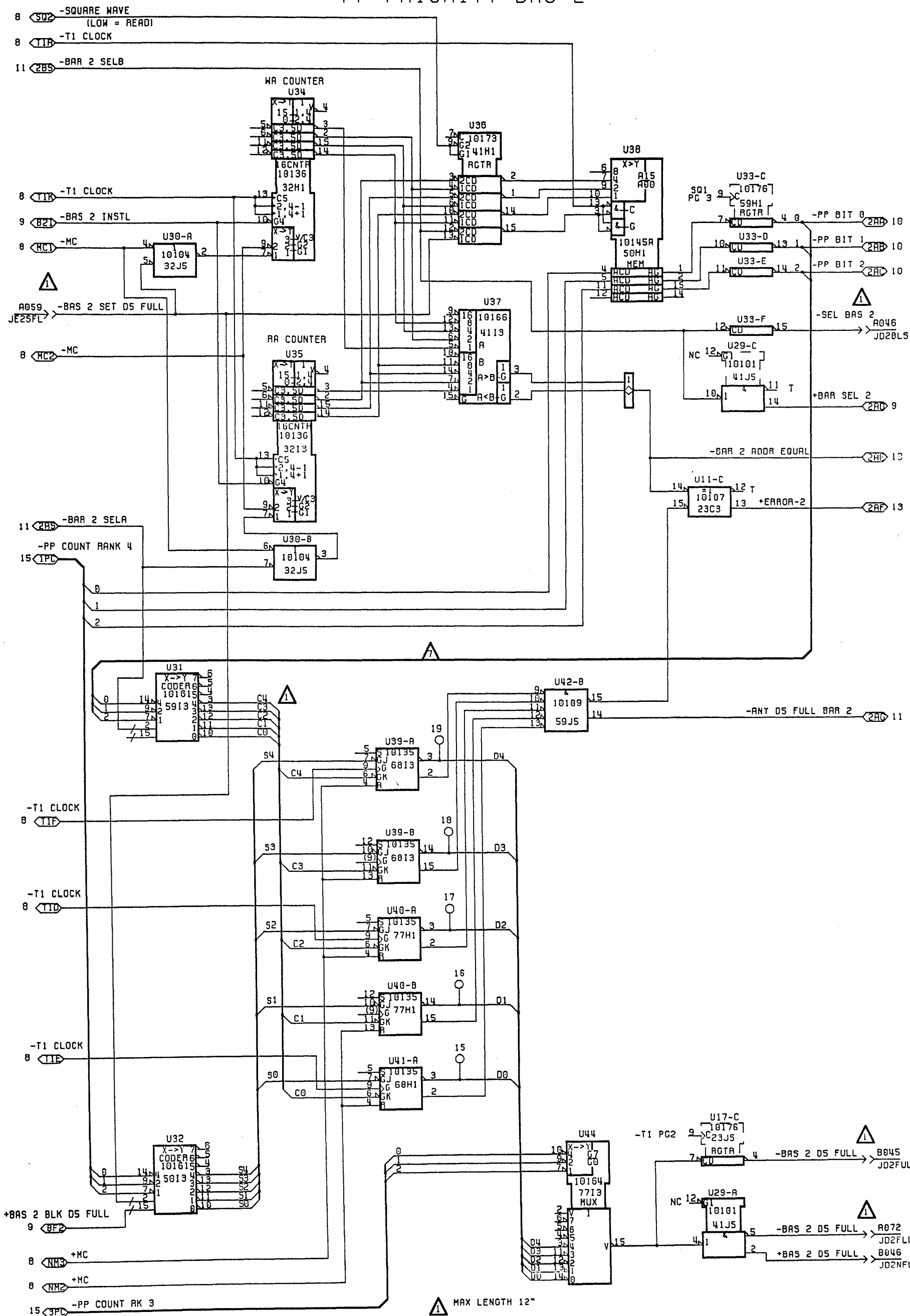


1 MAX LENGTH 12"

A MAX LENGTH 10"

 CONTROL DATA	ADU CONTROL BOARD PP PRIORITY BAS 1	8	DWG NO. 53575503	DATE 11/01/85	REV A
	TYPE 1JDH	SHEET NO. 3	60462210	PAGE 10-03	

PP PRIORITY BAS 2

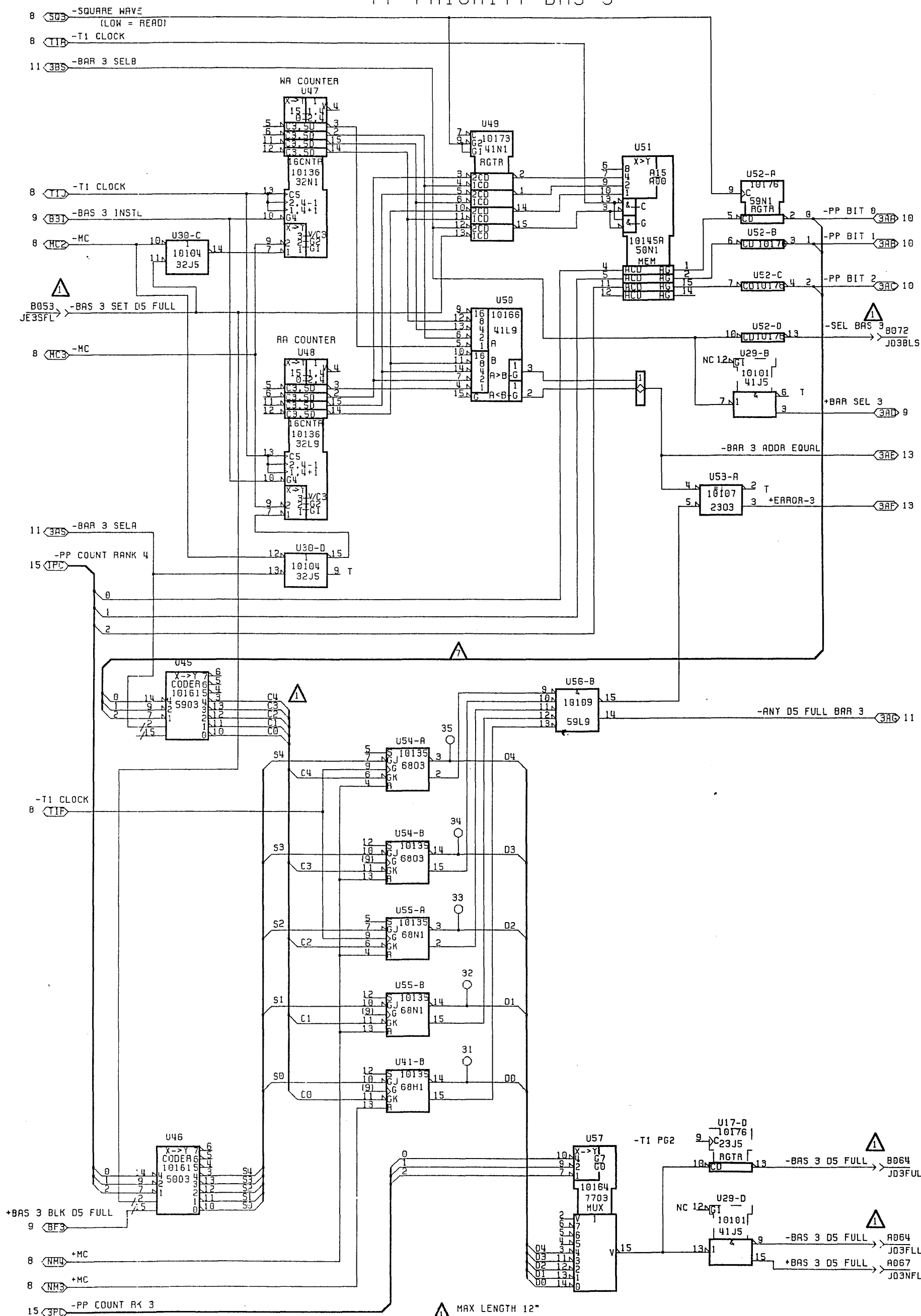


MAX LENGTH 12"

MAX LENGTH 10"

<div> <div> </div> <div> </div> </div>	ADU CONTROL BOARD PP PRIORITY BAS 2 TYPE 1J0H	B	DWG NO. 53575503	DATE 11/01/85	REV A

PP PRIORITY BAS 3

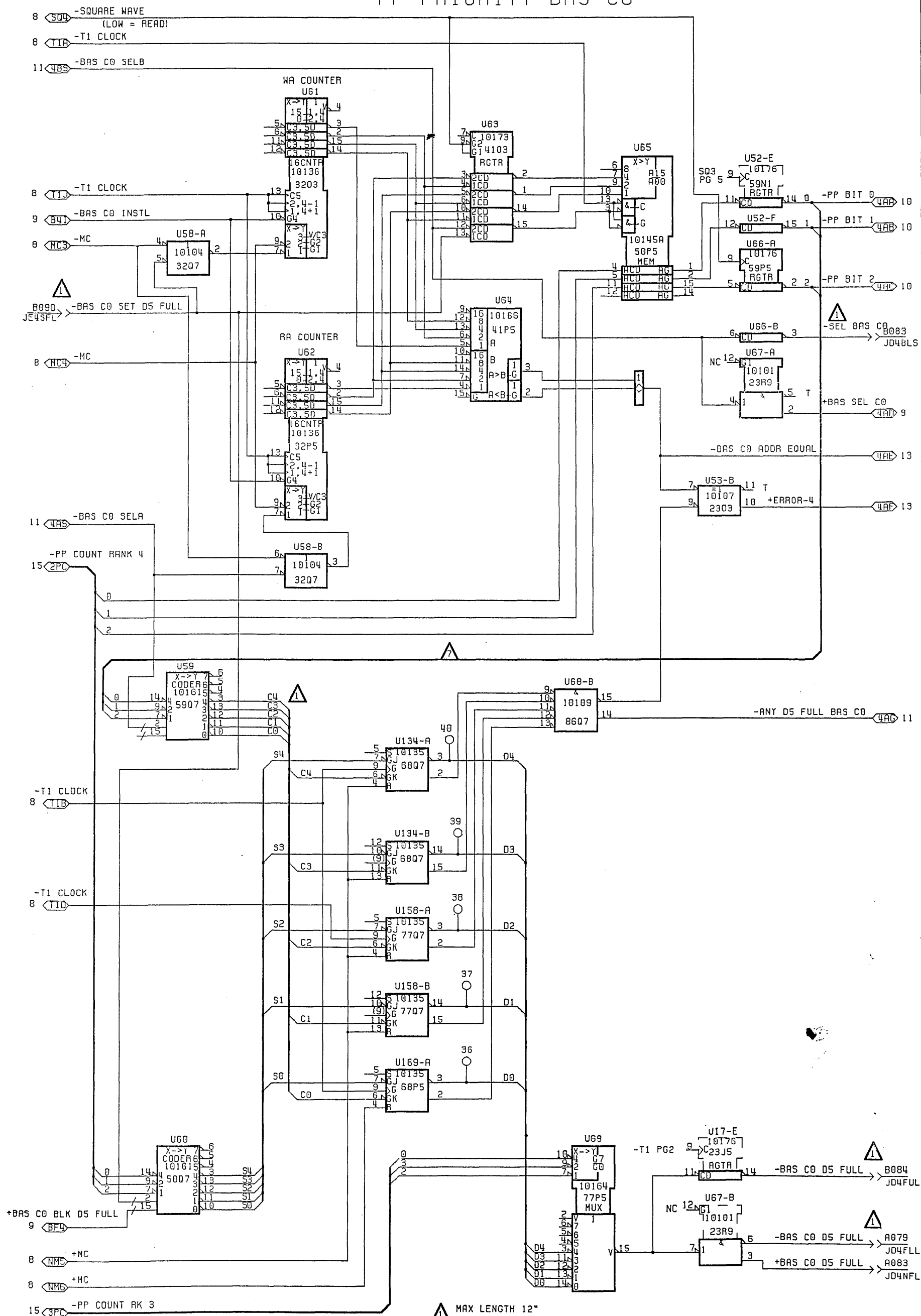


MAX LENGTH 12"

MAX LENGTH 10"


	ADU CONTROL BOARD PP PRIORITY BAS 3 TYPE 1JDH	B	DWG NO. 53575503	DATE 01/12/87	REV C

PP PRIORITY BAS CO

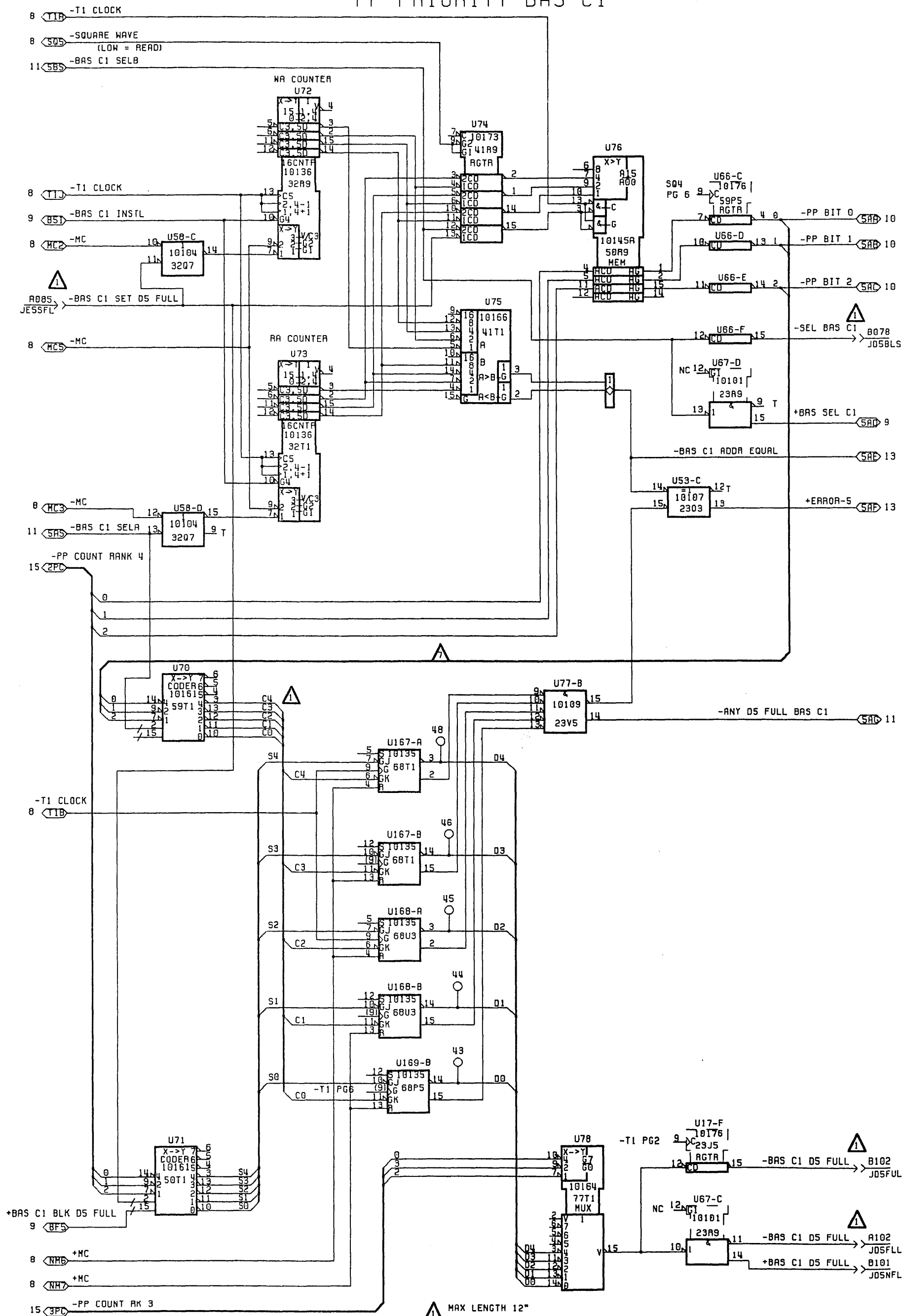


MAX LENGTH 12"

MAX LENGTH 10"

 CONTROL DATA	ADU CONTROL BOARD PP PRIORITY BAS CO TYPE 1JDH	B	DWG NO. 53575503	DATE 11/01/85	REV A
			SHEET NO. 6		60462210

PP PRIORITY BAS C1

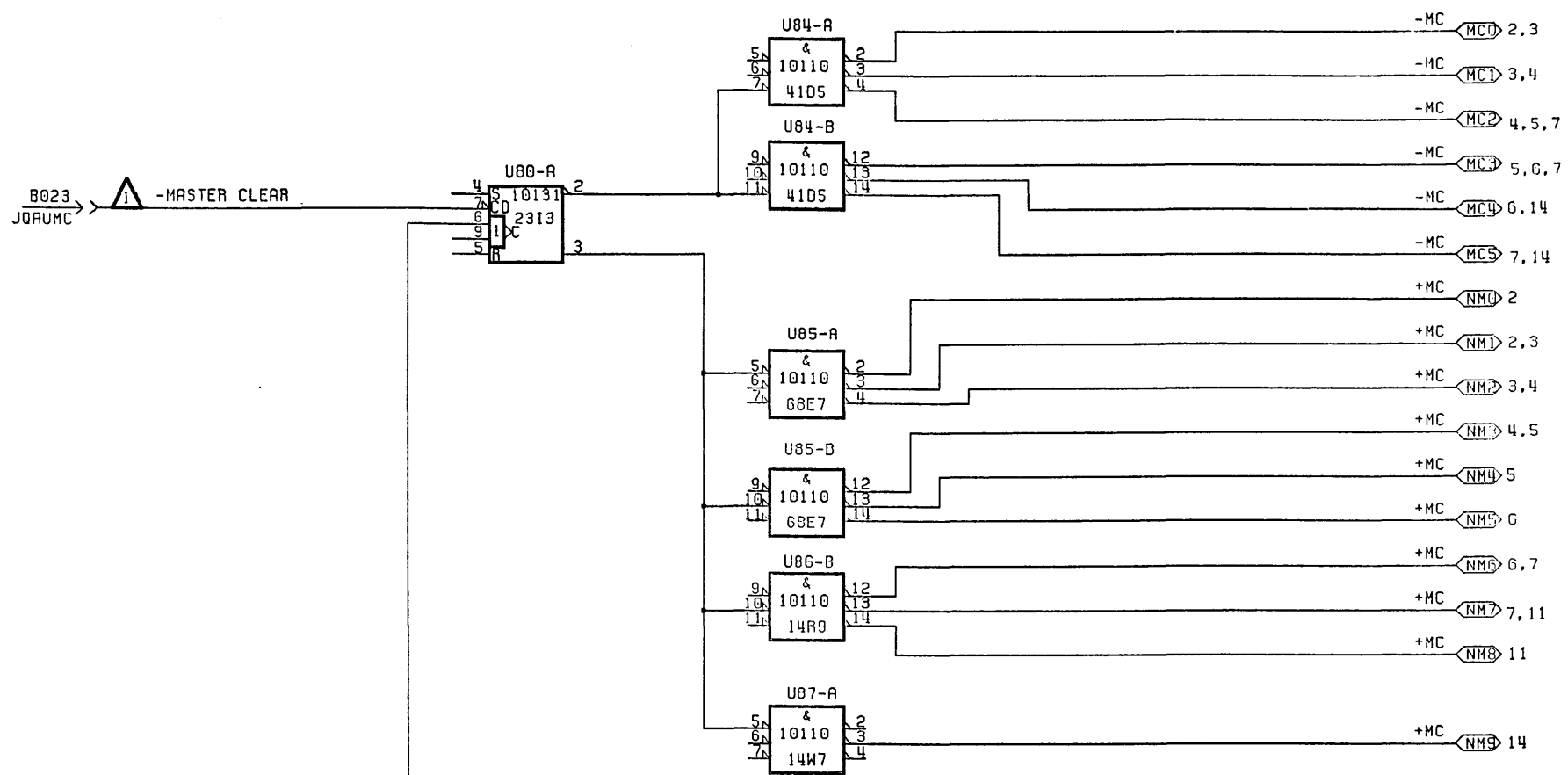


MAX LENGTH 12"

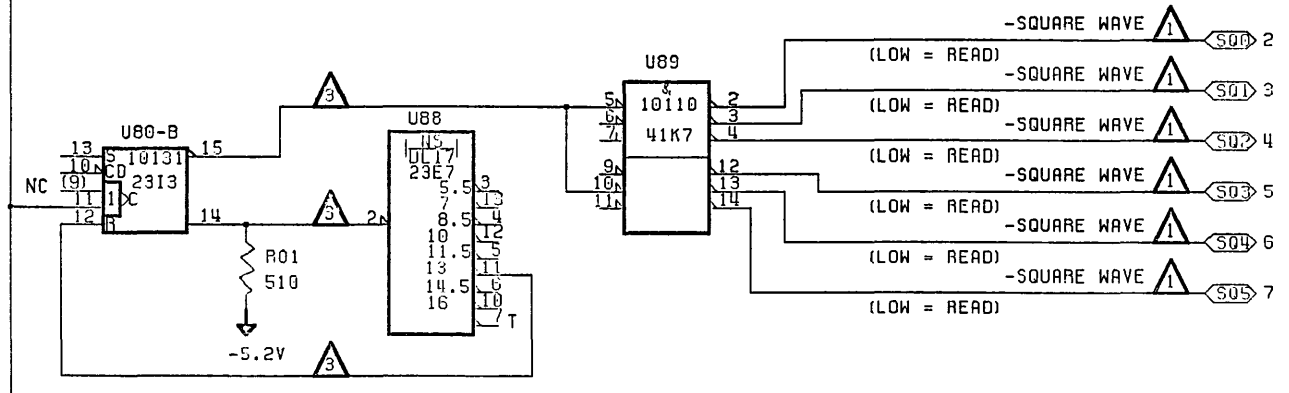
MAX LENGTH 10"

CONTROL DATA	ADU CONTROL BOARD PP PRIORITY BAS C1	B	DWG NO.	DATE	REV
			53575503	11/01/85	A
TYPE 1JDM	SHEET NO. 7	60462210	PAGE	J0-07	

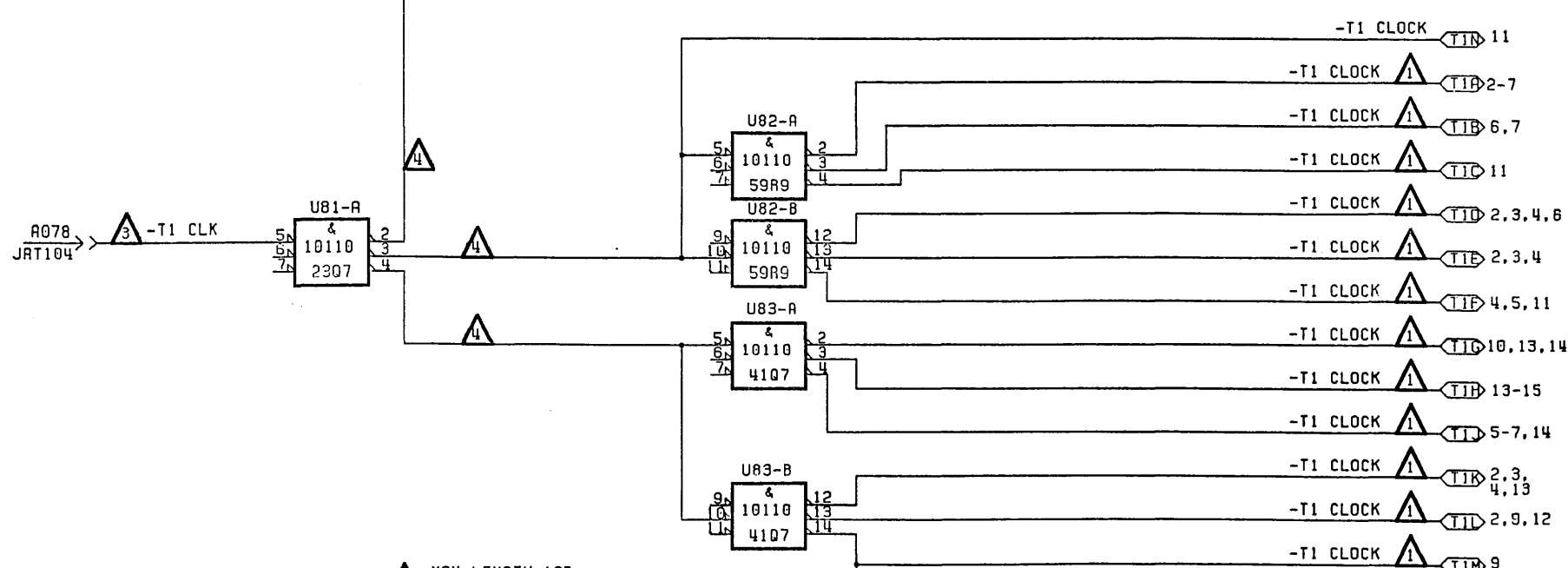
MC F/O




SQUARE WAVE GEN



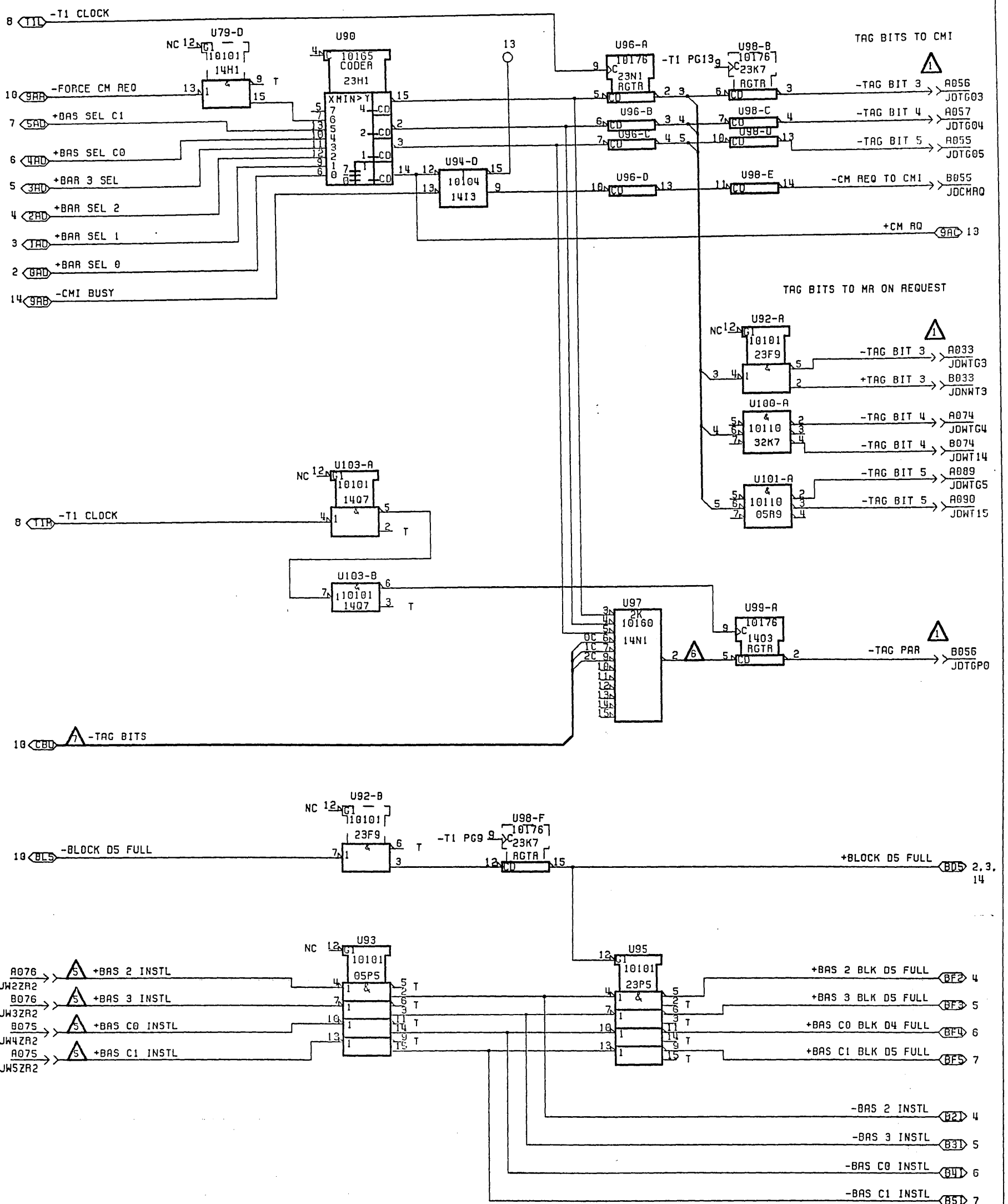
CLK F/O



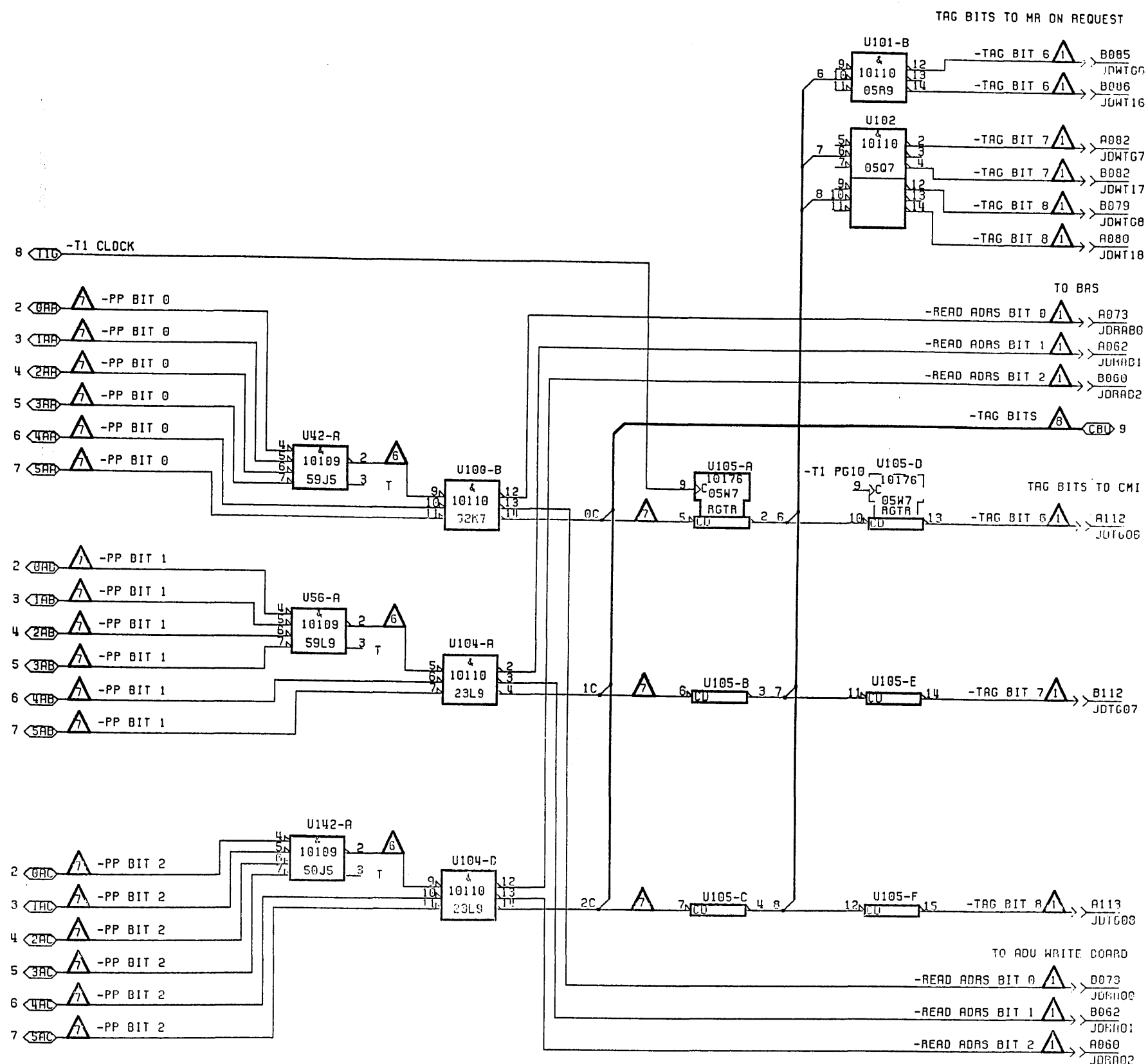
- 1 MAX LENGTH 12"
- 3 MAX LENGTH 4"
- 4 MAX LENGTH 7"

 CONTROL DATA	ADU CONTROL BOARD MASTER CLEAR, SQUARE WAVE AND CLOCK FANOUTS TYPE 1JDH	8	DWG NO.	DATE	REV
			53575503	11/01/85	A
			SHEET NO. 8		

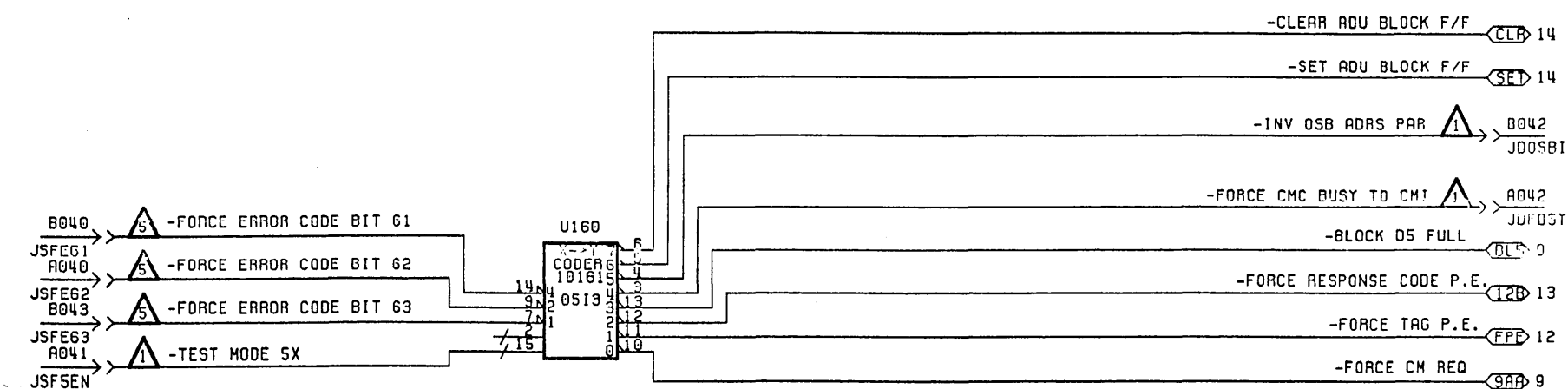
TAG BITS 3-5, PAR GEN F/O



TAG BITS 6-8



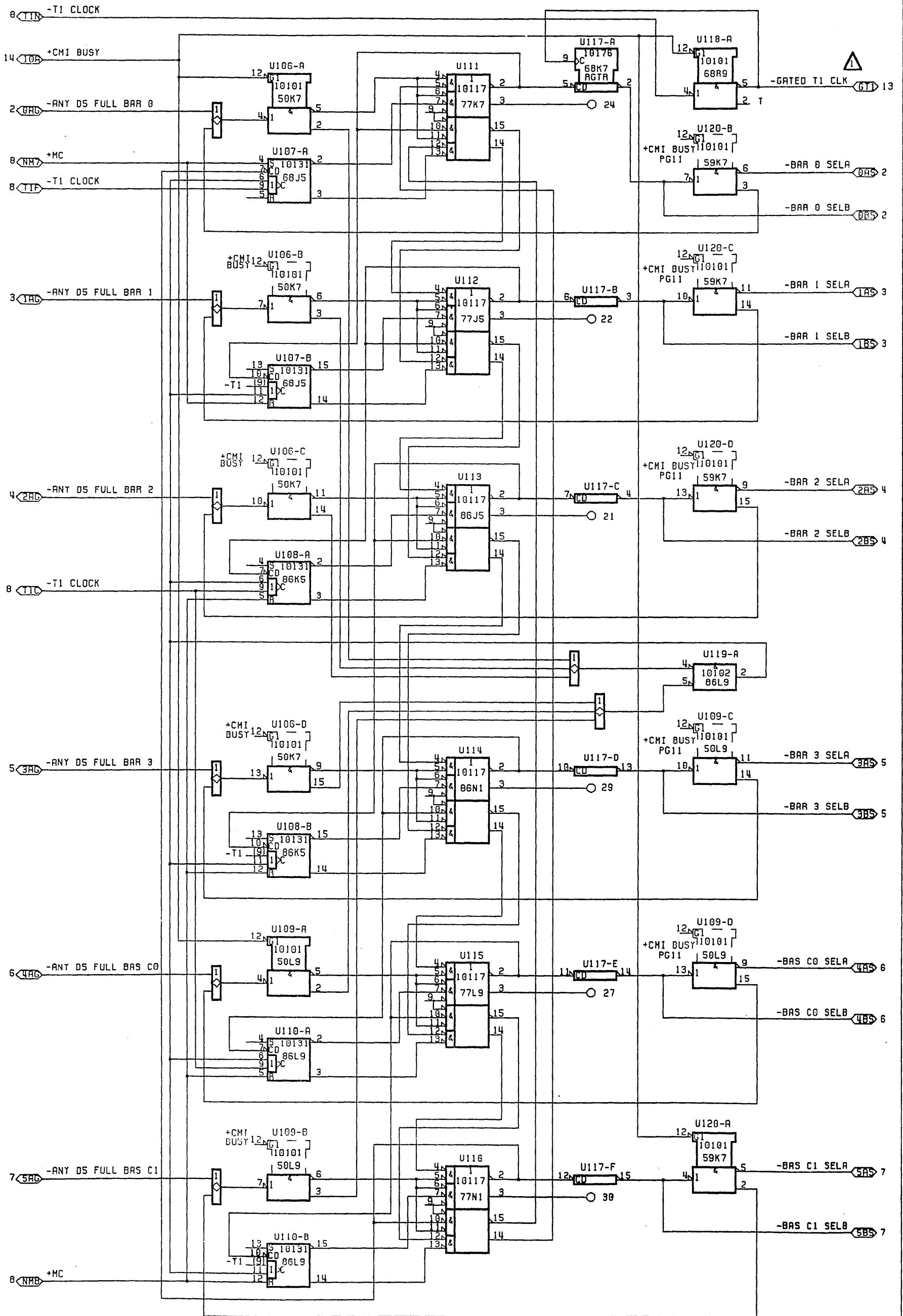
FORCE ERROR DCDR



- 1 MAX LENGTH 12"
- 2 MAX LENGTH 10"
- 3 NOT TERMINATED AND MAX LENGTH 4"
- 4 MAX LENGTH 10" AND ROUTE TO PAGE 9 FIRST
- 5 MAX LENGTH 3"

	ADU CONTROL BOARD TAG BITS 6-8 AND FORCE ERROR DECODE 1JDH	8	DWG NO. 53575503	DATE 11/01/85	REV A

BAS PRIORITY RGTR



MAX LENGTH 12"



NOTE: ALL LINES BETWEEN CHIPS ON THIS PAGE ARE TIMING CRITICAL & SHOULD NOT EXCEED 7" IN LENGTH



CONTROL DATA

ADU CONTROL BOARD
BARREL PRIORITY

TYPE 1J0H

B

OWG NO.
53575503

DATE
11/01/85

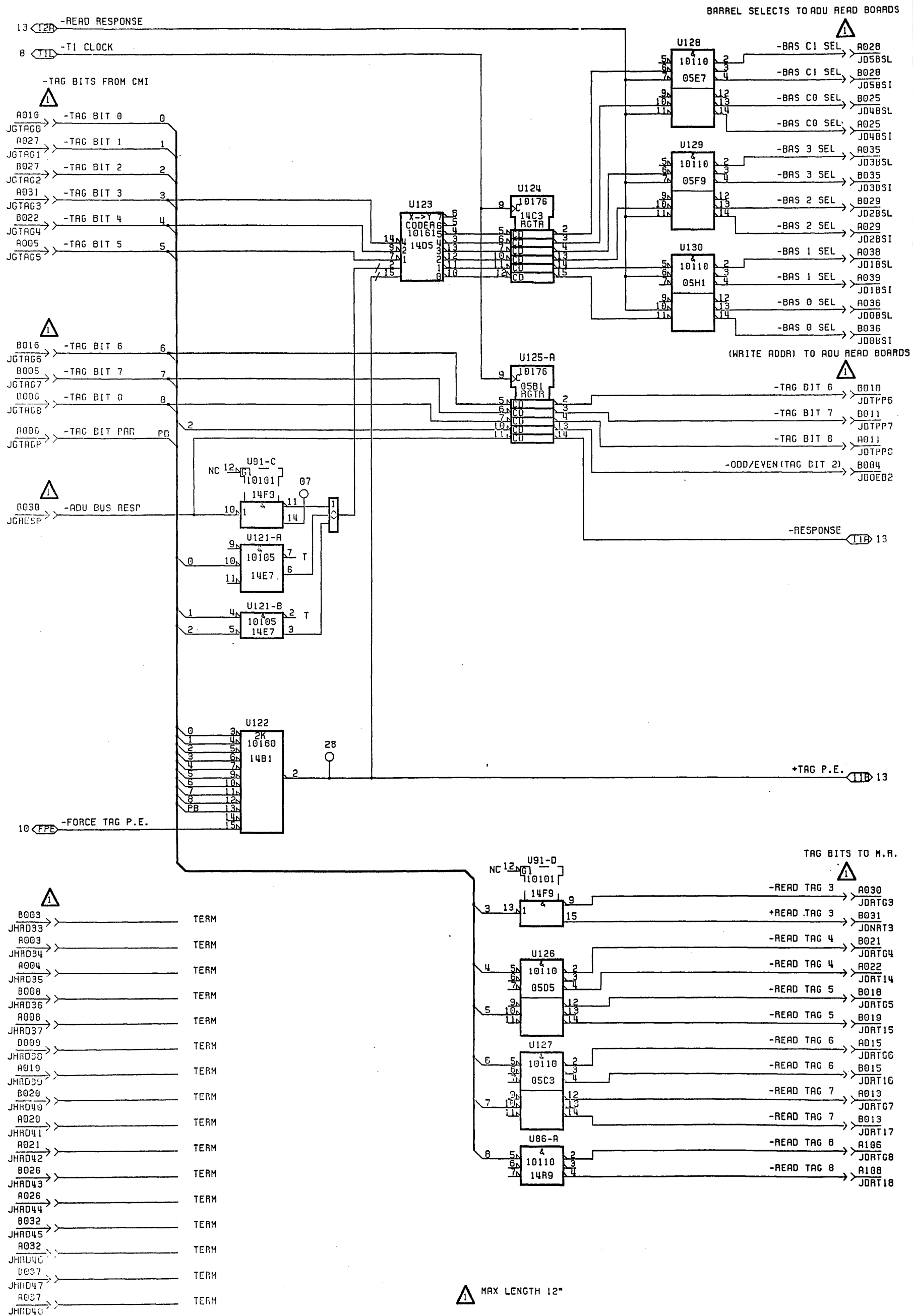
REV
A


SHEET NO. 11

60462210

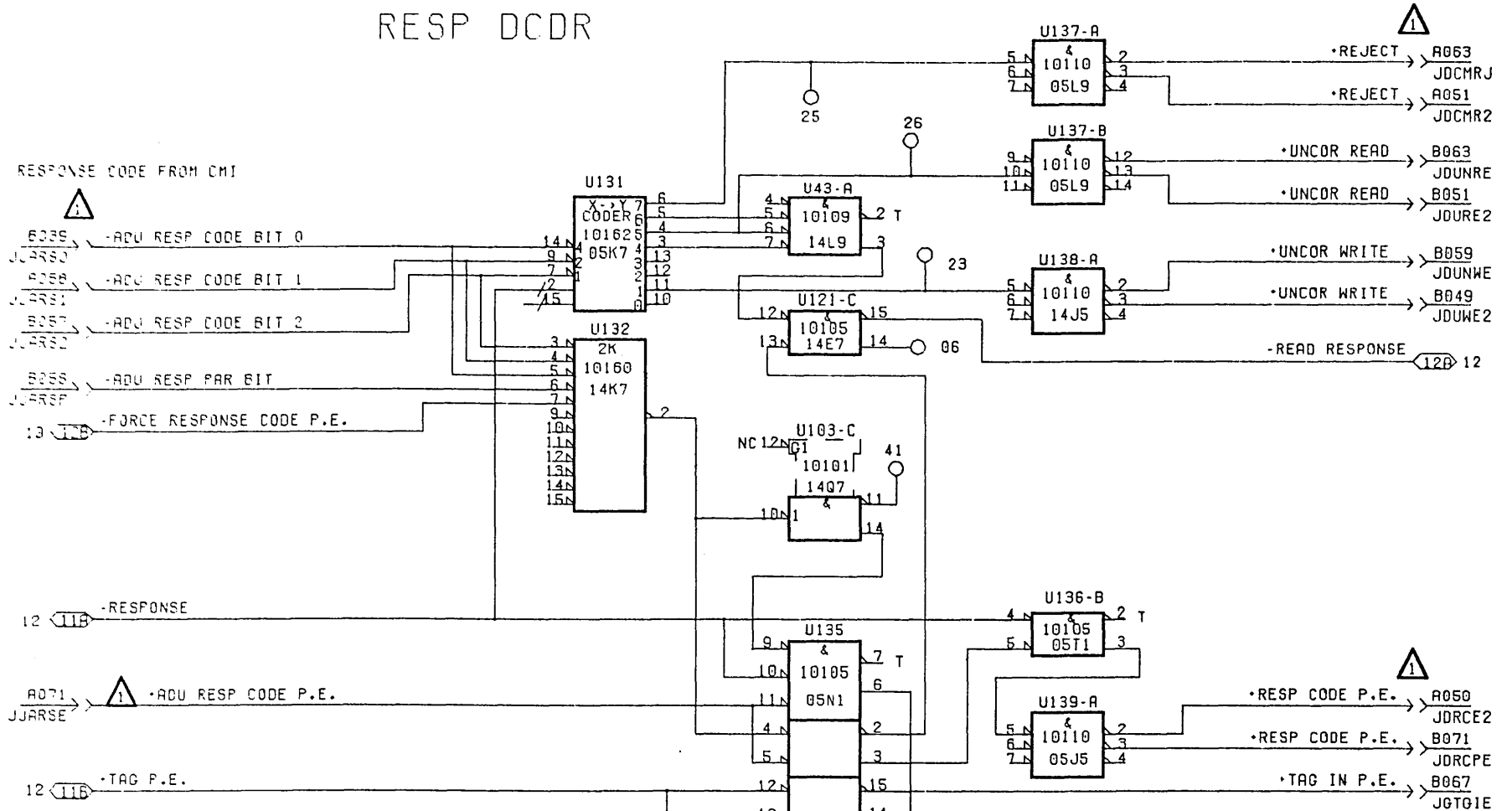
PAGE 10-11

TAG DCDR

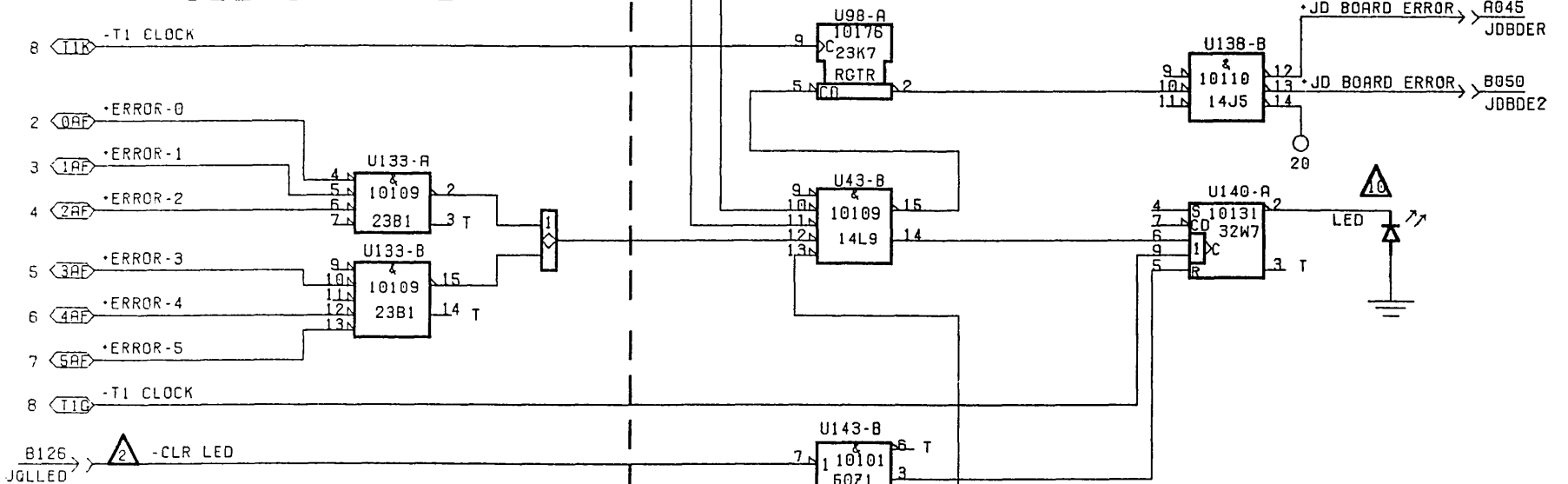


 CONTROL DATA	ADU CONTROL BOARD		B	DWS NO.	DATE	REV
	CMI TAG DECODE			53575503	11/01/05	A
	TYPE 1J0H			SHEET NO. 12	60462210	PAGE
			N			JD-12

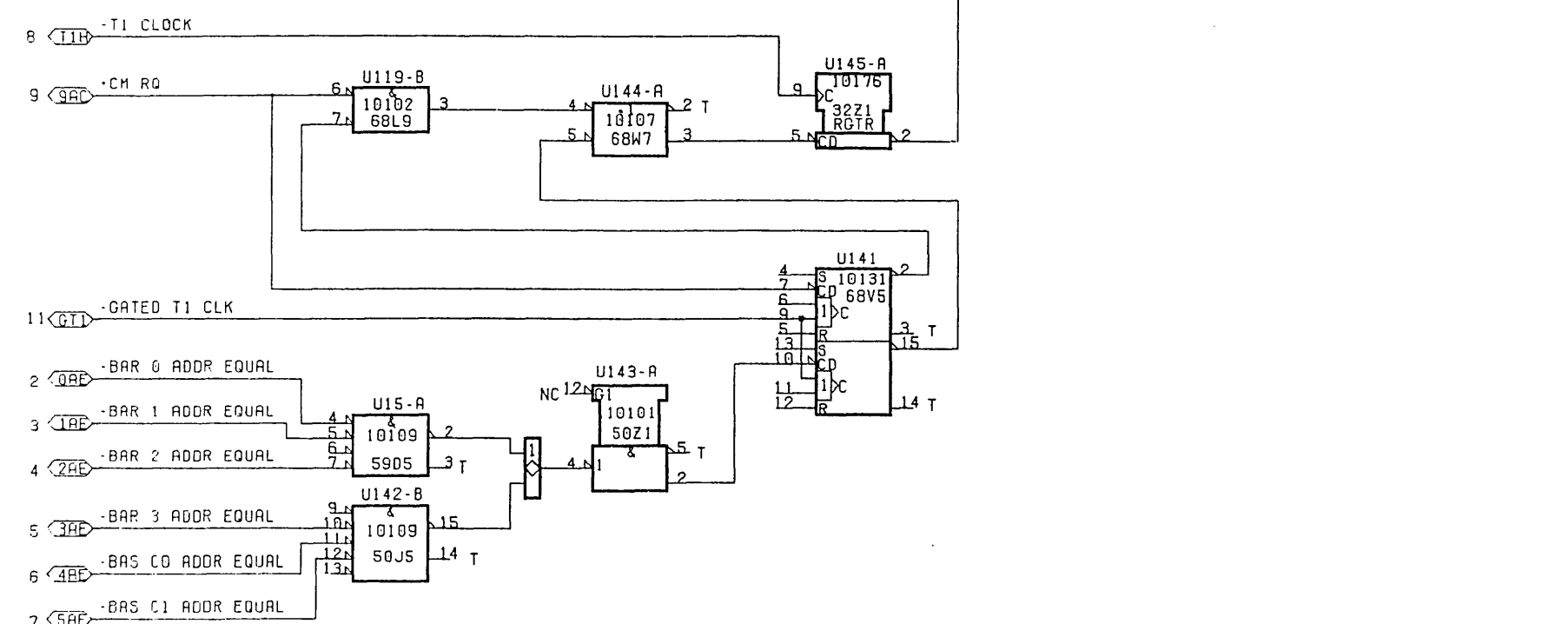
RESP DCDR




ADDRS CNTRS/D5 FULL COMPARE



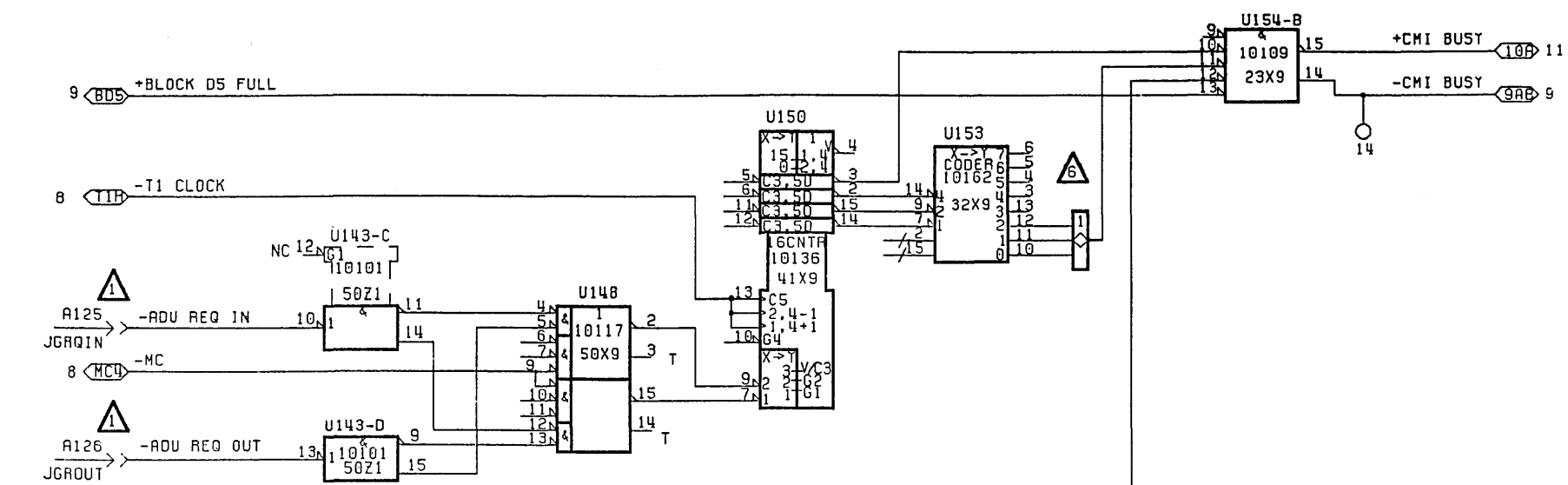
ADRS CNTRS EQUAL TEST



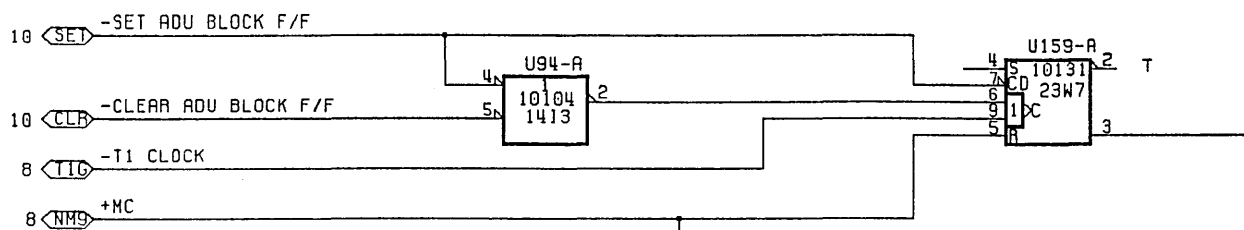
- 1 MAX LENGTH 12"
- 2 NOT TERMINATED AND MAX LENGTH 12"
- 3 TERMINATE

 CONTROL DATA	ADU CONTROL BOARD CMI RESPONSE DECODE. ADDR COUNTER/D5 FULL COMPARE. ADDR COUNTERS EQUAL TEST. BOARD ERROR 1J0H	B	DWG NO. 53575503	DATE 06/15/88	REV D
		SHEET NO.	13	60462210	PAGE
		JD-13			

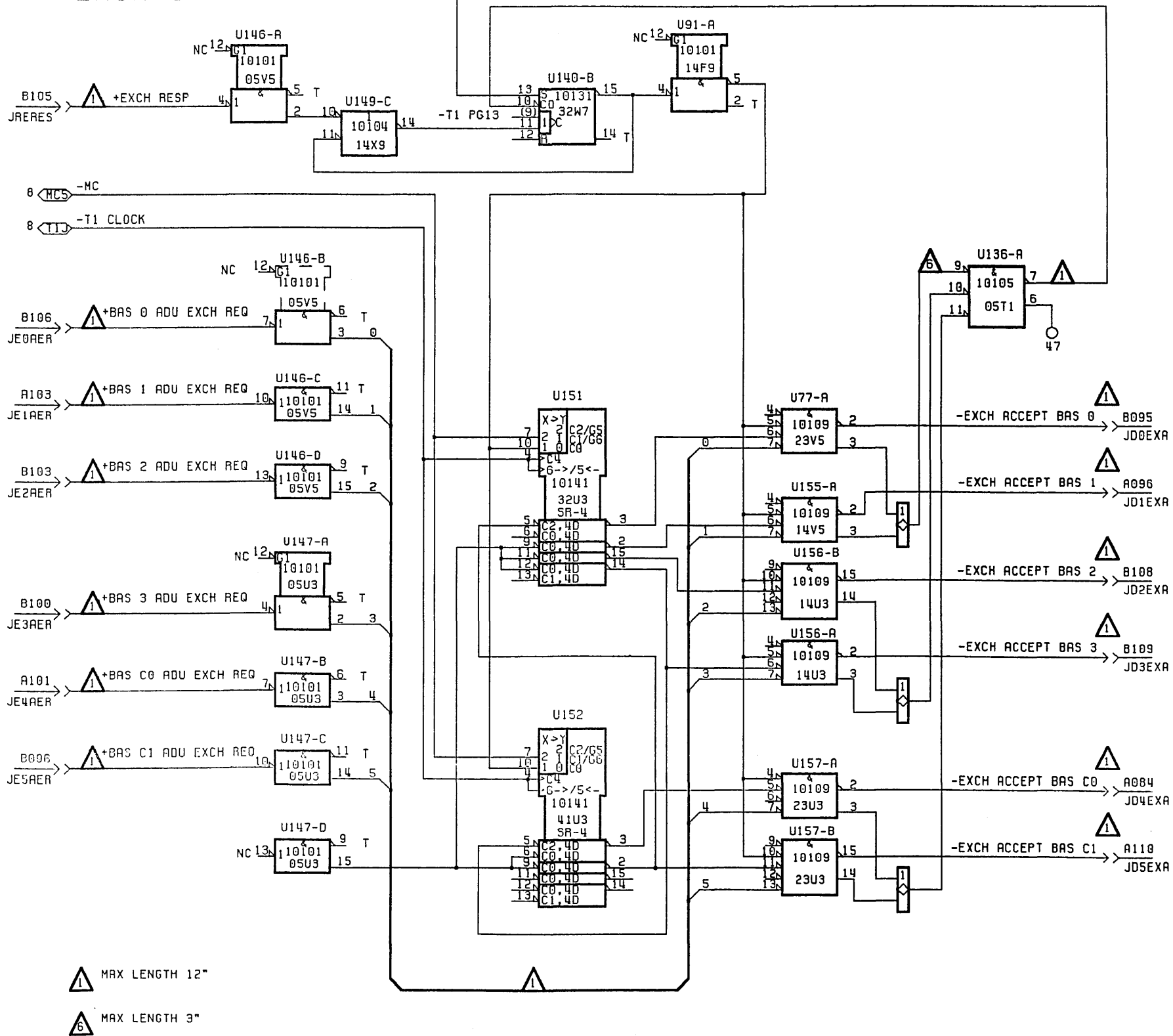
REQ CNTR



TEST CODE ADU CM REQ BLOCK

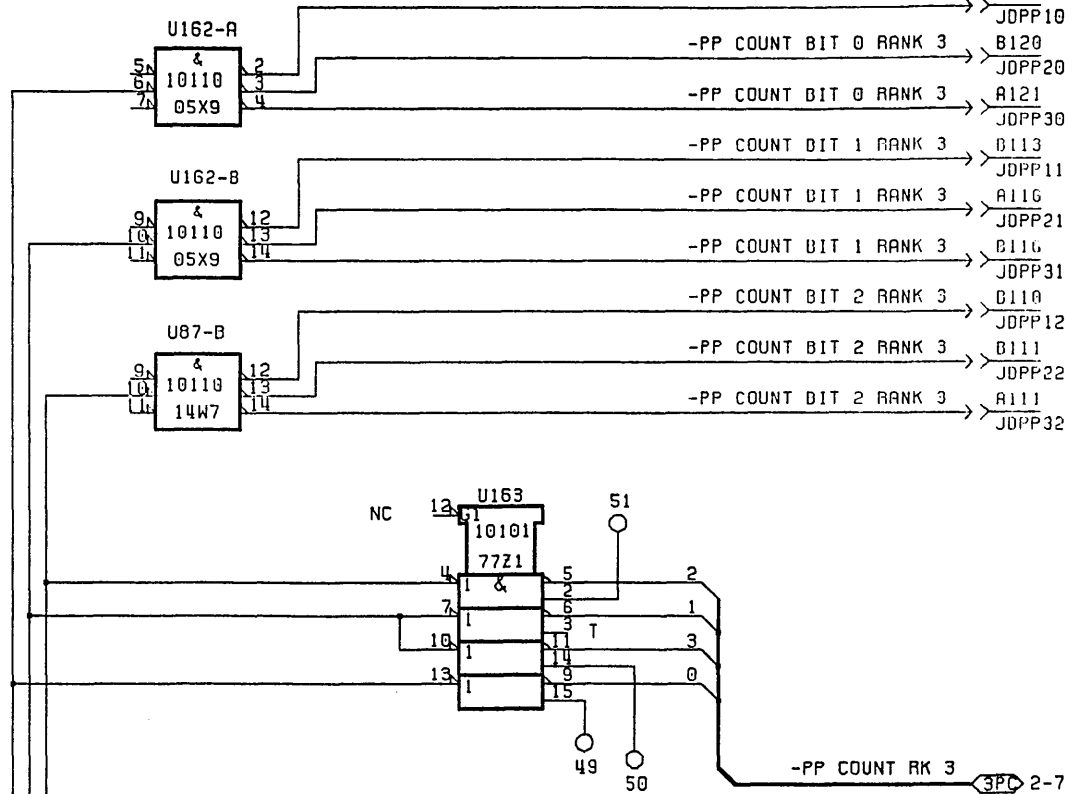


EXCH INTERLOCK

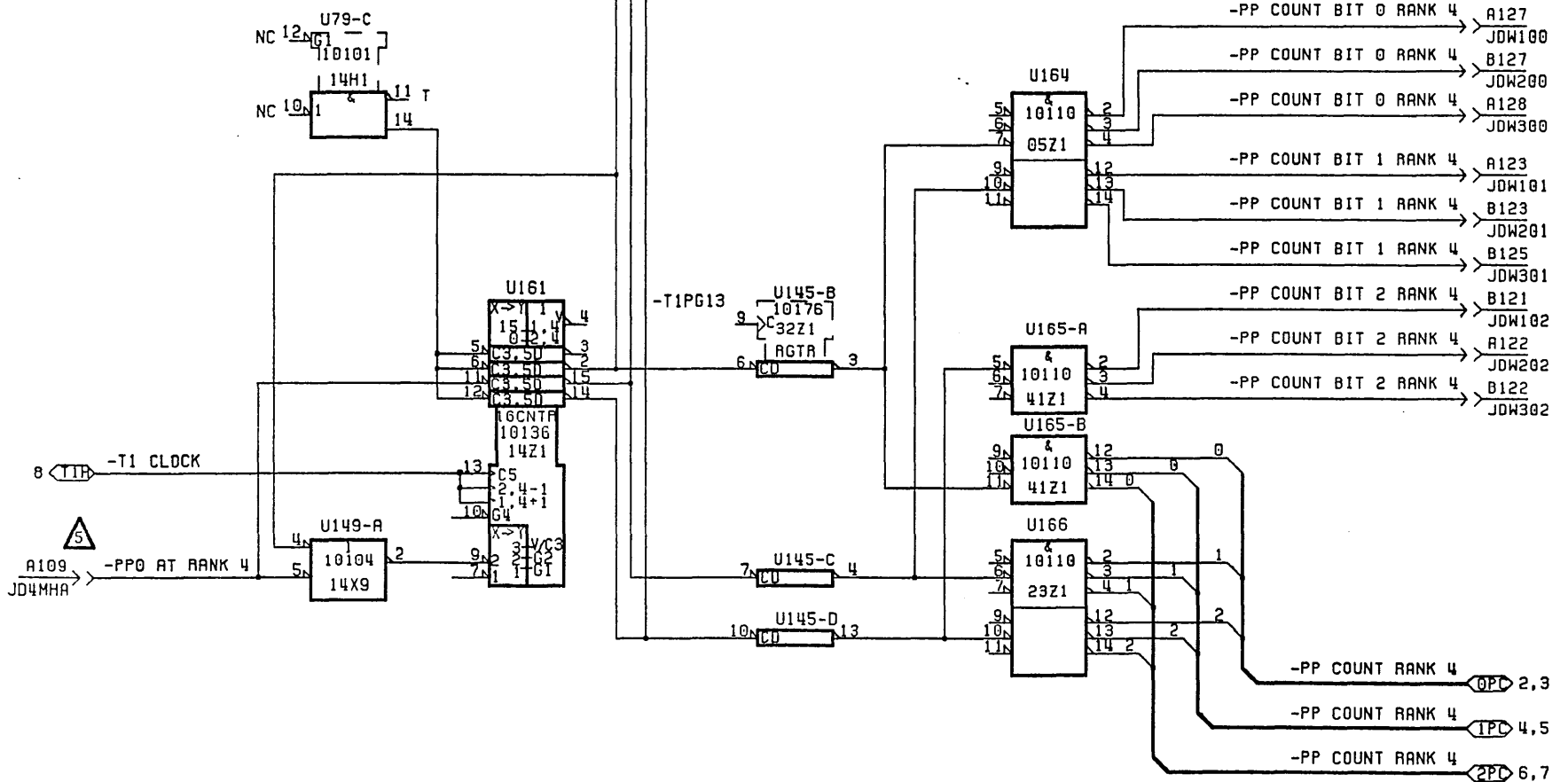


PP CNTR

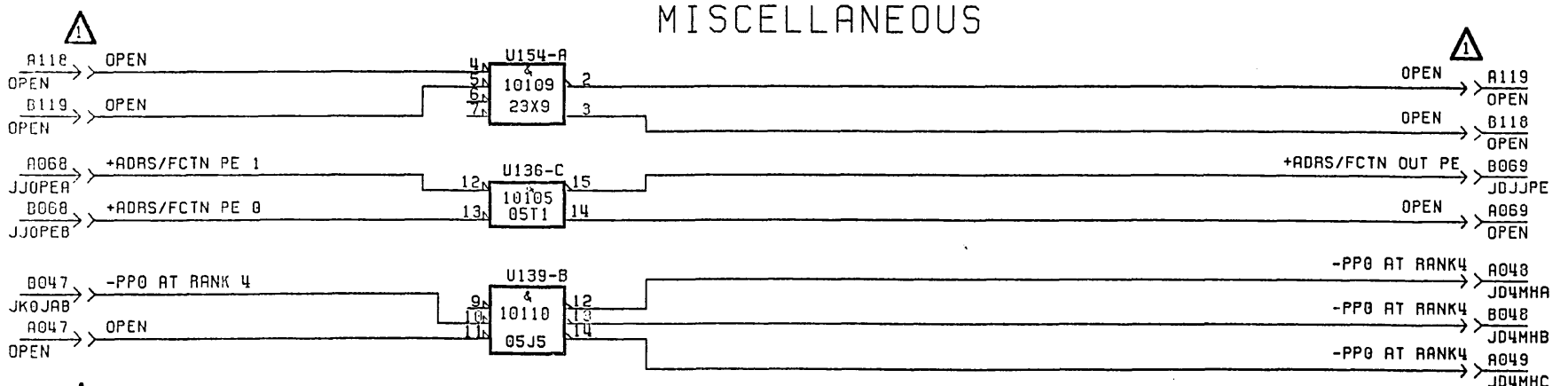
PP COUNT BITS TO ADU RD BOARD



PP COUNT BITS TO ADU WR BOARD



MISCELLANEOUS



- A081 TERM
- OPEN
- B081 TERM
- OPEN
- B080 TERM
- OPEN
- A088 TERM
- OPEN
- B088 TERM
- OPEN
- B089 TERM
- J0C0CRE


MAX LENGTH 12"

NOT TERMINATED AND MAX LENGTH OF 4"

	ADU CONTROL BOARD PP COUNTER		B	DWG NO. 53575503	DATE 11/01/85	REV A
	TYPE 1JDH		SHEET NO. 15	60462210	PAGE	40-15

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	02	-PP0,D5 FULL,BAS 0	27	11	+BBL C0 SELECT
02	02	-PP1,D5 FULL,BAS 0	28	12	+TAG PE
03	02	-PP2,D5 FULL,BAS 0	29	11	+BBL 3 SELECT
04	02	-PP3,D5 FULL,BAS 0	30	11	+BBL C1 SELECT
05	02	-PP4,D5 FULL,BAS 0	31	05	-PP0,D5 FULL,BAS 3
06	13	+READ RESPONSE	32	05	-PP1,D5 FULL,BAS 3
07	12	+ADU RESPONSE	33	05	-PP2,D5 FULL,BAS 3
08	03	-PP0,D5 FULL,BAS 1	34	05	-PP3,D5 FULL,BAS 3
09	03	-PP1,D5 FULL,BAS 1	35	05	-PP4,D5 FULL,BAS 3
10	03	-PP2,D5 FULL,BAS 1	36	06	-PP0,D5 FULL,BAS C0
11	03	-PP3,D5 FULL,BAS 1	37	06	-PP1,D5 FULL,BAS C0
12	03	-PP4,D5 FULL,BAS 1	38	06	-PP2,D5 FULL,BAS C0
13	09	+CENTRAL MEM REQ	39	06	-PP3,D5 FULL,BAS C0
14	14	-CMI BUSY	40	06	-PP4,D5 FULL,BAS C0
15	04	-PP0,D5 FULL,BAS 2	41	13	-RESPONSE CODE PE
16	04	-PP1,D5 FULL,BAS 2	42	08	-T1 CLOCK
17	04	-PP2,D5 FULL,BAS 2	43	07	-PP0,D5 FULL,BAS C1
18	04	-PP3,D5 FULL,BAS 2	44	07	-PP1,D5 FULL,BAS C1
19	04	-PP4,D5 FULL,BAS 2	45	07	-PP2,D5 FULL,BAS C1
20	13	+ADU CTRL BD ERROR	46	07	-PP3,D5 FULL,BAS C1
21	11	+BBL 2 SELECT	47	14	-ANY EXCH ACCEPT
22	11	+BBL 1 SELECT	48	07	-PP4,D5 FULL,BAS C1
23	13	+UNCORRECT WRITE	49	15	+PP COUNT BIT 0
24	11	+BBL 0 SELECT	50	15	+PP COUNT BIT 1
25	13	+REJECT	51	15	+PP COUNT BIT 2
26	13	+UNCORRECT READ			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [NOT USED]
TERM	A003,B003,A004,A008,B008,B009,A019,A020,B020,A021,A026,B026,A032,B032,A037,B037,B080,A081,B081,A088,B088,B089
UNUSED	A009,B038,B041,A043,A086,A091,B091,A092,B092,A093,B093,A094,B094,A095,A098,B098,A099,B099,A100,A104,B104,A105,A114,B114,A115,B115,B128

	ADU CONTROL BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JDH		B	DWG NO. 53575503	DATE 11/01/85	REV A
	SHEET NO. 16		60462210		PAGE 10-16	

CAUTION


There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

ADU WRITE BOARD

[illegible]

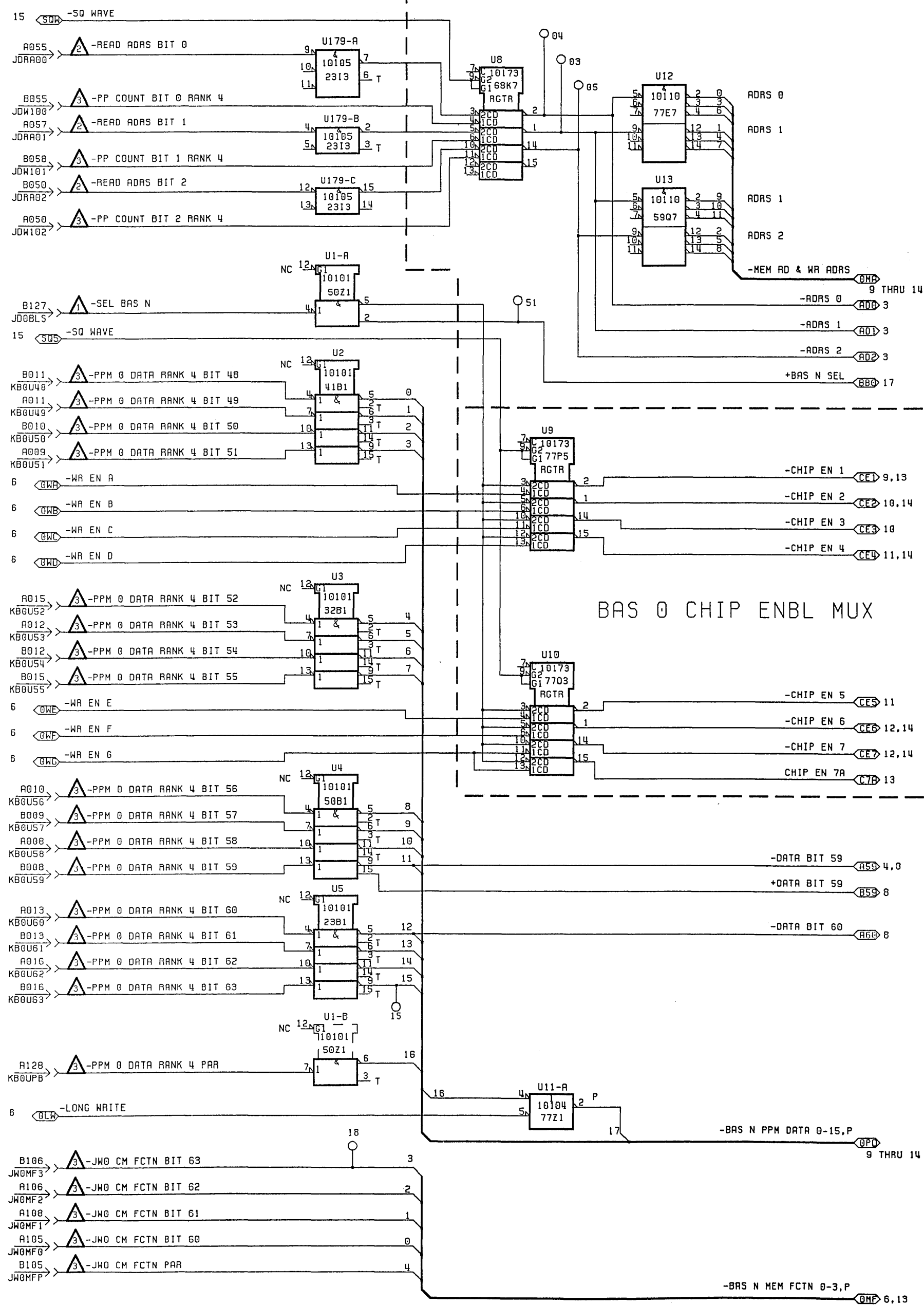
LOC: A14, A13, A12

DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	W E DIEHART	12/05/85
PUBS	R K BONDE	12/05/85
APP	W E DIEHART	12/05/85


 CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575504	DATE 06/17/87	REV C
	TYPE 1JEH/1JVH	SHEET NO. 1	60462210	PAGE 1	OF 01

DATA, FCTN, AND BAS N SEL F/O

ADRS MUX & BAS N ADRS F/O

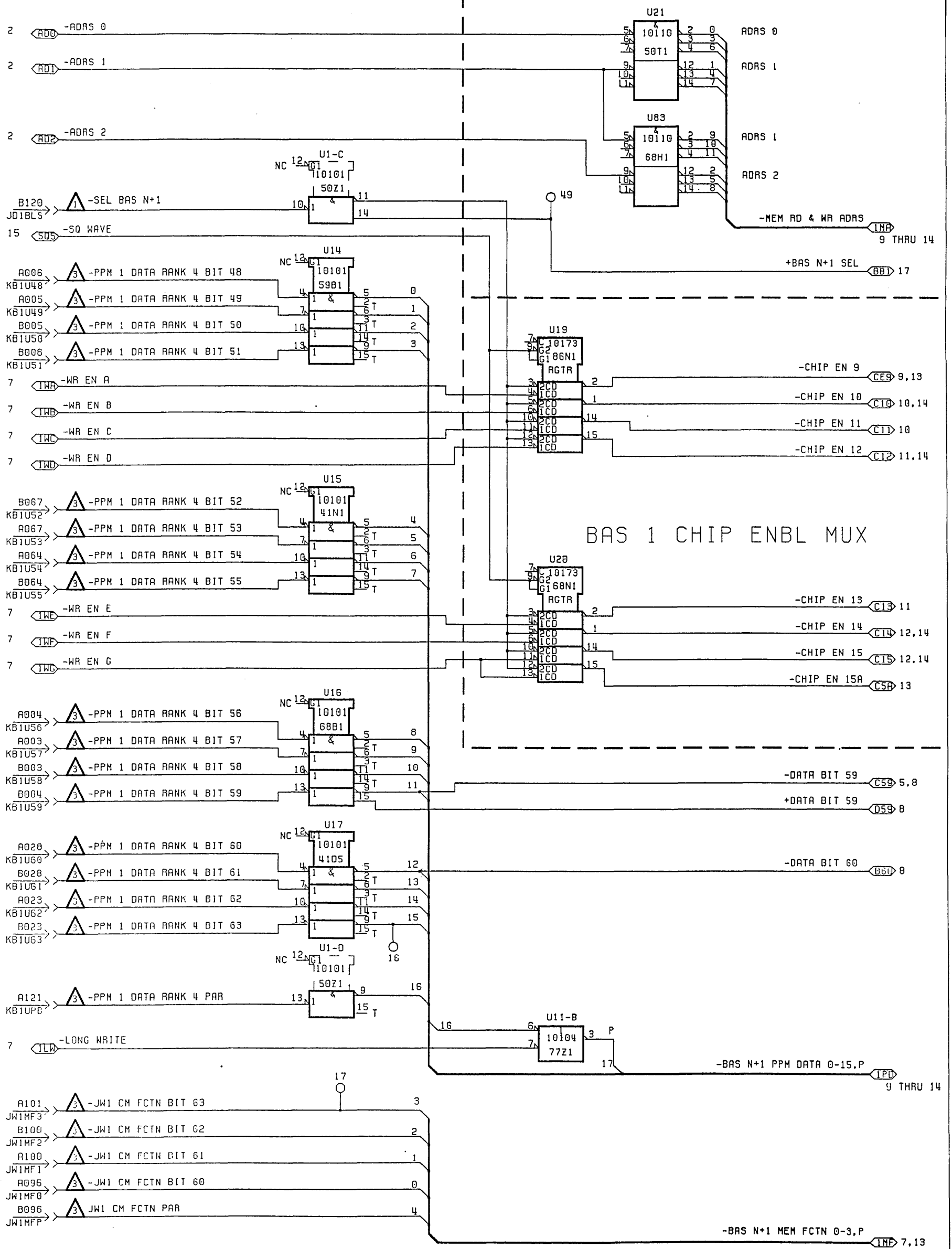


- 1 NOT TERMINATED AND MAX LENGTH 4"
- 2 GROUPED TERMINATION AND MAX LENGTH 4"
- 3 MAX LENGTH 12"

 CONTROL DATA	ADU WRITE BOARD		B	DWG NO.	DATE	REV	
	BAS N FCTN, PPM DATA, CHIP EN.			53575504	11/01/85	A	
	READ & WRITE ADDRESS F/O						
TYPE 1JEH/1JVH		N	SHEET NO.	2	60462210	PAGE	IF-02

DATA, FCTN, AND
BAS N+1 SEL F/O

BAS N+1 ADRS F/O



1 NOT TERMINATED AND MAX LENGTH 4"

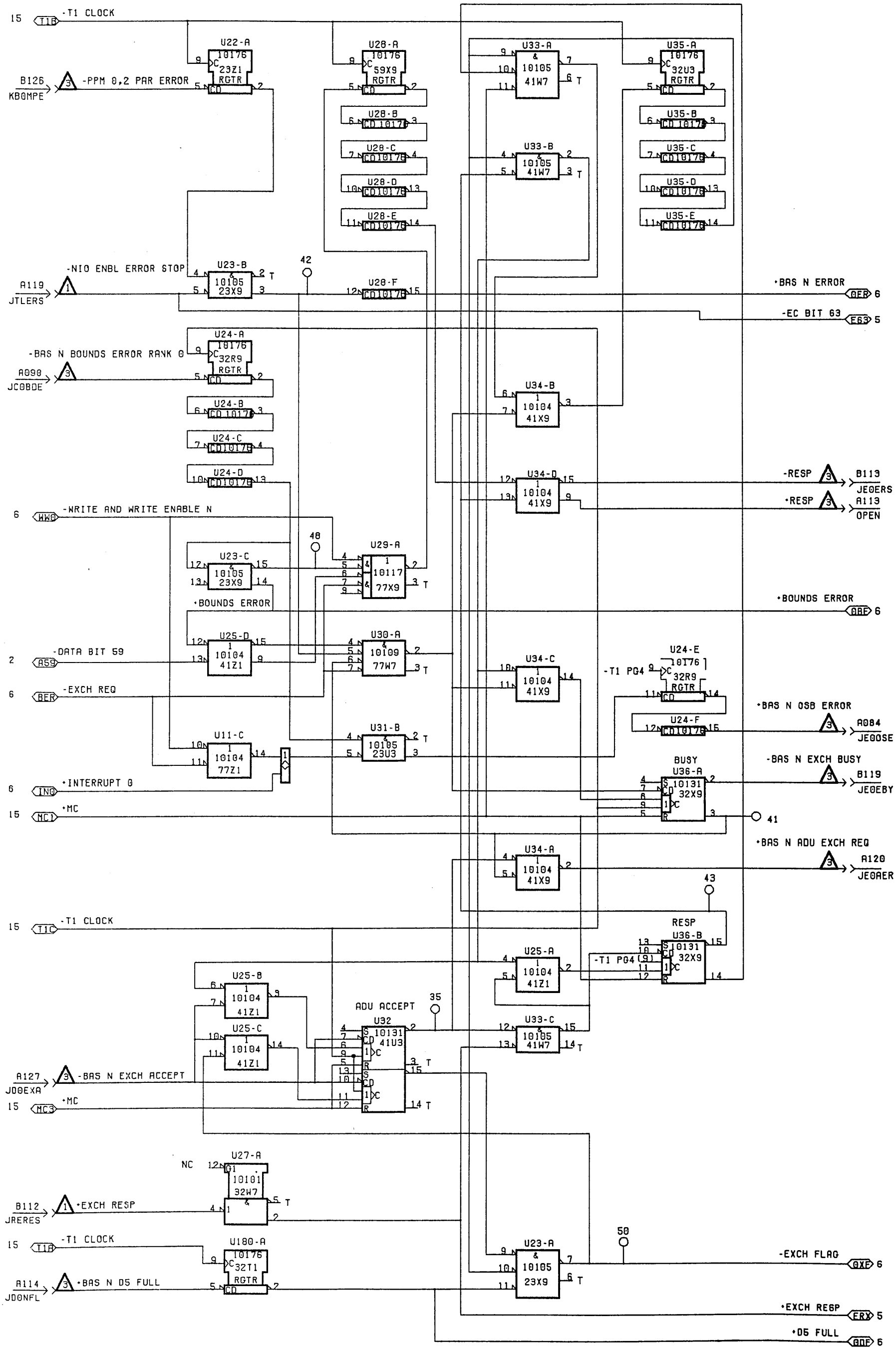
3 MAX LENGTH 12"



ADU WRITE BOARD
BAS N+1 FCTN, PPM DATA, CHIP EN,
READ & WRITE ADDRESS F/O
TYPE 1JH/1JVH

DWG NO.	DATE	REV
8	53575504	11/01/85
SHEET NO. 3	60462210	PAGE 10

BAS N EXCH REQ LOGIC



1 NOT TERMINATED AND MAX LENGTH 4"

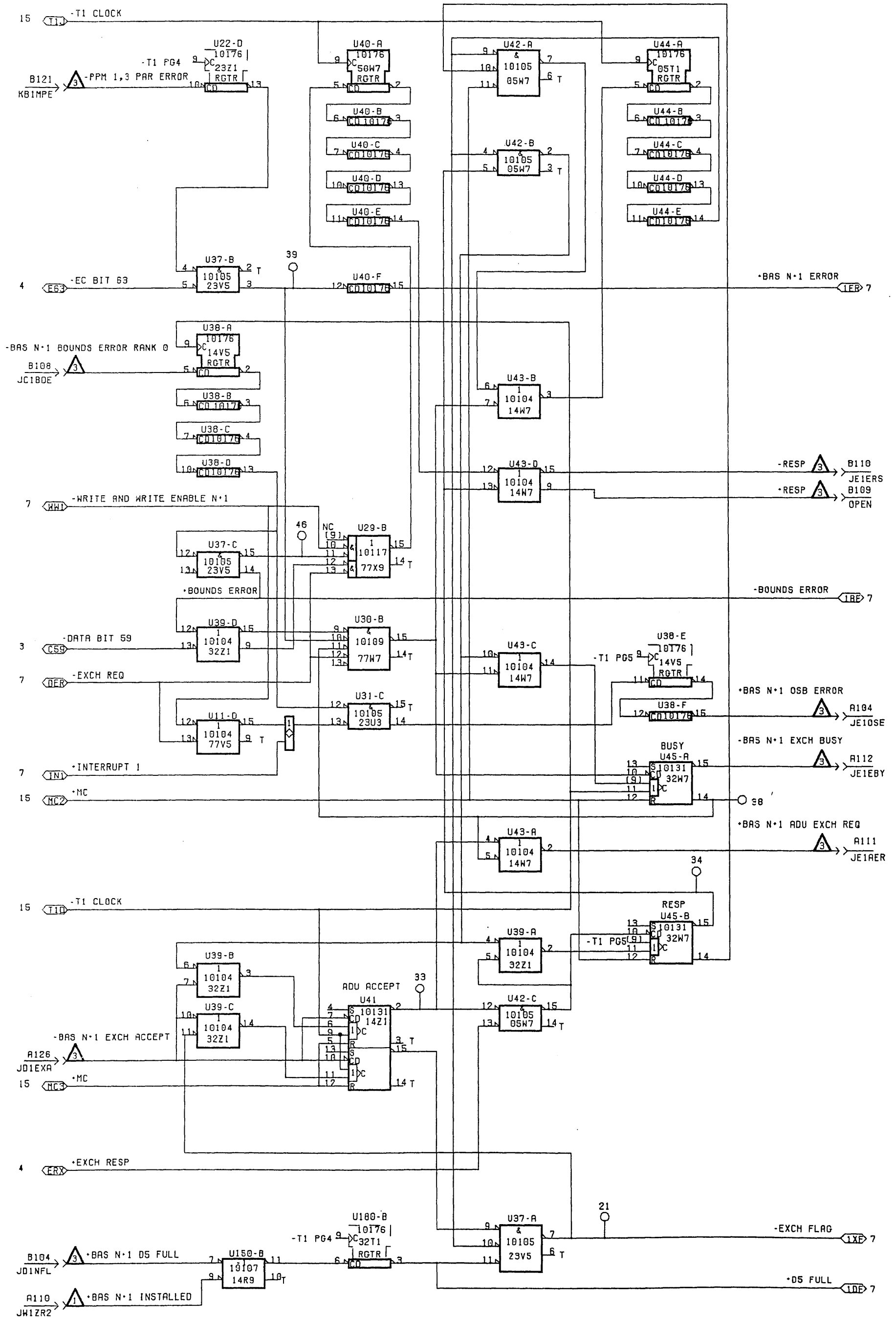
3 MAX LENGTH 12"



ADU WRITE BOARD
BAS N EXCHANGE REQUEST
TYPE 1JEH/1JVH

B	DWG NO. 53575504	DATE 06/17/87	REV C
SHEET NO. 4		60462210	PAGE JE-04

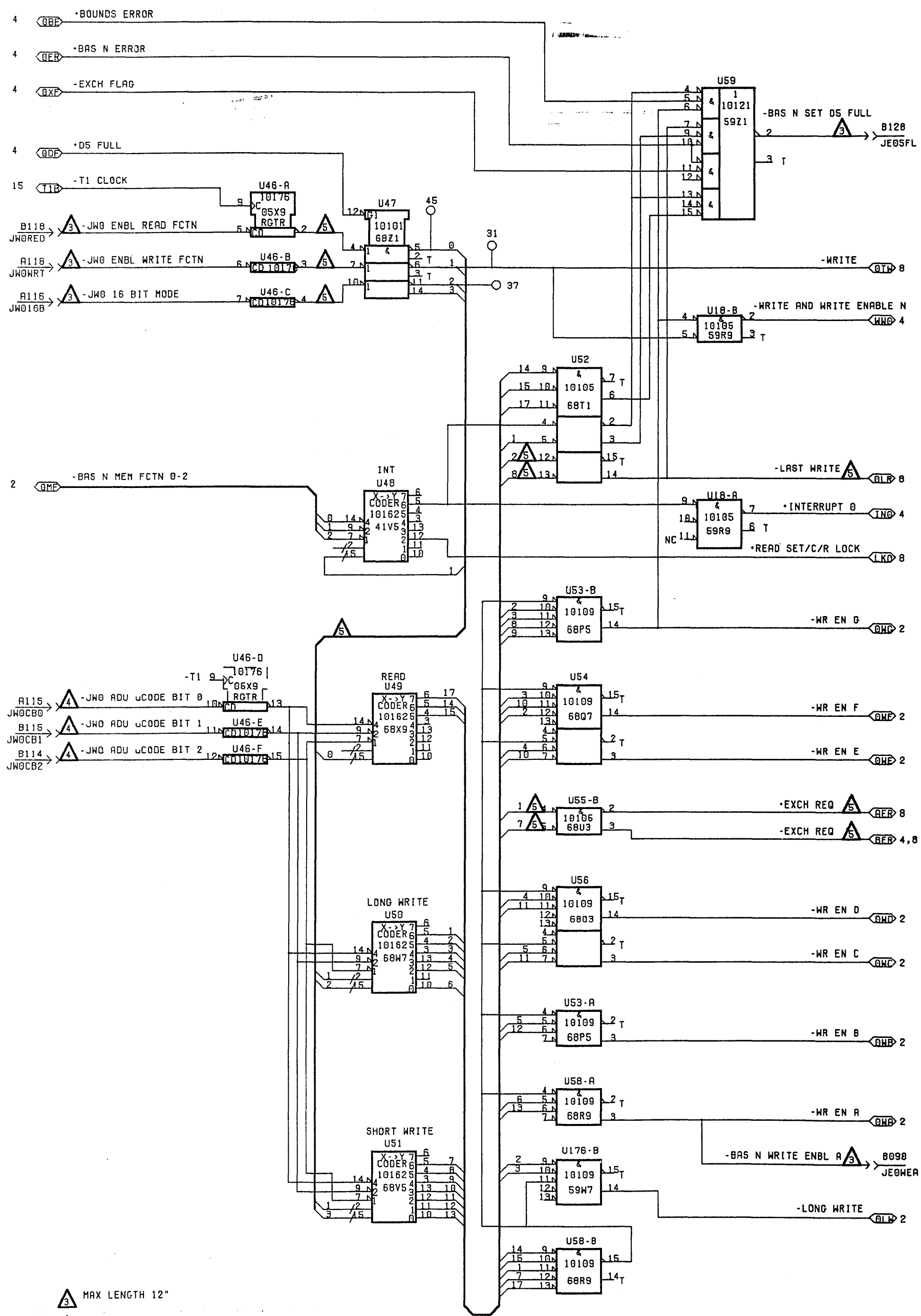
BAS N+1 EXCH REQ LOGIC







DO NOT TERMINATE AND MAX LENGTH 4"
MAX LENGTH 12"

	ADU WRITE BOARD BAS N+1 EXCHANGE REQUEST		DWG NO. 53575504	DATE 06/17/87	REV C
	TYPE 1JEH/1JVH		SHEET NO. 6	60462210	PAGE 05

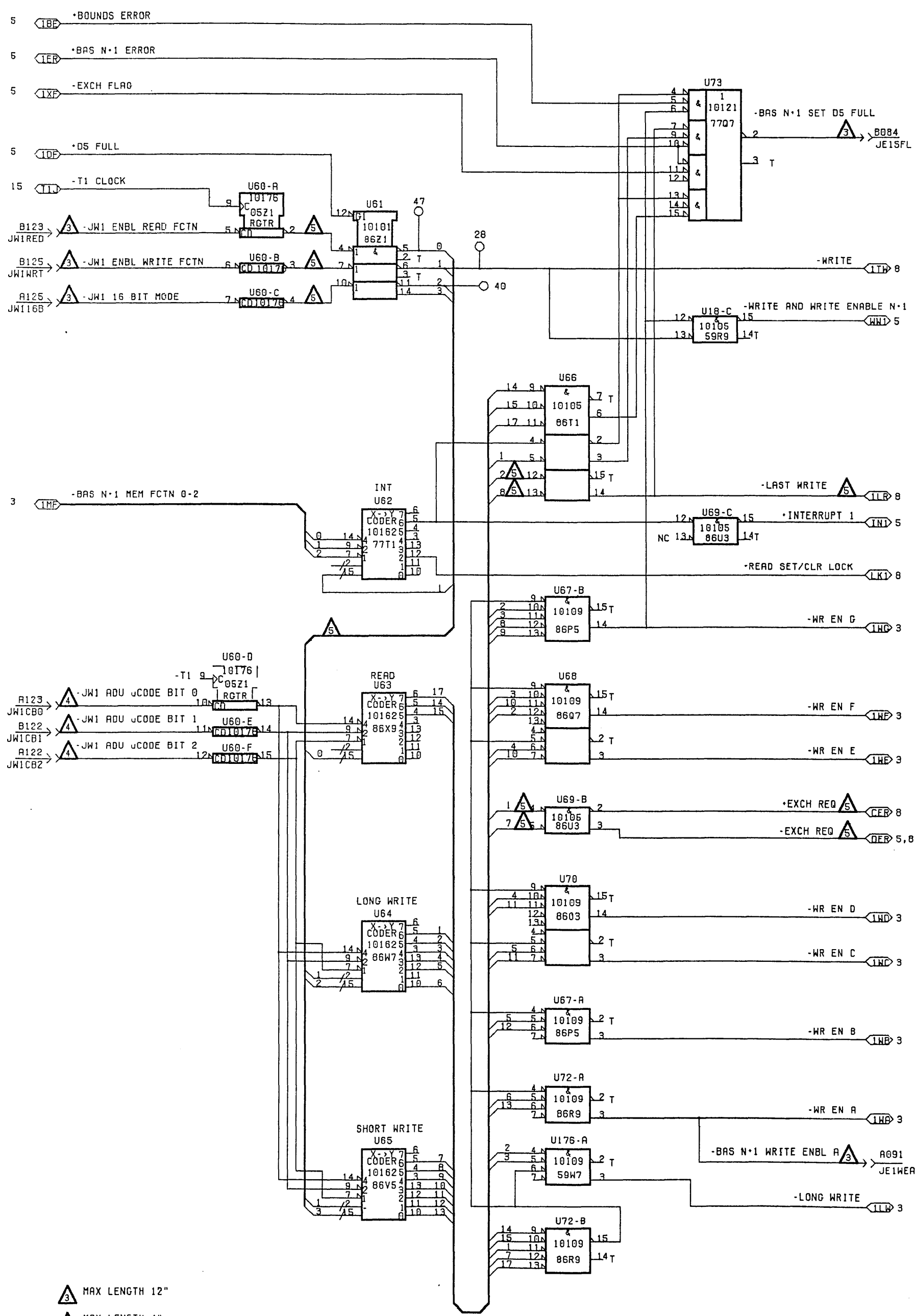
BAS N WRITE ENBLS AND EXCH REQ




 MAX LENGTH 12"
 MAX LENGTH 4"
 MAX LENGTH 6"

 CONTROL DATA	ADU WRITE BOARD BAS N WRITE ENABLE AND EXCHANGE REQUEST F/O TYPE 1JEH/1JVH		B	DWG NO. 53575504	DATE 06/17/87	REV C
	SHEET NO. 6		60462210		PAGE	JE-06

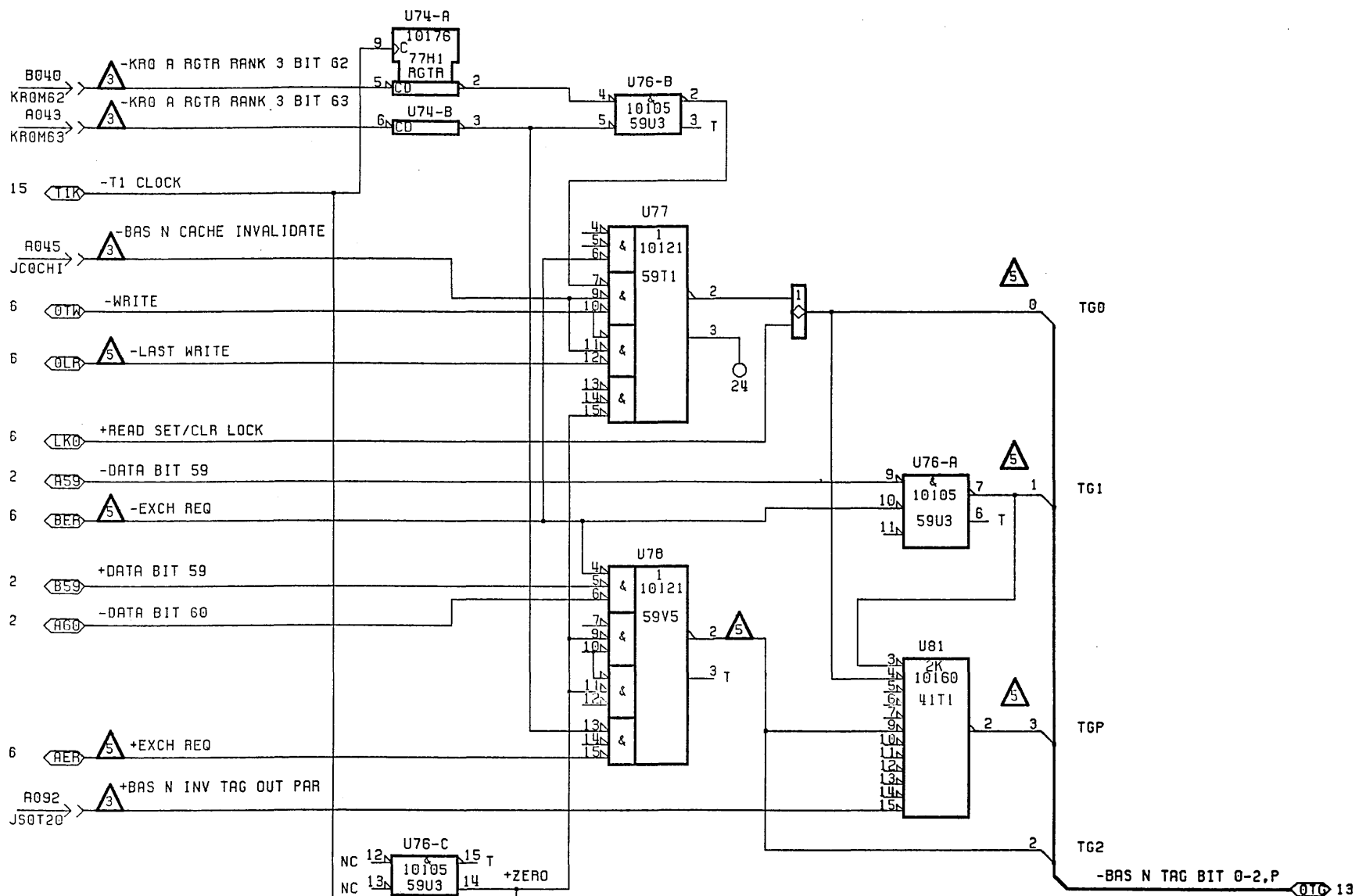
BAS N+1 WRITE ENBLS AND EXCH REQ



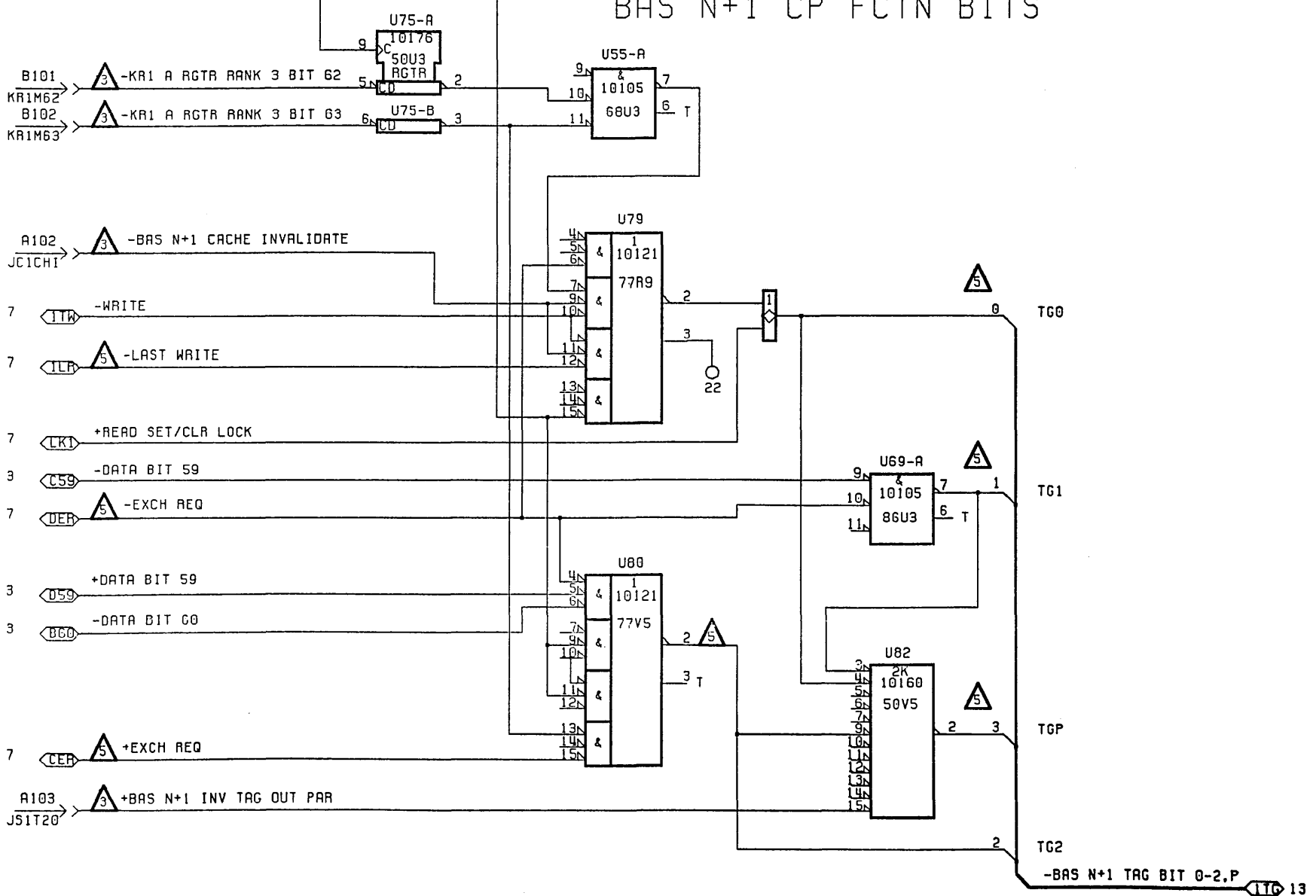
- MAX LENGTH 12"
- MAX LENGTH 4"
- MAX LENGTH 6"

 CONTROL DATA	ADU WRITE BOARD BAS N-1 WRITE ENABLE AND EXCHANGE REQUEST F/O TYPE 1JH/JVH	N	B	DWG NO.	DATE	REV
				53575504	06/17/87	C
			SHEET NO.	7	60462210	PAGE

BAS N CP FCTN BITS



BAS N+1 CP FCTN BITS

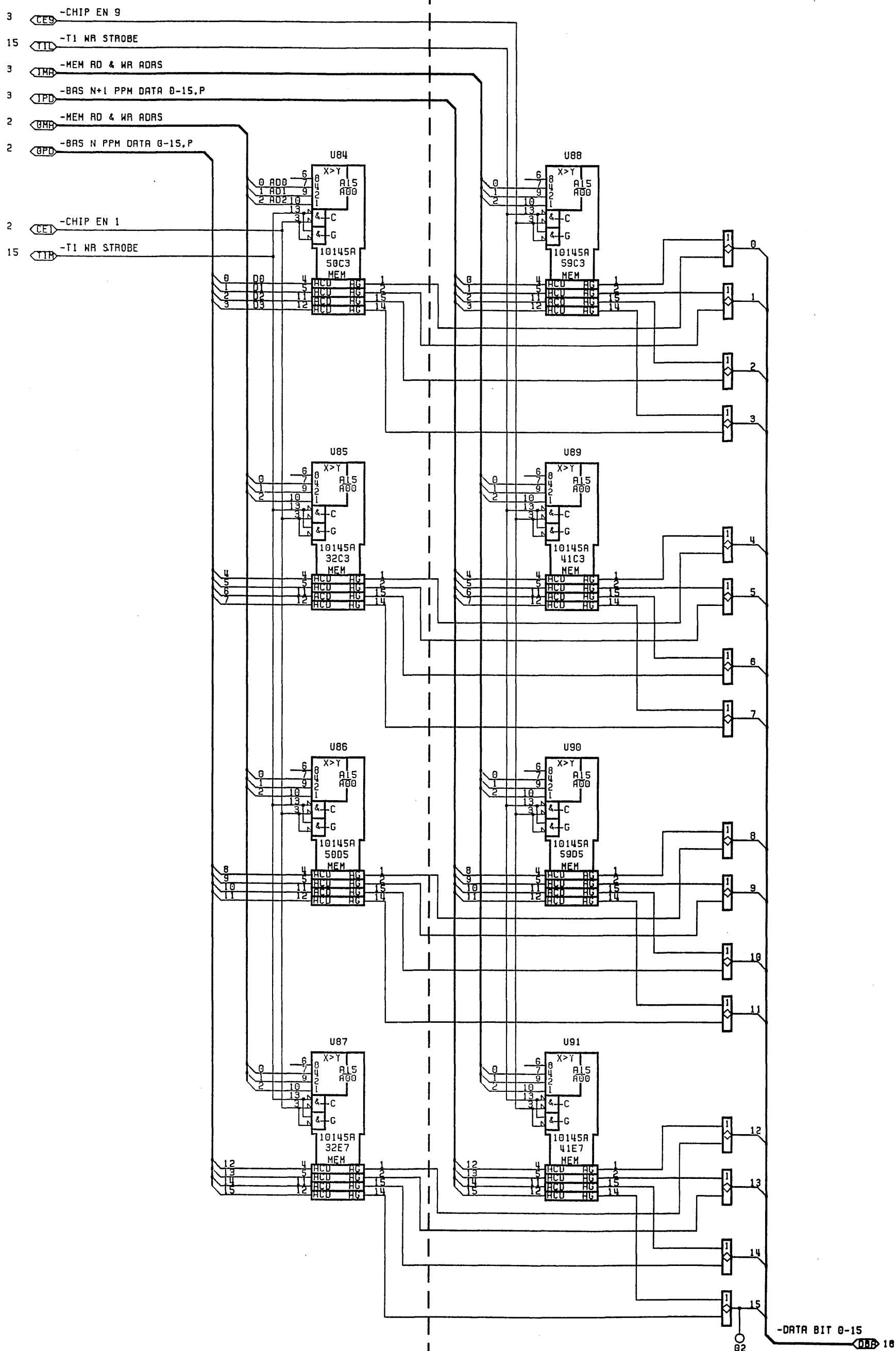


3 MAX LENGTH 12"
 5 MAX LENGTH 6"

	ADV WRITE BOARD BAS N & N+1 CP FUNCTION BITS		DWG NO. 53575504	DATE 11/01/85	REV A
	TYPE 1JEH/1JVH	SHEET NO. 8	60462210	PAGE	JE-08

BAS N ASSY RGTR BITS 0-15

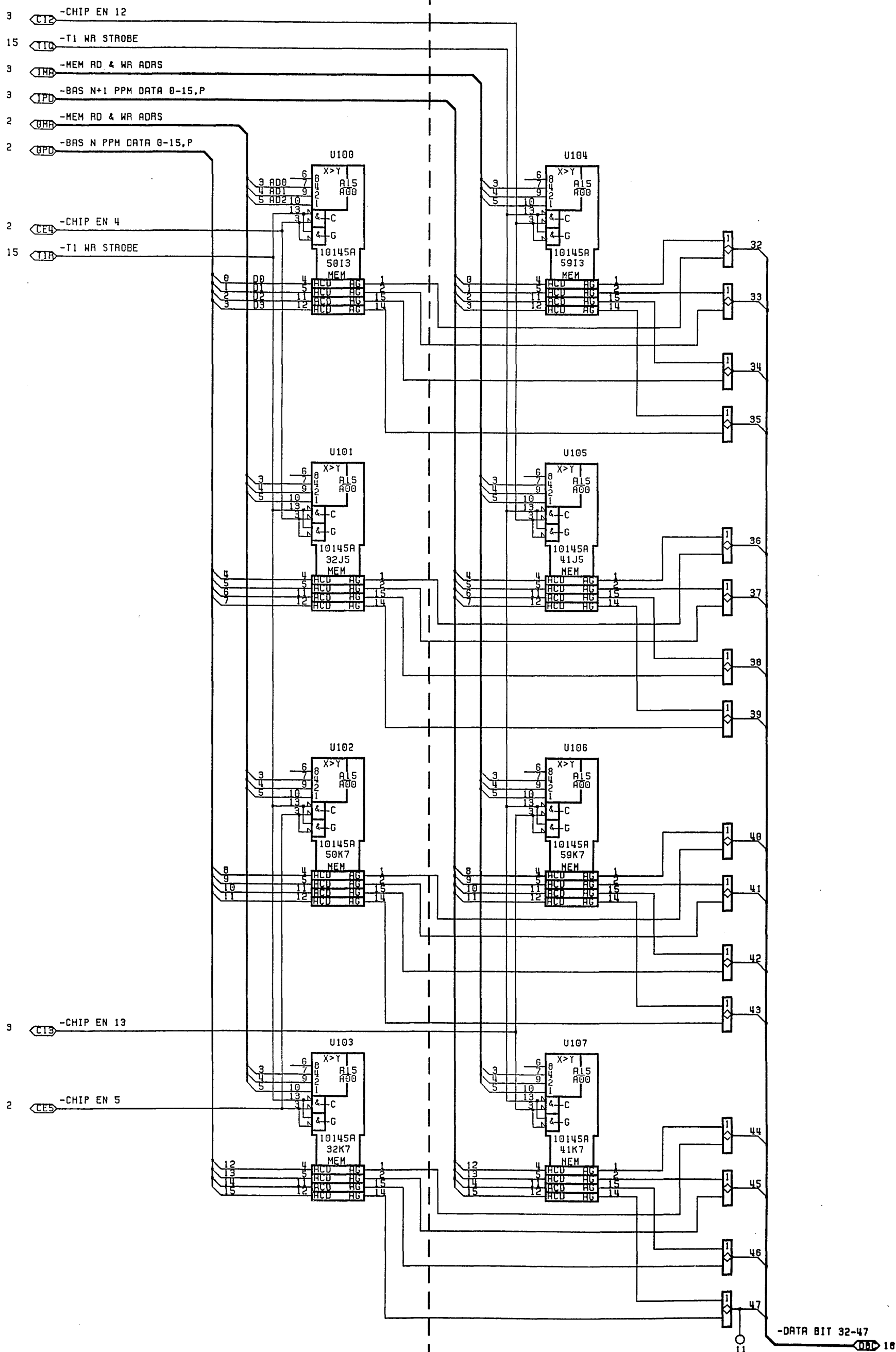
BAS N+1 ASSY RGTR BITS 0-15



	ADU WRITE BOARD		DWG NO.	DATE	REV
	ASSY RGTR BAS N AND N+1		B	53575504	11/01/85
DATA BITS 0-15		SHEET NO.	9	60462210	PAGE
TYPE 1JEH/1JVH		JF-09			

BAS N ASSY RGTR BITS 32-47

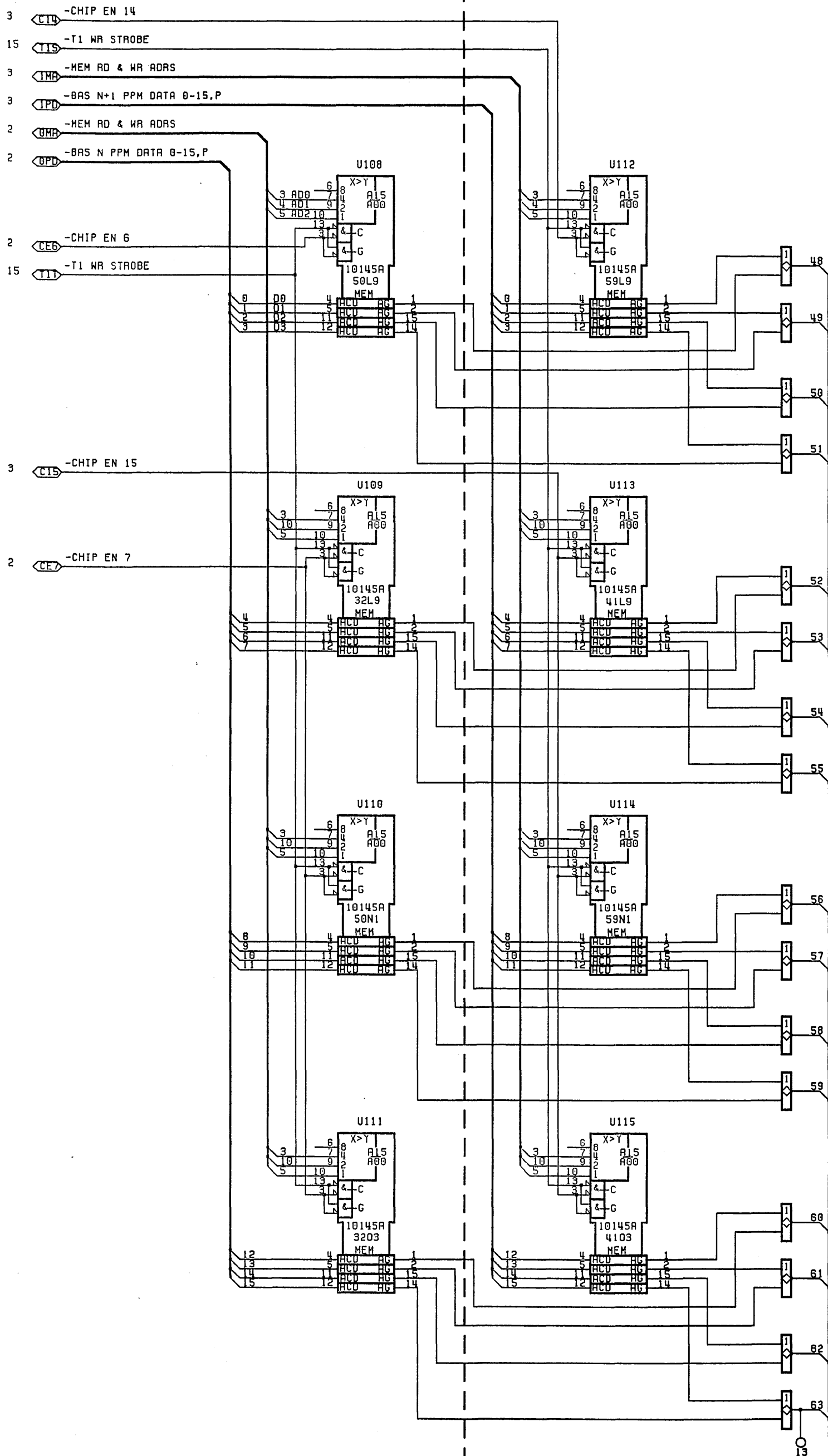
BAS N+1 ASSY RGTR BITS 32-47




	ADU WRITE BOARD		DWG NO.	DATE	REV
	ASSY RGTR BAS N AND N+1		B	53575504	11/01/85
	DATA BITS 32-47		SHEET NO. 11	60462210	PAGE 11
TYPE 1JEH/1JVH					

BAS N ASSY RGTR BITS 48-63

BAS N+1 ASSY RGTR BITS 48-63

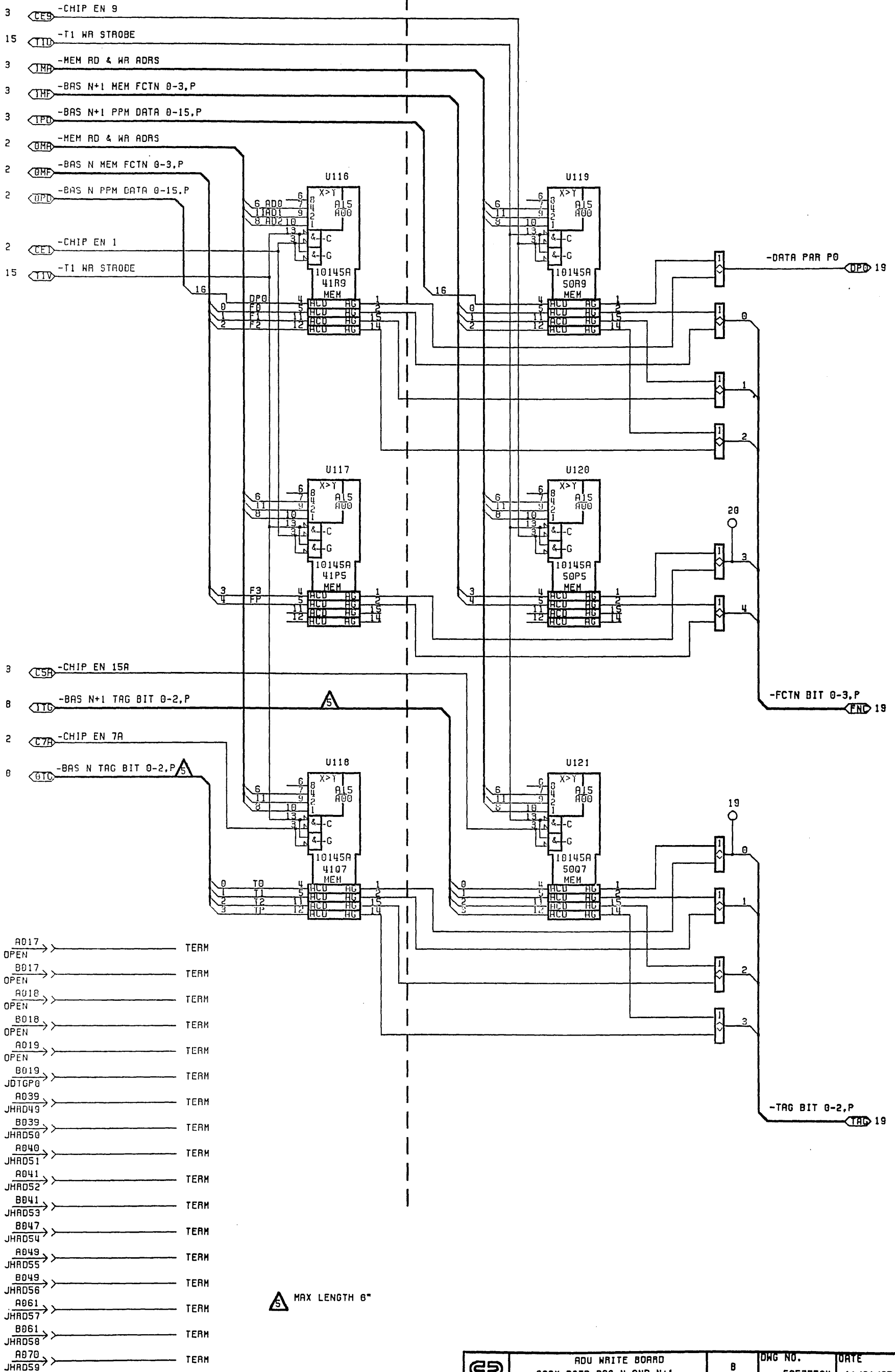


-DATA BIT 48-63
DAD 19

 CONTROL DATA	ADU WRITE BOARD		B	DWG NO.	DATE	REV
	ASSY RGTR BAS N AND N+1			53575504	11/01/85	A
	DATA BITS 48-63					
	TYPE 1JEH/1JVH					
	N		SHEET NO. 12	60462210	PAGE	E-12

BAS N ASSY RGTR PAR BIT 0,FCTN,TAG

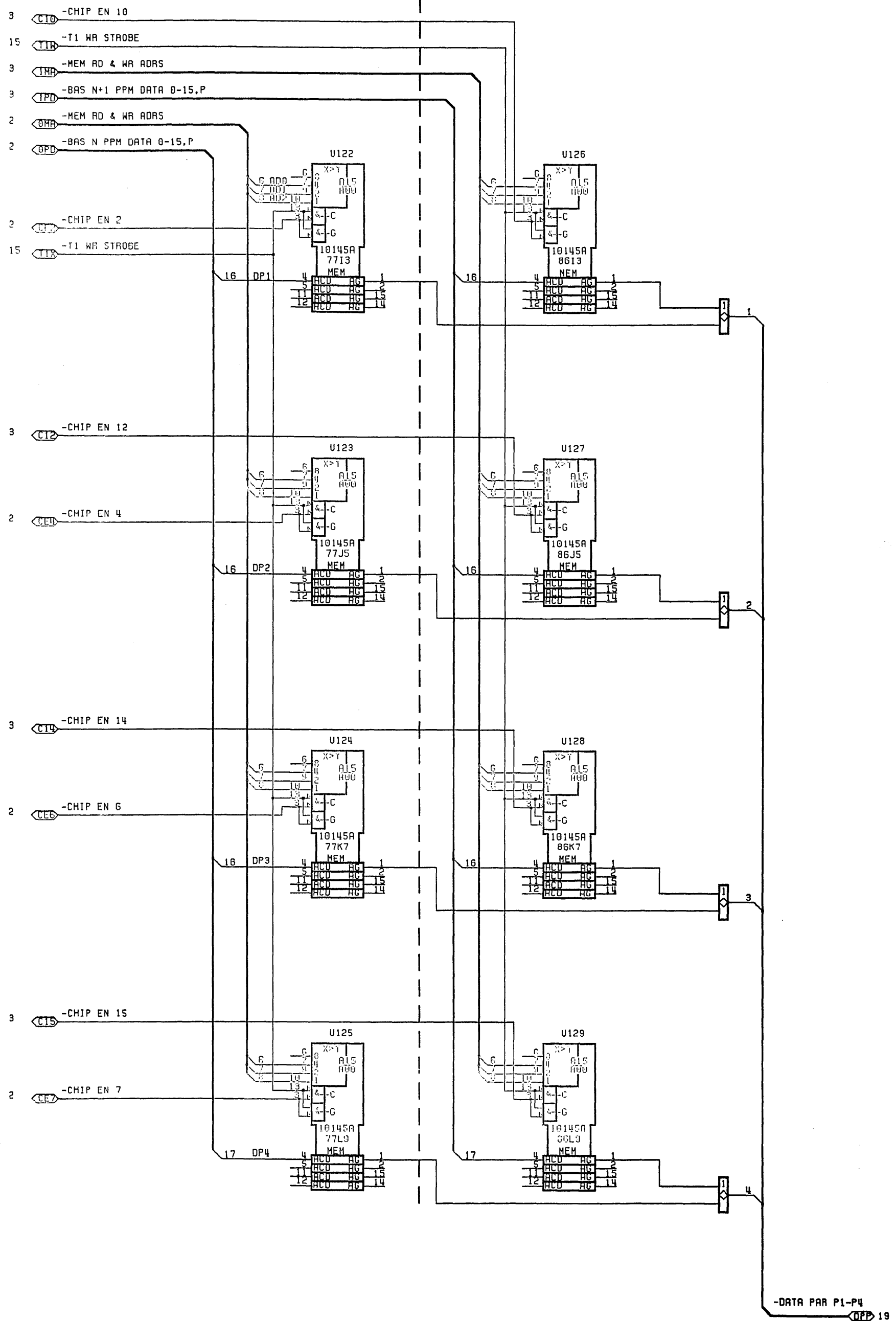
BAS N+1 ASSY RGTR PAR BIT 0,FCTN,TAG



	ADU WRITE BOARD		DWG NO.	DATE	REV
	ASSY RGTR BAS N AND N+1		8	53575504	11/01/85
CONTROL DATA	DATA P0, FCTN 0-3,P & TAG 0-2,P		SHEET NO. 13	60462210	PAGE
	TYPE 1JEH/1JVH		N	JE-19	

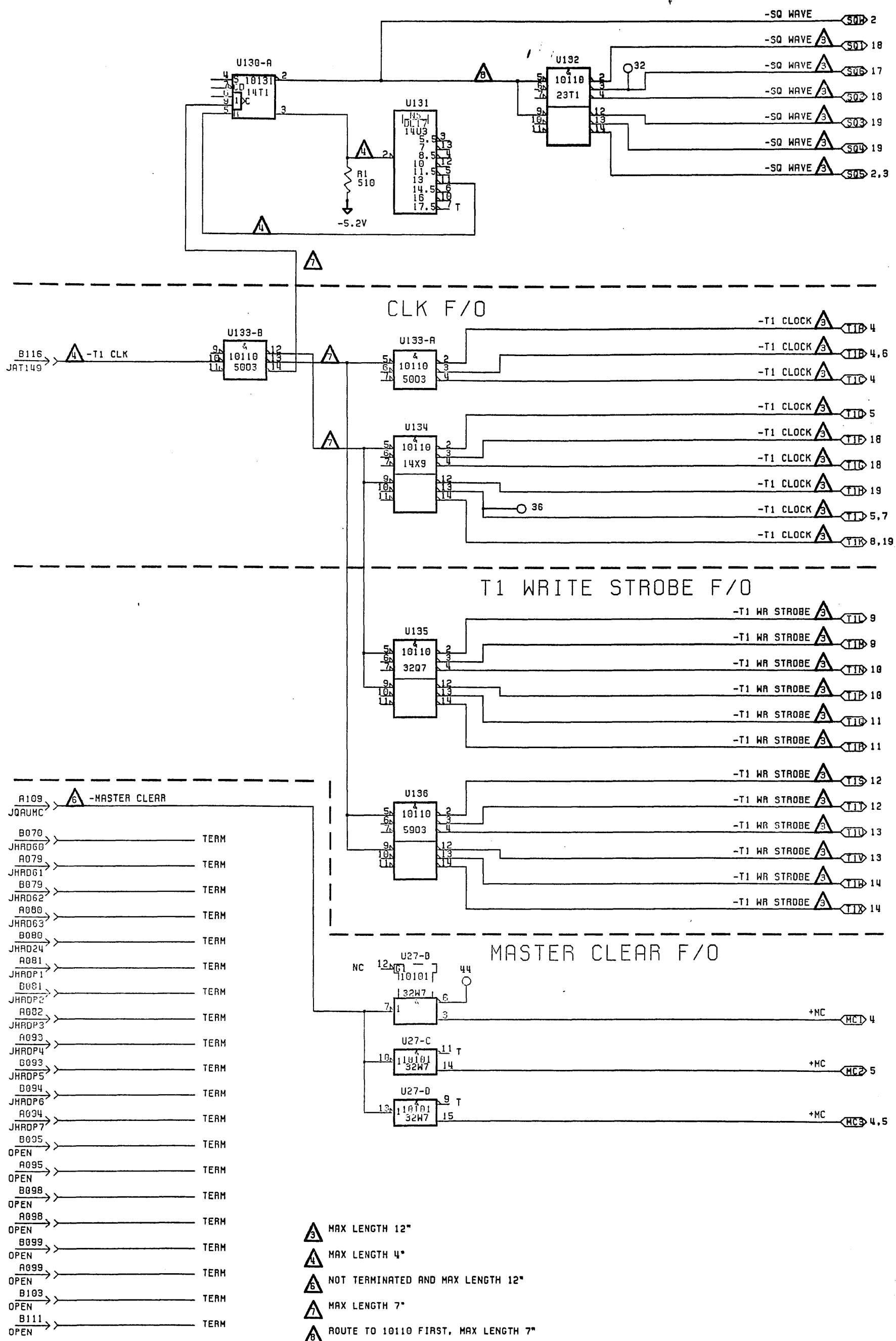
BAS N ASSY RGTR PAR BITS 1-4

BAS N+1 ASSY RGTR PAR BITS 1-4

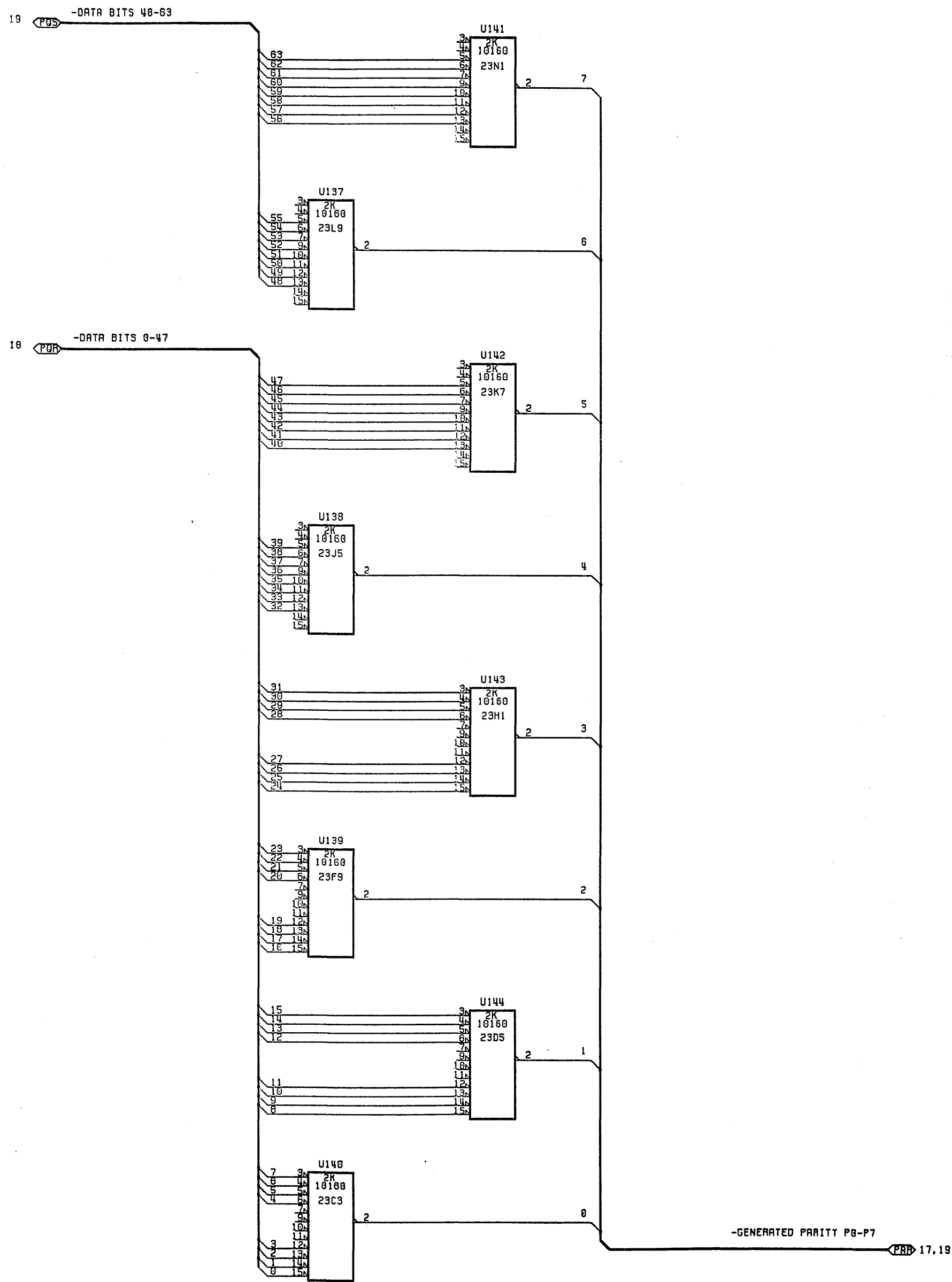


	ADU WRITE BOARD ASSY RGTR BAS N AND N+1 DATA PARITY P1-P4 TYPE 1JEH/1JVH		DWG NO. 53575504	DATE 11/01/85	REV A
	SHEET NO. 14	60462210	PAGE JE-14		

SQ WAVE GEN

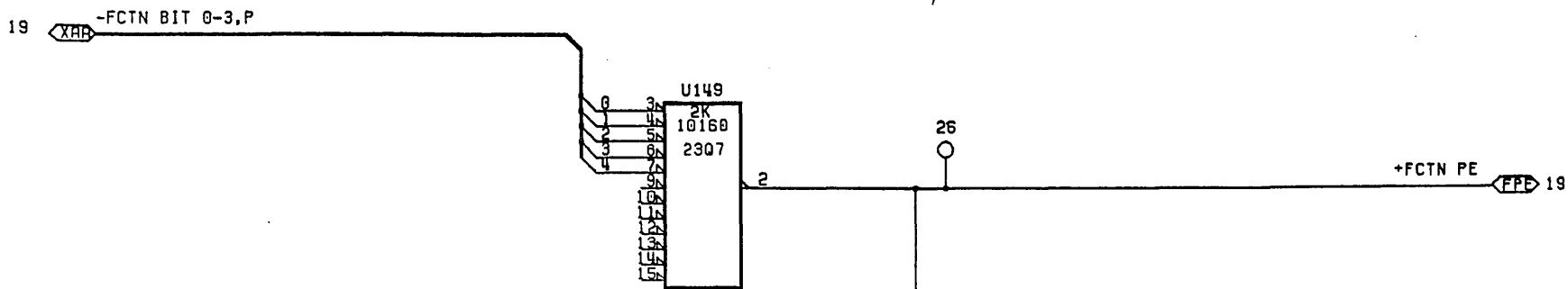


DATA PAR GEN

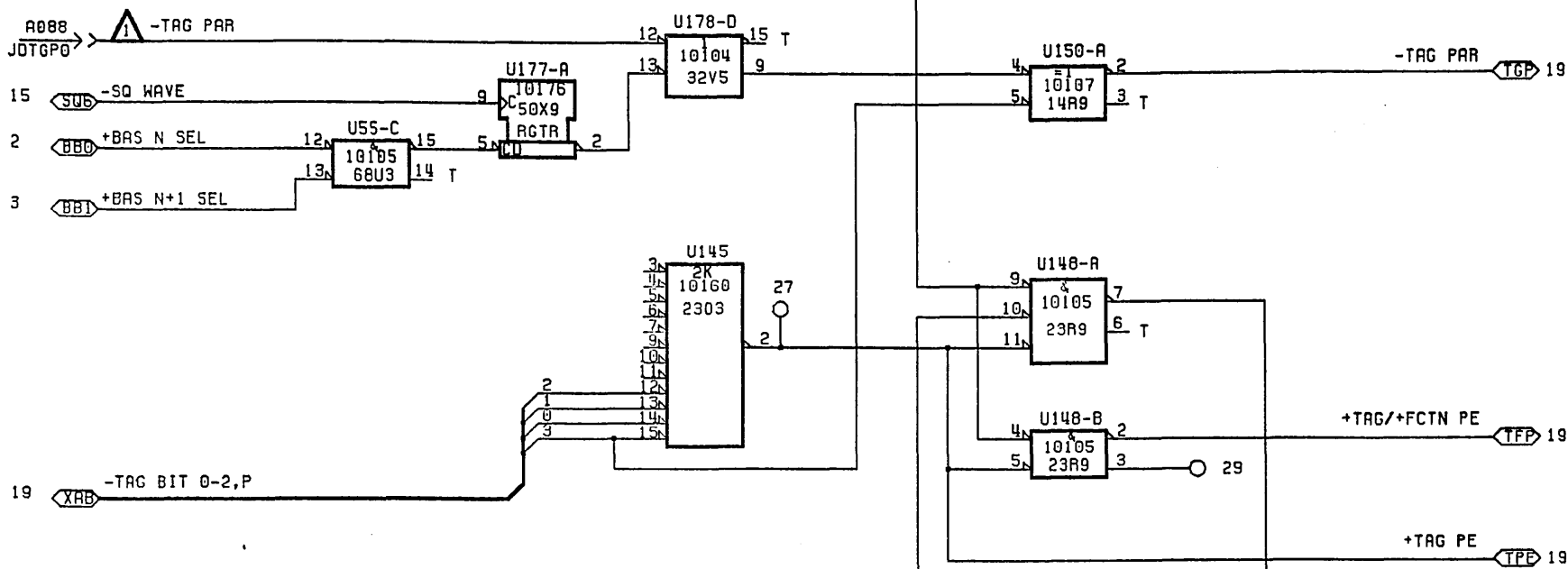


CD CONTROL DATA	ADU WRITE BOARD DATA PARITY GENERATE P0-P7		DWG NO. B 53575504	DATE 11/01/85	REV A
	TYPE 1JEH/1JVH		SHEET NO. 16	60462210	PAGE JE-16
			N		

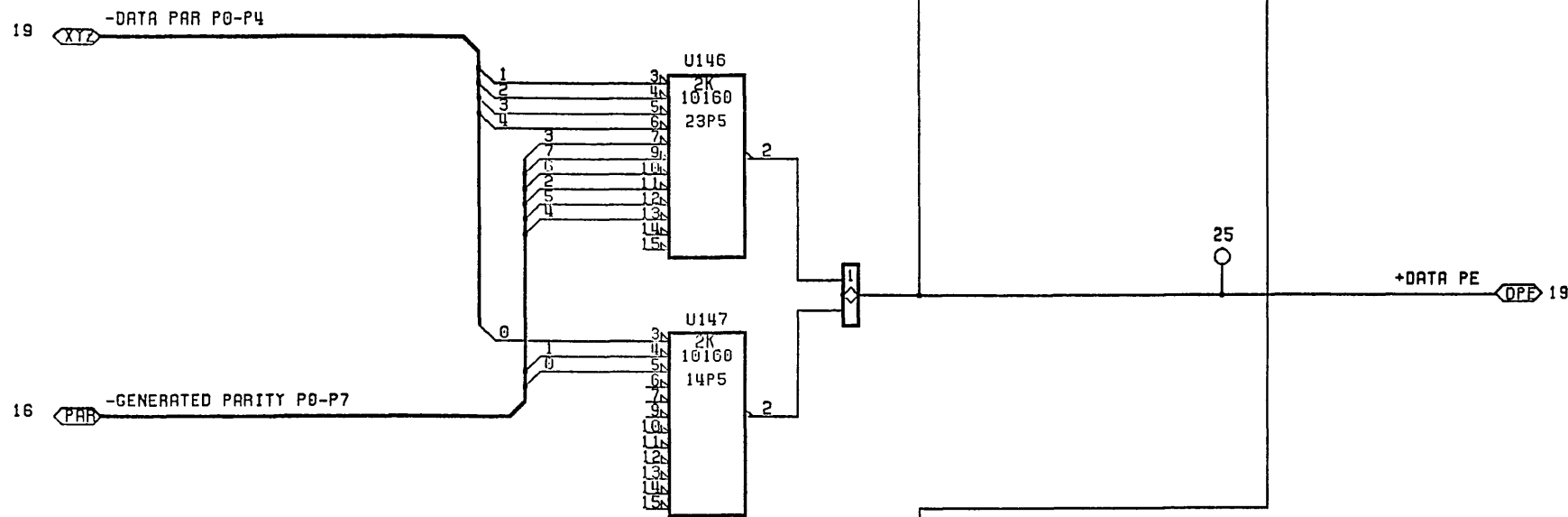
FCTN PAR CHECKER



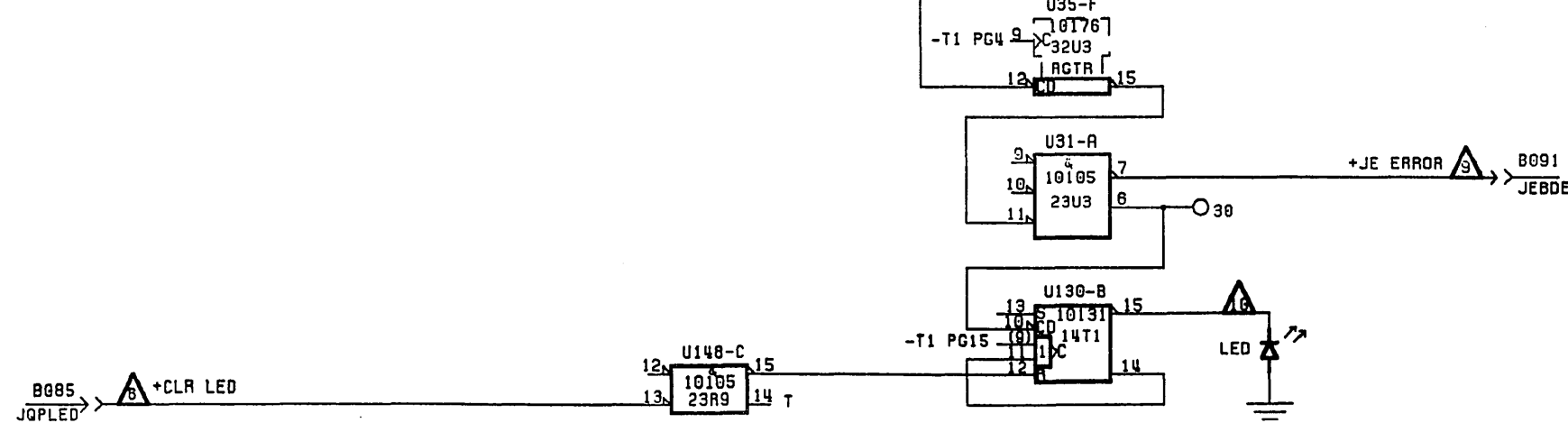
TAG PAR CHECKER AND GEN




DATA PAR CHECKER



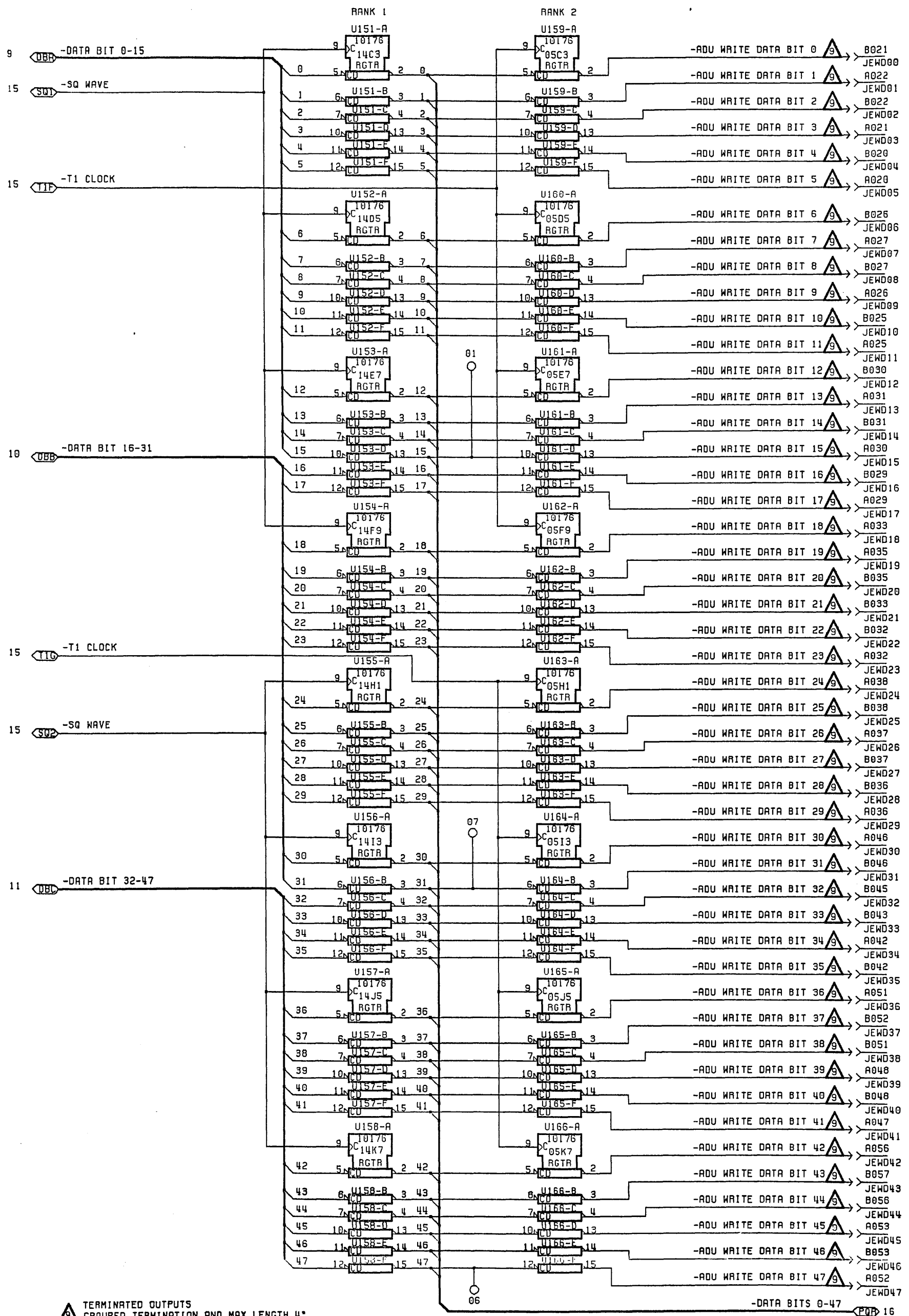
BOARD ERROR



- NOT TERMINATED AND MAX LENGTH 4"
- NOT TERMINATED AND MAX LENGTH 12"
- TERMINATED OUTPUT GROUPED TERMINATION AND MAX LENGTH 4" NOT TERMINATED ON THE 1JVH BOARD
- TERMINATED

 CONTROL DATA	ADU WRITE BOARD DATA, FCTN AND TAG PAR CHECKERS AND BOARD ERROR TYPE 1JEH/1JVH	B	DWG NO.	DATE	REV
			53575504	11/01/85	A
			SHEET NO. 17		

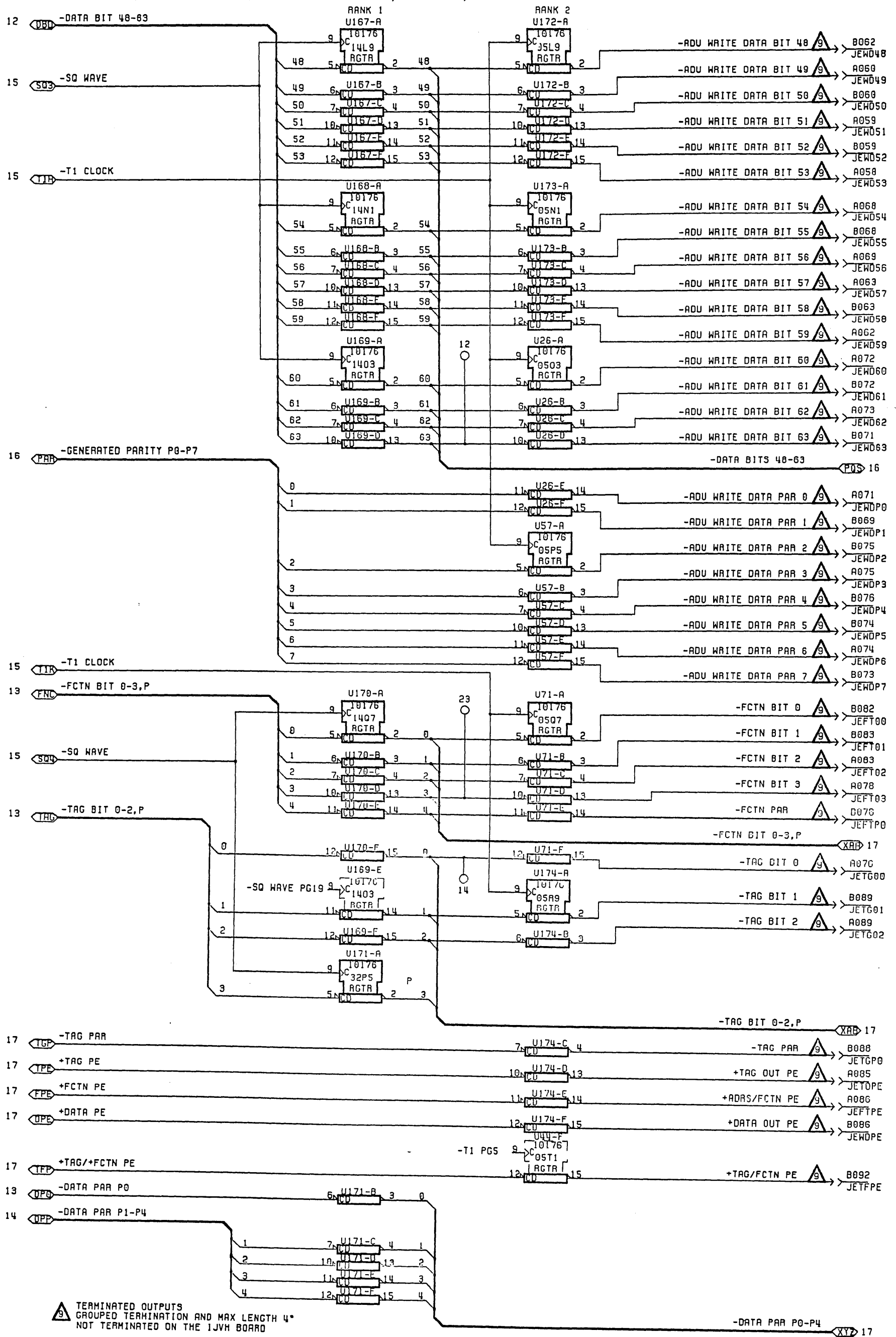
OUT RGTR BITS 0-47




ADU WRITE BOARD
OUTPUT REGISTER
DATA BITS 0-47
TYPE 1JEH/1JVH

DWG NO.	DATE	REV
8	53575504	11/01/85
SHEET NO. 18	60462210	PAGE 18

OUT RGTR BITS 48-63, PAR, FCTN & TAG




9 TERMINATED OUTPUTS
GROUPED TERMINATION AND MAX LENGTH 4"
NOT TERMINATED ON THE 1JVB BOARD

 CONTROL DATA	ADU WRITE BOARD OUTPUT REGISTER FOR DATA, PAR, FCTN AND TAG TYPE 1JEH/1JVH	B	DWG NO.	DATE	REV
			53575504	11/01/85	A
SHEET NO. 19		60462210		PAGE 19	

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	18	-DATA BT 15 OUT REG	27	17	+TAG PAR ERROR
02	09	-DATA BT 15 ASY REG	28	07	-BAS N+1 WRITE BIT
03	02	-RD/WRT ADRS BIT 1	29	17	-TAG/FCTN PAR ERROR
04	02	-RD/WRT ADRS BIT 0	30	17	-BOARD ERROR
05	02	-RD/WRT ADRS BIT 2	31	06	-BAS N WRITE BIT
06	18	-DATA BT 47 OUT REG	32	15	-SQUARE WAVE
07	18	-DATA BT 31 OUT REG	33	05	-BAS N+1 ADU EX ACPT
08	10	-DATA BT 31 ASY REG	34	05	-BAS N+1 EX RESPON
09			35	04	-BAS N ADU EX ACCEPT
10			36	15	-T1 CLOCK
11	11	-DATA BT 47 ASY REG	37	06	-BAS N 16 BIT WRITE
12	19	-DATA BT 63 OUT REG	38	05	-BAS N+1 EX BUSY
13	12	-DATA BT 63 ASY REG	39	05	+BAS N+1 PPM PAR ERR
14	19	-TAG BIT 0 OUT REG	40	07	-BAS N+1 16 BIT WRT
15	02	-BAS N PPM 0 BIT 63	41	04	-BAS N EX BUSY
16	03	-BAS N+1 PPM 1 BT63	42	04	+BAS N PPM PAR ERR
17	03	-BAS N+1 MEM FN BT3	43	04	-BAS N EX RESP
18	02	-BAS N MEM FN BT 3	44	15	-MASTER CLEAR
19	13	-TAG BIT 0 ASY REG	45	06	-BAS N READ BIT
20	13	-FCTN BIT 3 ASY REG	46	05	-BAS N+1 BOUNDS ERR
21	05	-BAS N+1 EXCH FLAG	47	07	-BAS N+1 READ BIT
22	08	-BAS N+1 TAG BIT 0	48	04	-BAS N BOUNDS ERR
23	19	-FCTN BIT 3 OUT REG	49	03	+BAS N+1 SELECT
24	08	-BAS N TAG BIT 0	50	04	-BAS N EX FLAG
25	17	+DATA PAR ERROR	51	02	+BAS N SELECT
26	17	+FCTN PAR ERROR			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 (USED FOR TERMINATION)
TERM	A017,B017,A018,B018,A019,B019,A039,B039,A040,A041,B041,B047,A049,B049,A061,B061,A070,B070,A079,B079,A080,B080,A081,B081,A082,A093,B093,A094,B094,A095,B095,A098,B098,A099,B099,B103,B111
UNUSED	NONE

	ADU WRITE BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JEH/1JVH	B	DWG NO. 53575504	DATE 11/01/85	REV A
		SHEET NO. 20	60462210	PAGE	JE-20

CAUTION


There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

ADU WRITE BOARD

[illegible]

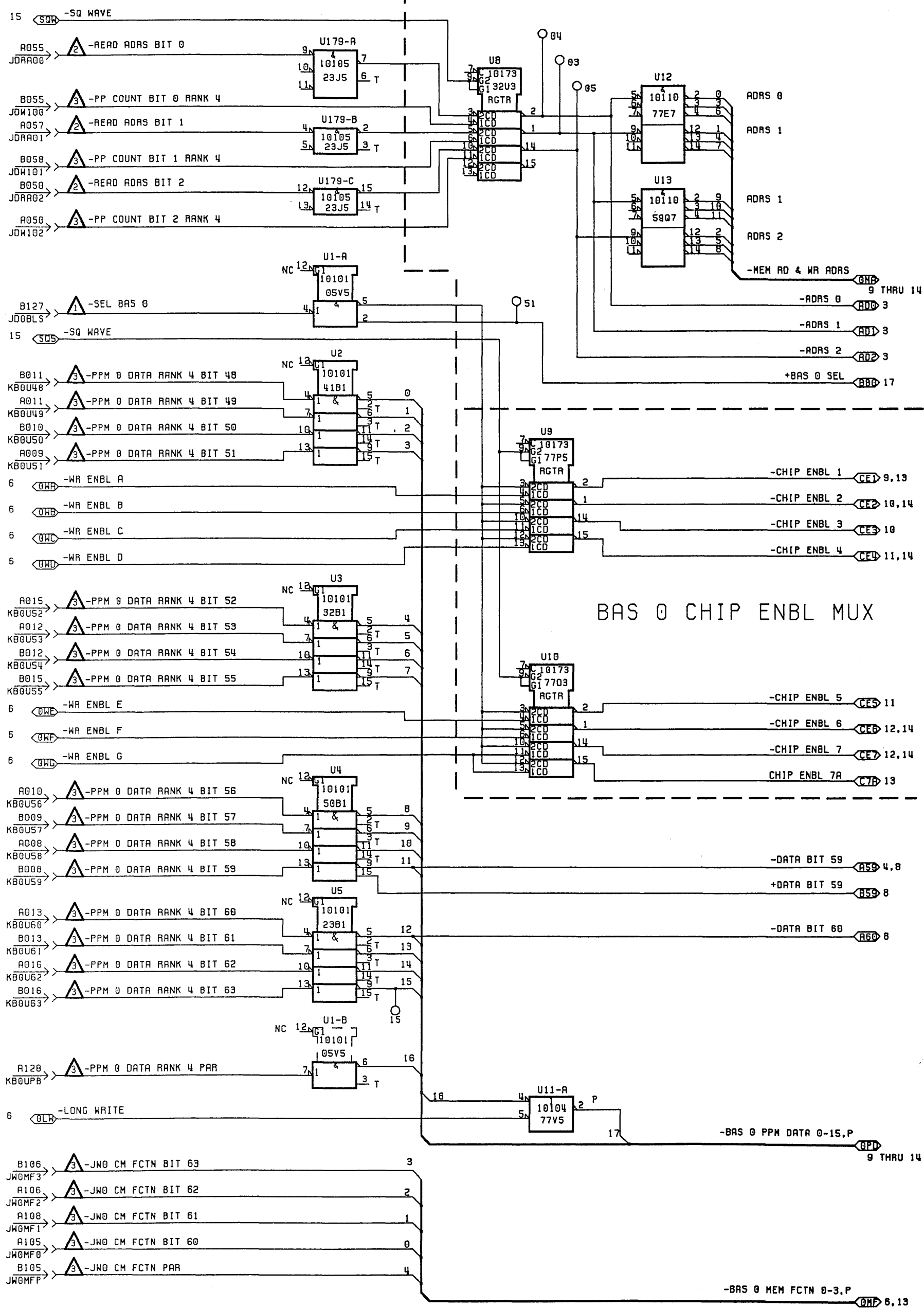
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LOC:  JE AT A14
      JV AT A13 & A12
```

DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	01/21/86
ENG	W E DIETHART	01/10/86
PUBS	R K BONDE	01/10/86
APP	W E DIETHART	01/10/86


 CONTROL DATA	REVISION HISTORY	B	DWG NO.	DATE	REV
	TYPE 1JEH/1JVH		22105672	08/21/87	D
		SHEET NO.	1	60462210	PAGE 1E-01

DATA, FCTN, AND BAS 0 SEL F/O

ADRS MUX & BAS 0 ADRS F/O

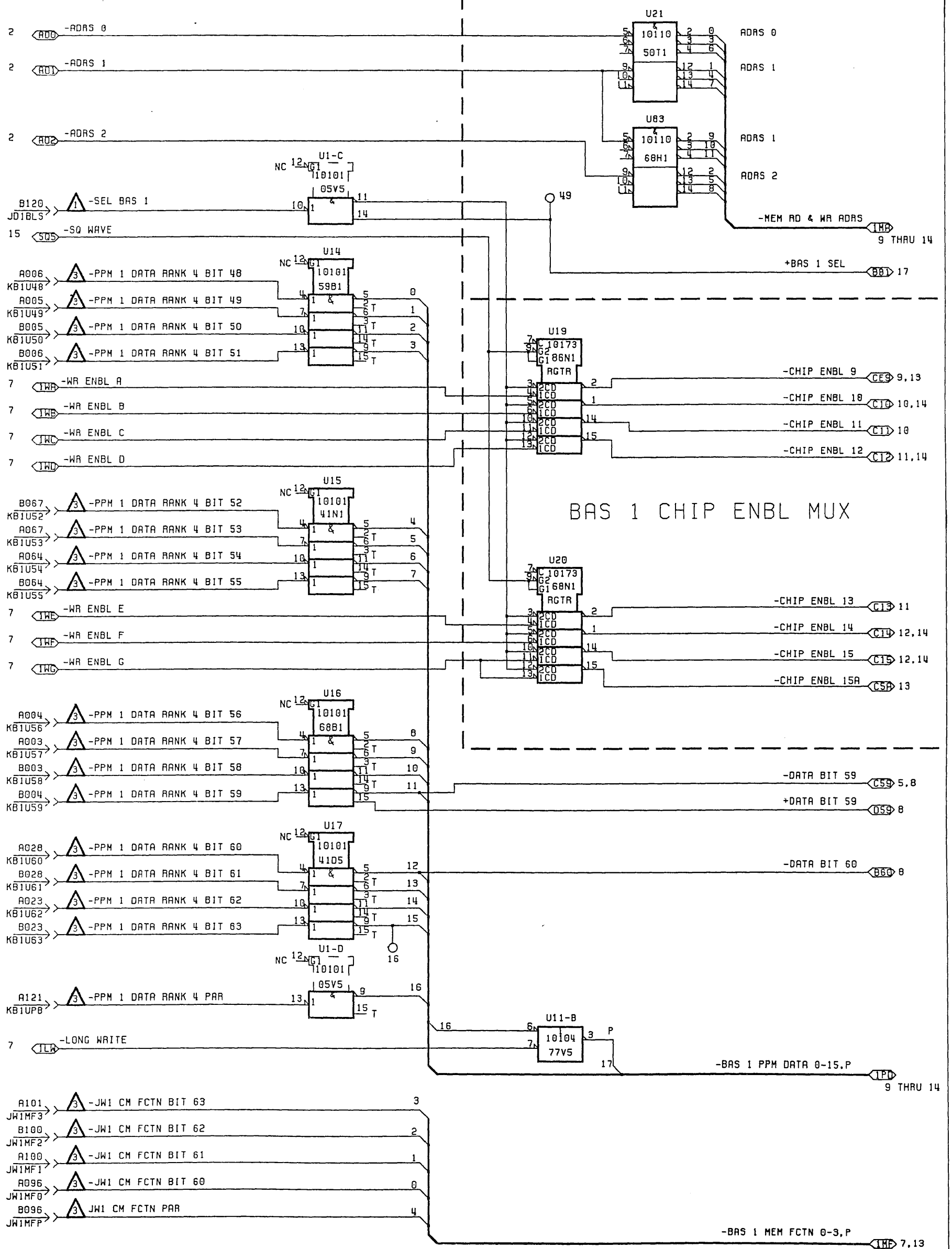


- \triangle NOT TERMINATED AND MAX LENGTH 4"
- \triangle GROUPED TERMINATION AND MAX LENGTH 4"
- \triangle MAX LENGTH 12"


 CONTROL DATA	ADU WRITE BOARD		B	DWG NO. 22105672	DATE 11/01/85	REV A
	BAS 0 FCTN, PPM DATA, CHIP ENBL. READ & WRITE ADDRESS F/O					
	TYPE 1JEH/1JVH		SHEET NO. 2	60462210	PAGE 02	

DATA, FCTN, AND BAS 1 SEL F/O

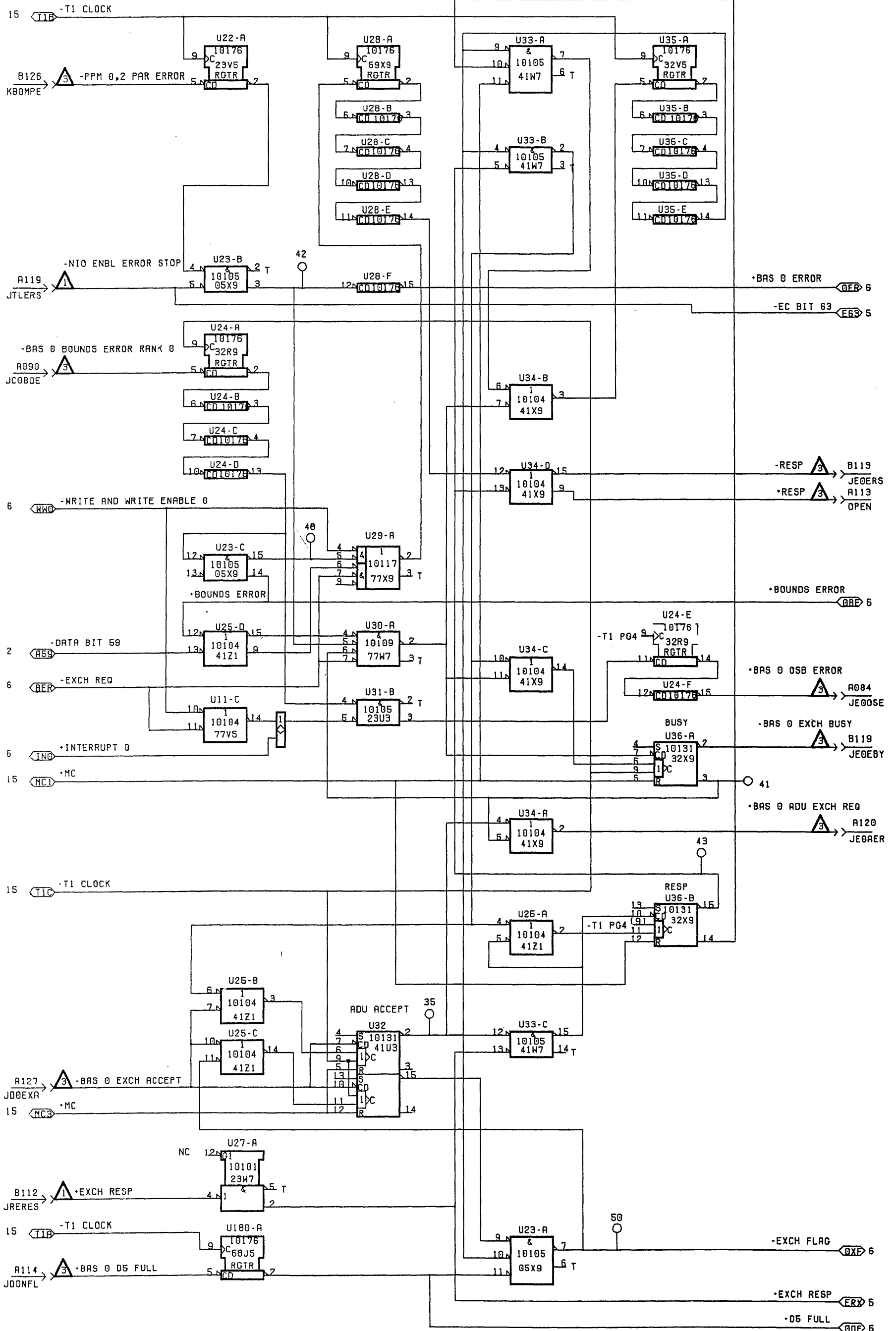
BAS 1 ADRS F/O



△ NOT TERMINATED AND MAX LENGTH 4"
△ MAX LENGTH 12"

 CONTROL DATA	ADU WRITE BOARD BAS 1 FCTN, PPM DATA, CHIP ENBL READ & WRITE ADDRESS F/O TYPE 1JEH/1JVH	8	DWG NO.	DATE	REV
			22105672	11/01/85	A
		SHEET NO. 3		60462210	PAGE IF-03

BAS 0 EXCH REQ LOGIC



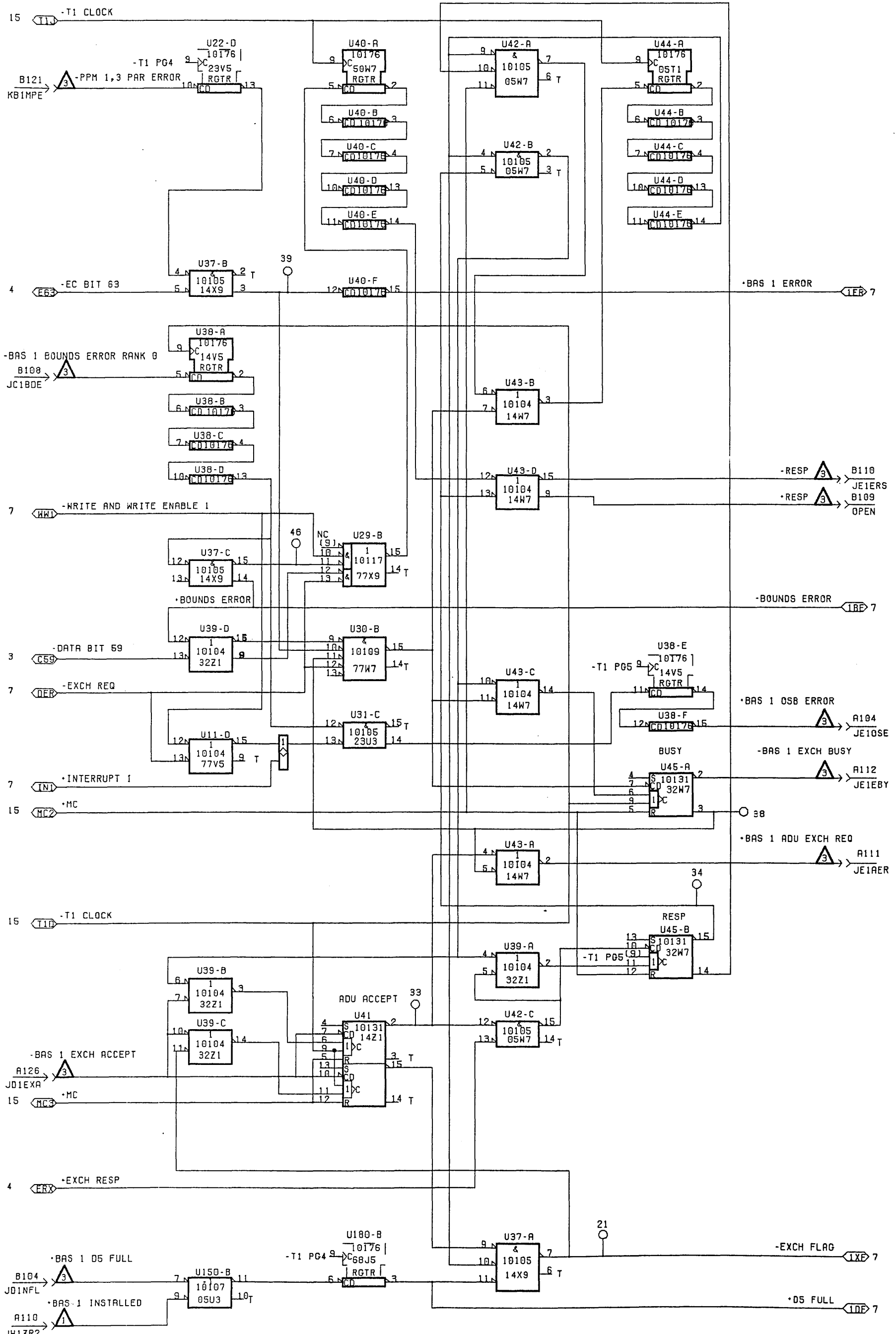
1 NOT TERMINATED AND MAX LENGTH 4"
 3 MAX LENGTH 12"



ADU WRITE BOARD
 BARREL 0 EXCHANGE REQUEST
 TYPE 1JEH/1JVH


DWG NO.	DATE	REV
22105672	06/18/87	C
SHEET NO.	PAGE	REV
4	60462210	JE-04

BAS 1 EXCH REQ LOGIC

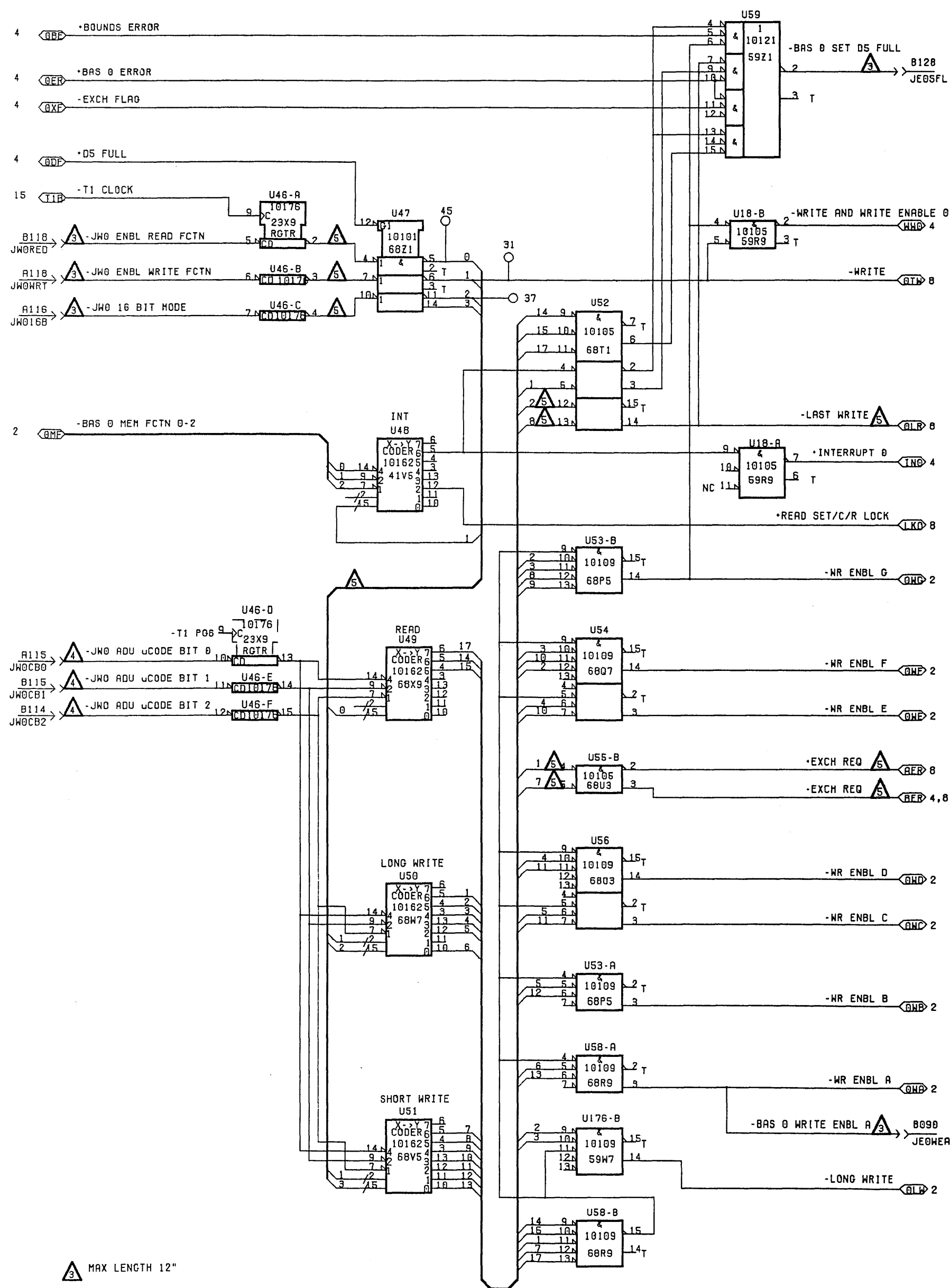



DO NOT TERMINATE AND MAX LENGTH 4"

△ MAX LENGTH 12"

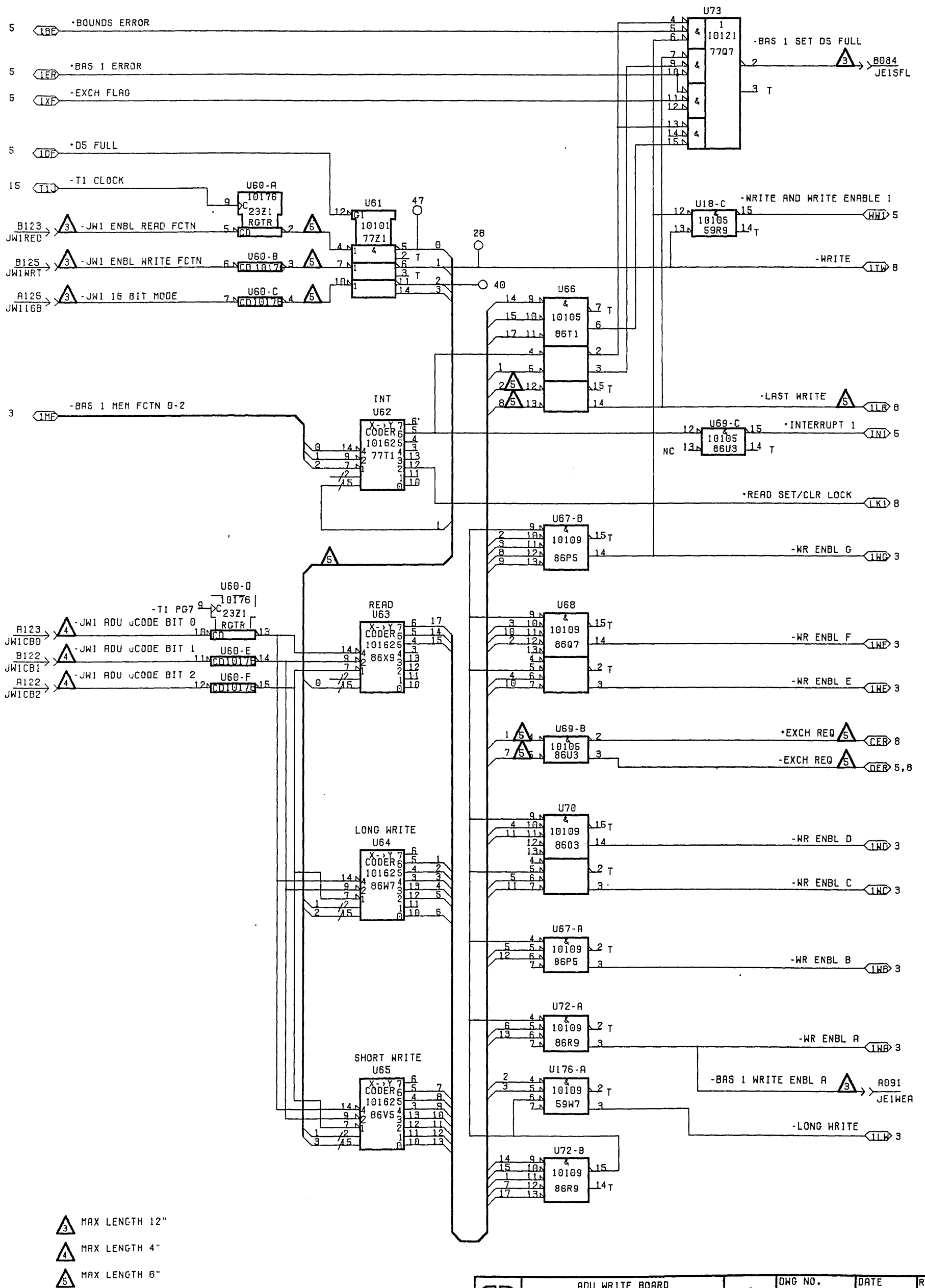
 CONTROL DATA	ADU WRITE BOARD BARREL 1 EXCHANGE REQUEST		B	DWG NO. 22105672	DATE 06/17/87	REV C
	TYPE 1JEH/1JVH			SHEET NO. 5	60462210	PAGE 1E-05


BAS 0 WRITE ENBLS AND EXCH REQ



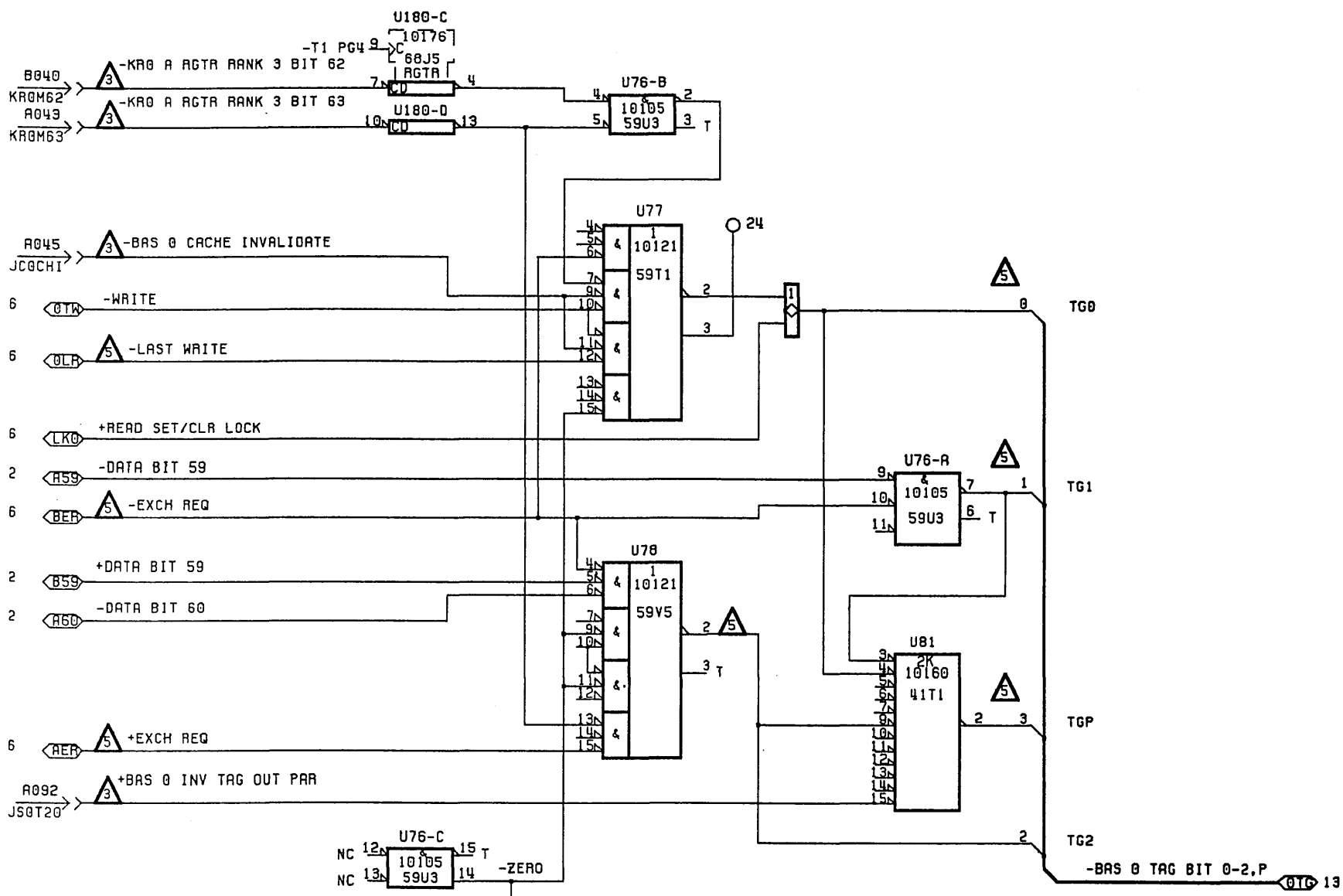
 CONTROL DATA	ADU WRITE BOARD BARREL 0 WRITE ENABLE AND EXCHANGE REQUEST F/O TYPE 1JFH/1JVH	B	DWG NO.	DATE	REV
			22105672	06/18/87	C
			SHEET NO. 6		60462210

BAS 1 WRITE ENBLS AND EXCH REQ

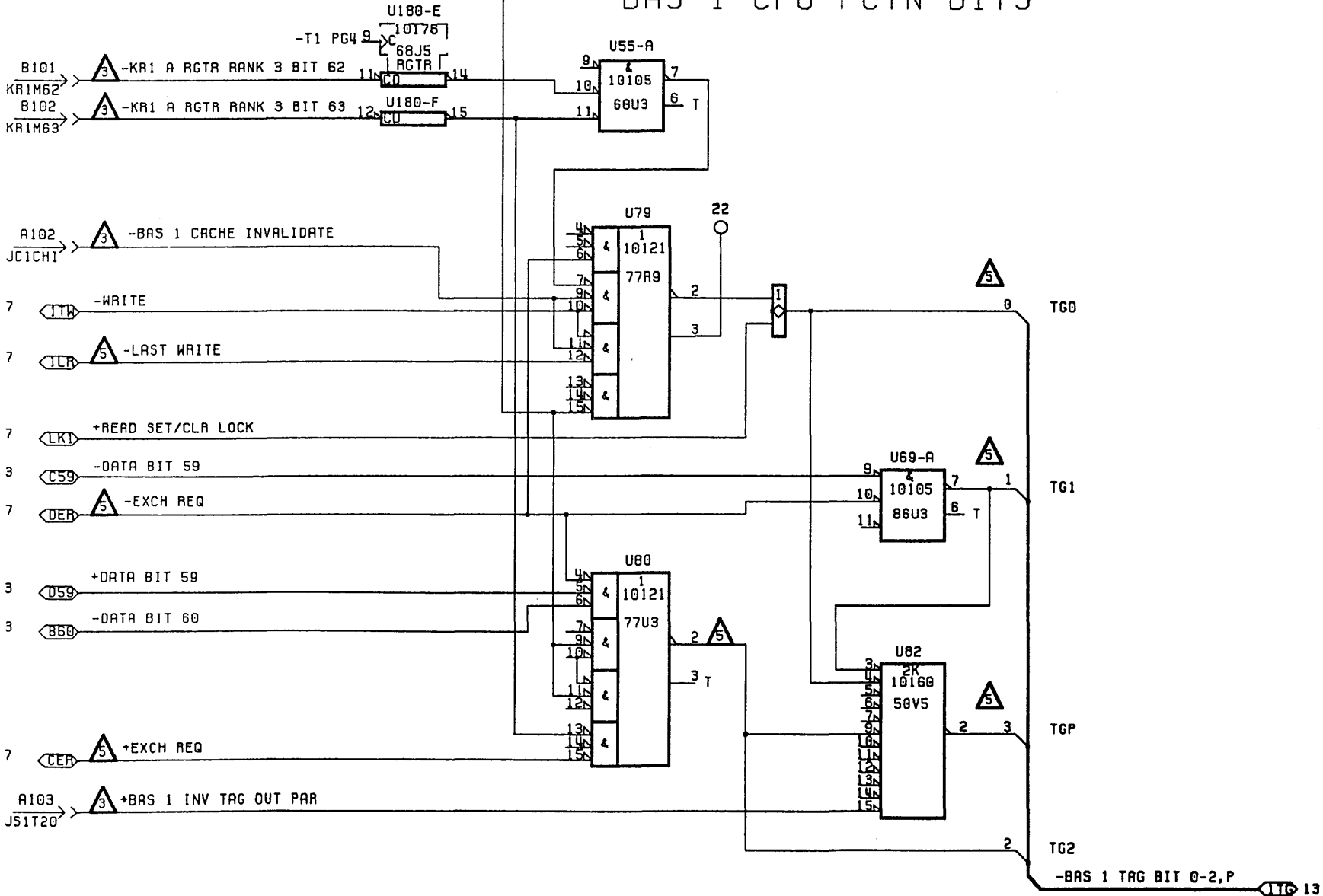


 CONTROL DATA	ADU WRITE BOARD BARREL 1 WRITE ENABLE AND EXCHANGE REQUEST F/O TYPE 1JEH/JVH	N	DWG NO.	DATE	REV	
			8	22105672	06/18/87	C
			SHEET NO. 7		60462210	PAGE

BAS 0 CPU FCTN BITS



BAS 1 CPU FCTN BITS

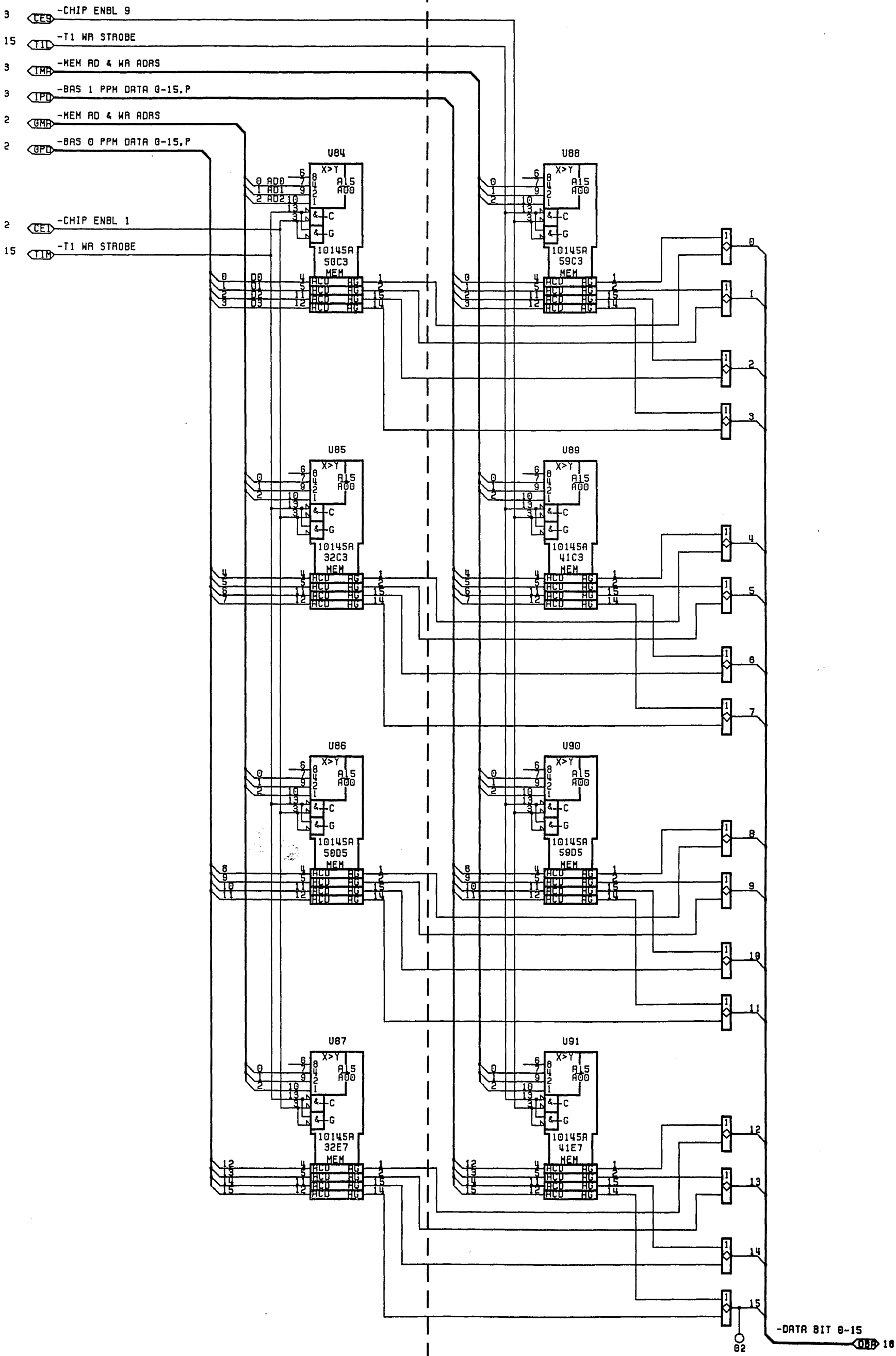



3 MAX LENGTH 12"
5 MAX LENGTH 6"

CONTROL DATA	ADU WRITE BOARD BAS 0 & 1 CP FUNCTION BITS		DWG NO. 8	DATE 11/01/85	REV A
	TYPE 1JEH/1JVH		SHEET NO. 8	68462210	PAGE 1E-00

BAS 0 ASSY RGTR BITS 0-15

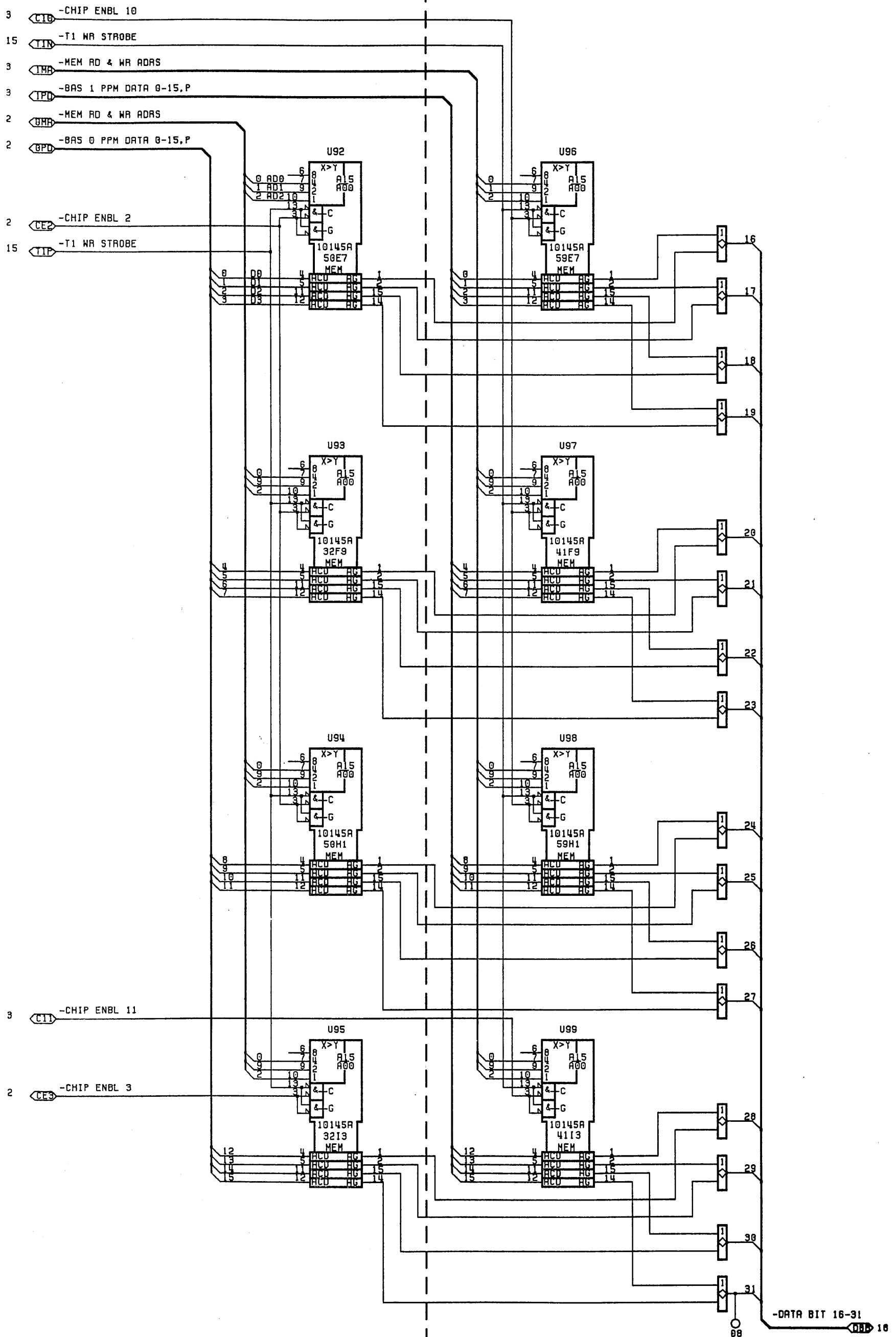
BAS 1 ASSY RGTR BITS 0-15



 CONTROL DATA	ADU WRITE BOARD		B	DWG NO.	DATE	REV
	ASSY RGTR BARREL 0 AND 1			22185672	11/01/85	A
	DATA BITS 0-15					
	TYPE 1JEH/1JVH					
	N		SHEET NO. 9	68462210	PAGE	10-88

BAS 0 ASSY RGTR BITS 16-31

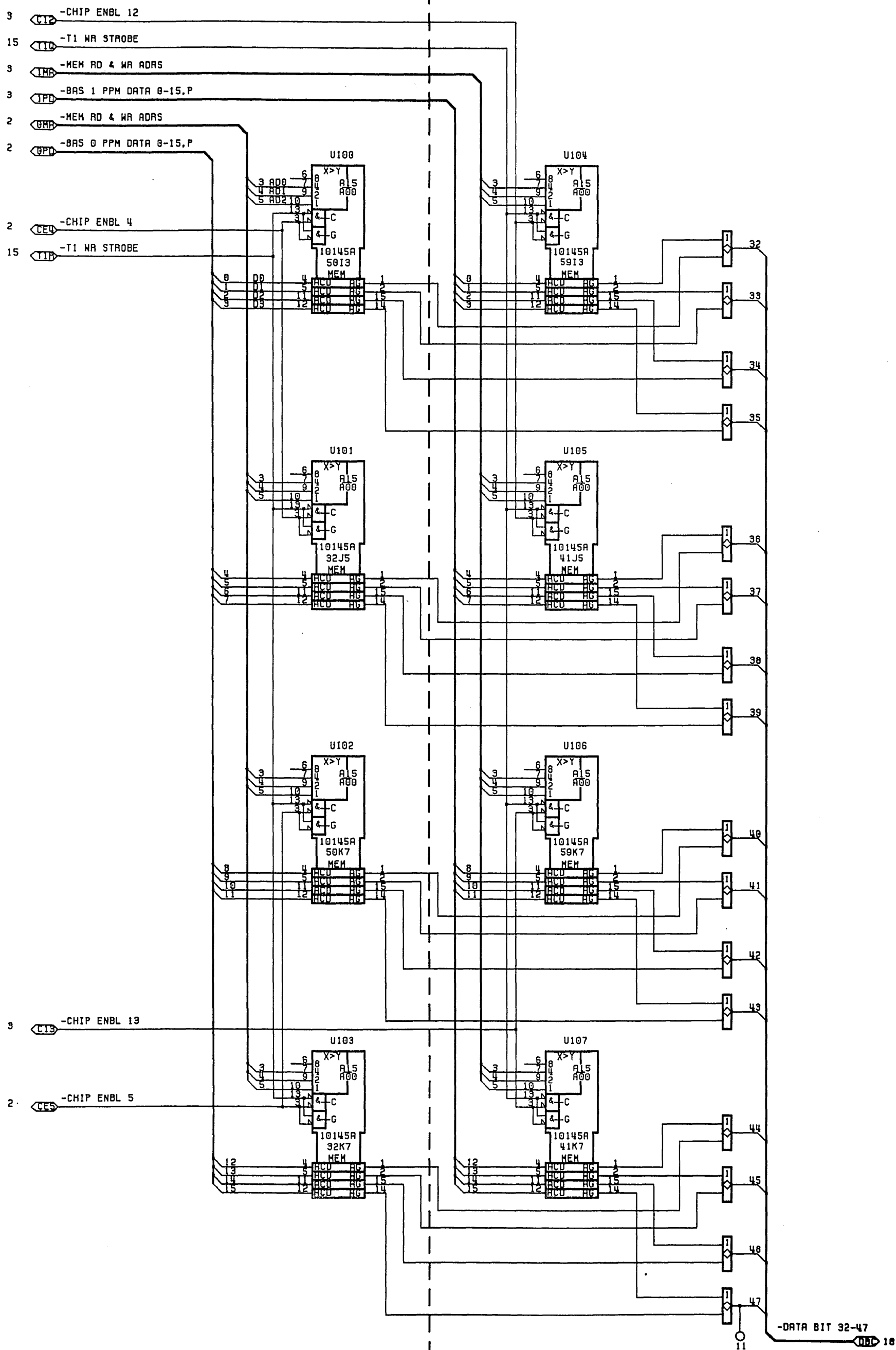
BAS 1 ASSY RGTR BITS 16-31



	ADU WRITE BOARD		8	DWG NO.	DATE	REV
	ASSY RGTR BARREL 0 AND 1			22105672	11/01/85	A
DATA BITS 16-31		TYPE 1JEH/1JVH		SHEET NO. 10	60462210	PAGE 10

BAS 0 ASSY RGTR BITS 32-47

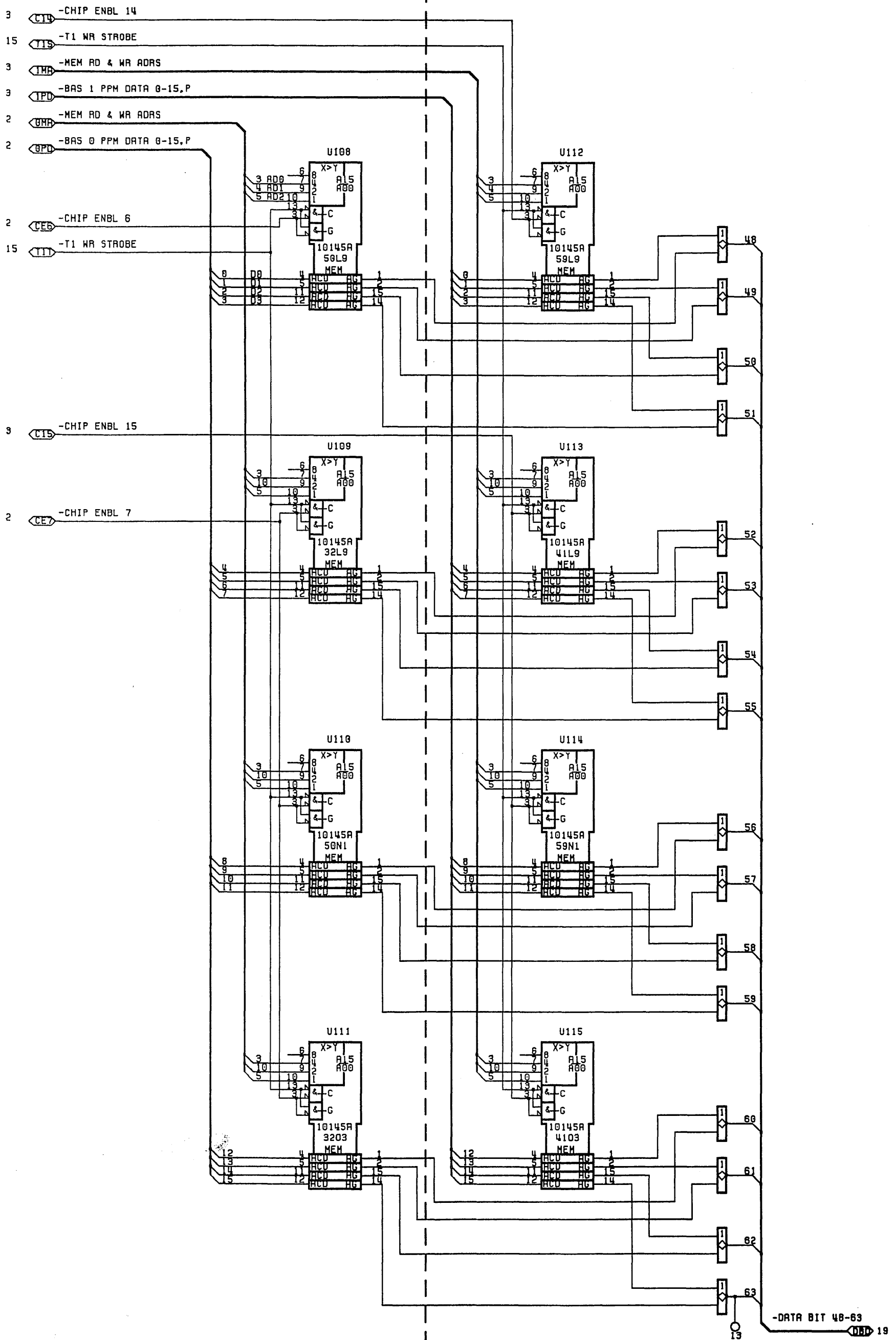
BAS 1 ASSY RGTR BITS 32-47



	ADU WRITE BOARD			
	ASSY RGTR BARREL 0 AND 1			
	DATA BITS 32-47			
TYPE 1JEH/1JVH	DWG NO. 8		DATE 11/01/85	REV A
	SHEET NO. 11		60462210	PAGE 11

BAS 0 ASSY RGTR BITS 48-63

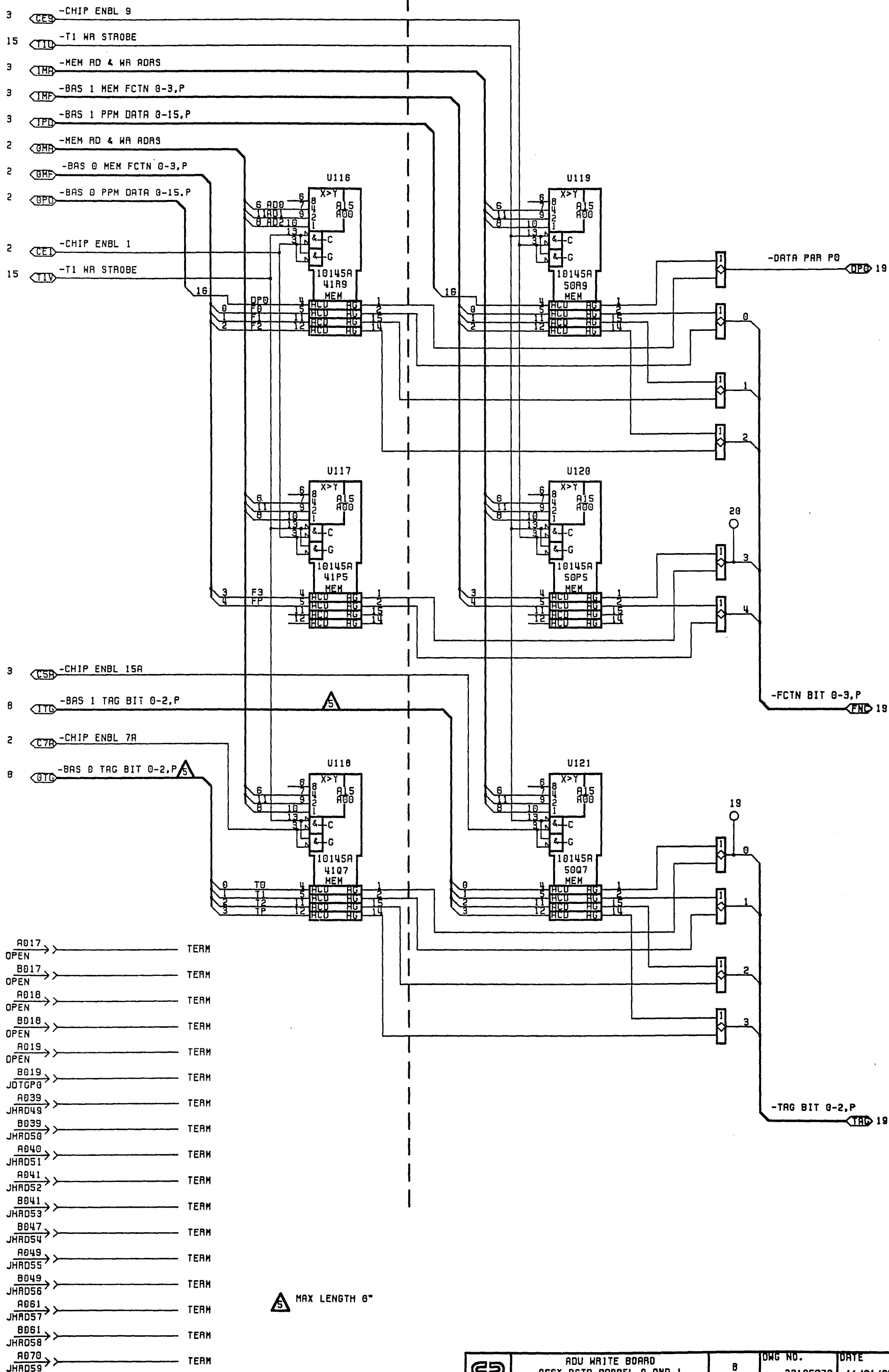
BAS 1 ASSY RGTR BITS 48-63



	ADU WRITE BOARD		DWG NO.	DATE	REV
	ASSY RGTR BARREL 0 AND 1		B	22105672	11/01/85
	DATA BITS 48-63				A
TYPE 1JH/1JVH	SHEET NO. 12	60462210	PAGE	JE-12	

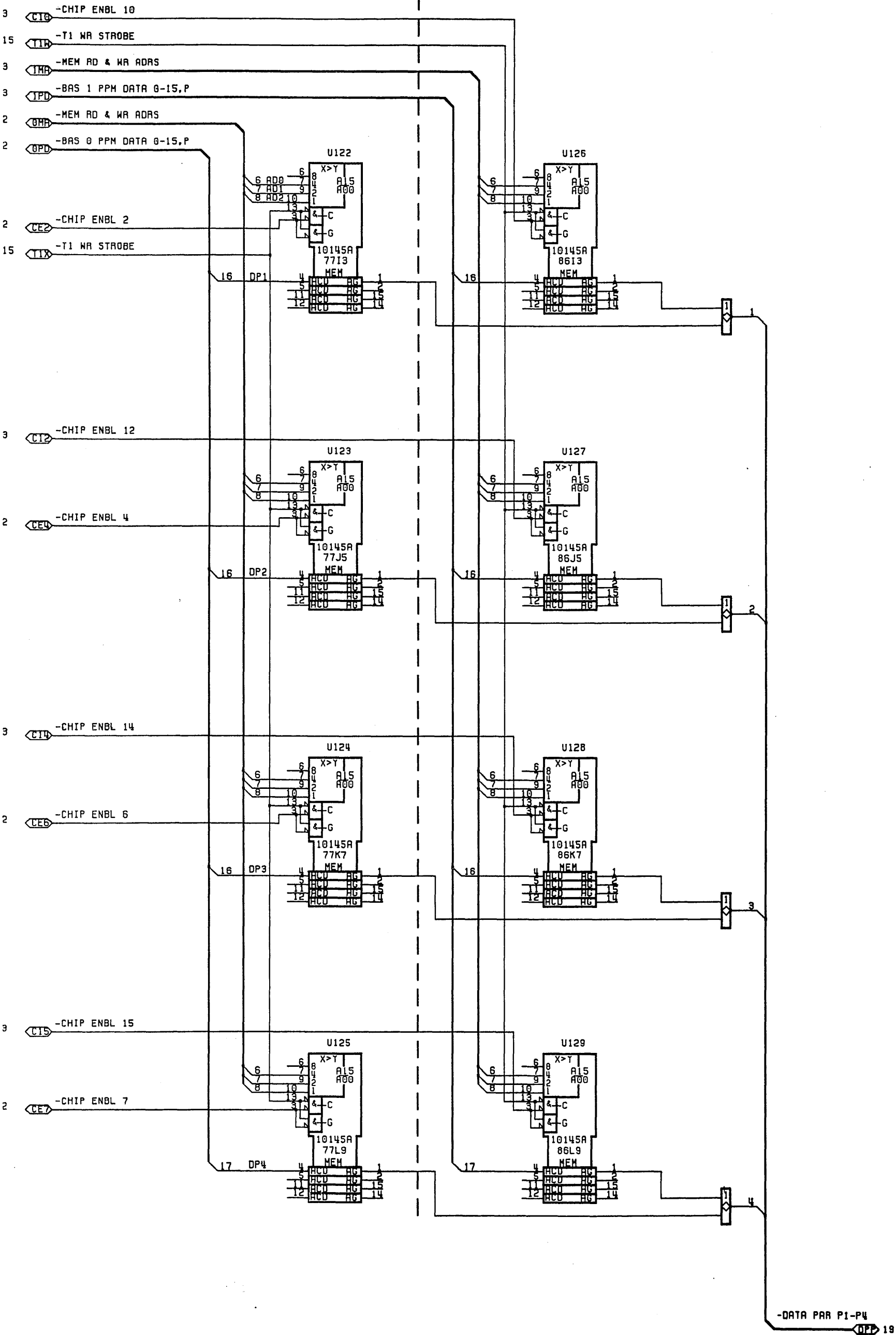
BAS 0 ASSY RGTR PAR BIT 0, FCTN, TAG

BAS 1 ASSY RGTR PAR BIT 0 FCTN & TAG



	ADU WRITE BOARD ASSY RGTR BARREL 0 AND 1 DATA P0, FCTN 0-3,P & TAG 0-2,P TYPE 1JEH/1JVH	B	DWG NO. 22105672	DATE 11/01/85	REV A

BAS 0 ASSY RGTR PAR BITS 1-4 | BAS 1 ASSY RGTR PAR BITS 1-4



ADU WRITE BOARD
ASSY RGTR BAS 0 AND 1
DATA PARITY P1-P4
TYPE 1JEH/1JVH

B

DWG NO.
22105072

DATE
11/01/85

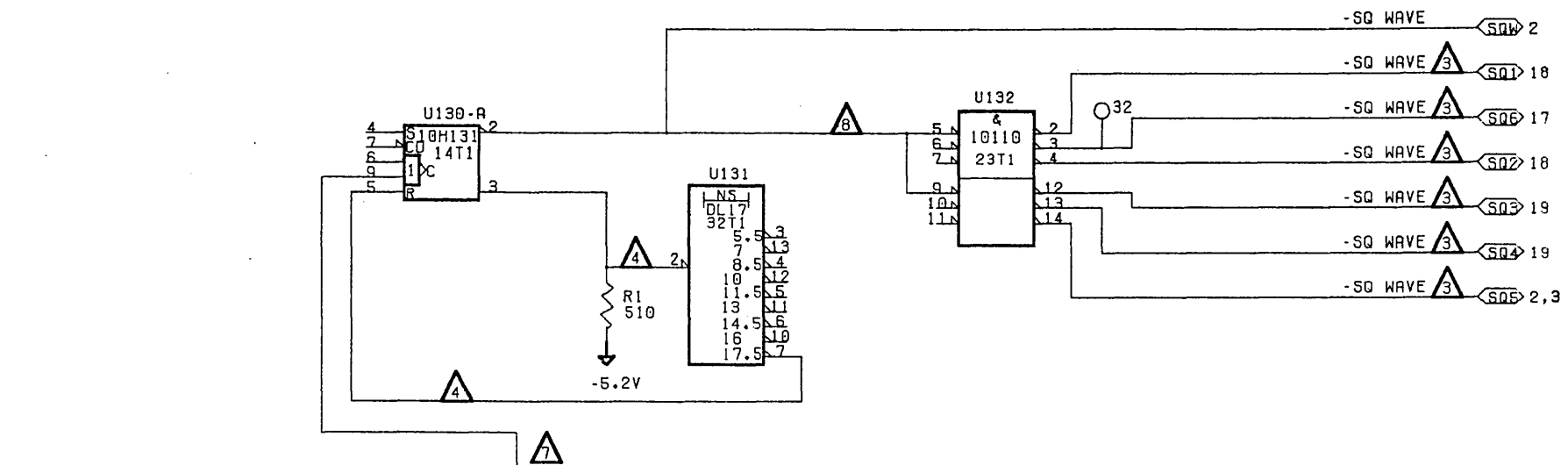
REV
A

SHEET NO. 14

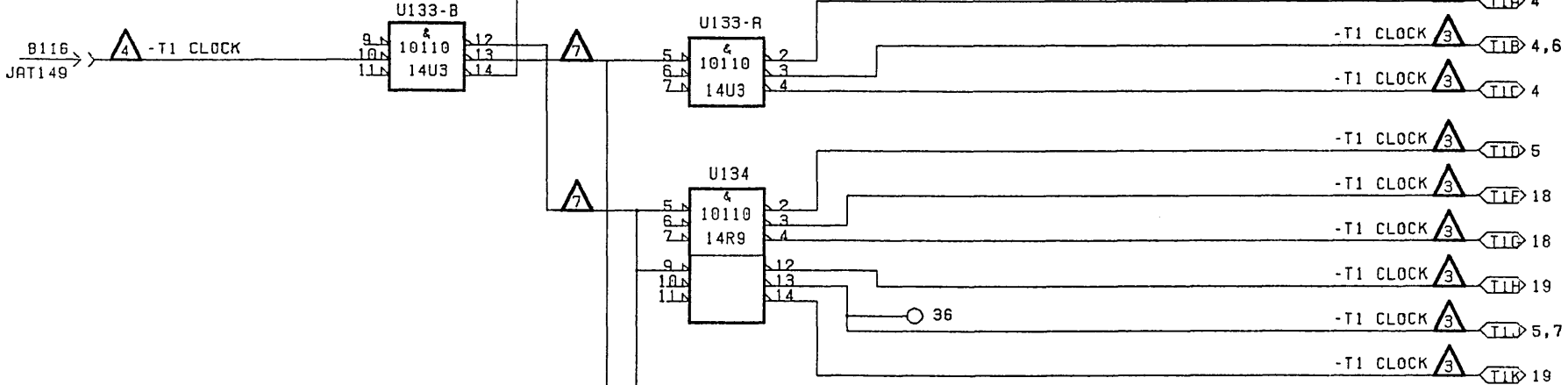
60462210

PAGE
JE-14

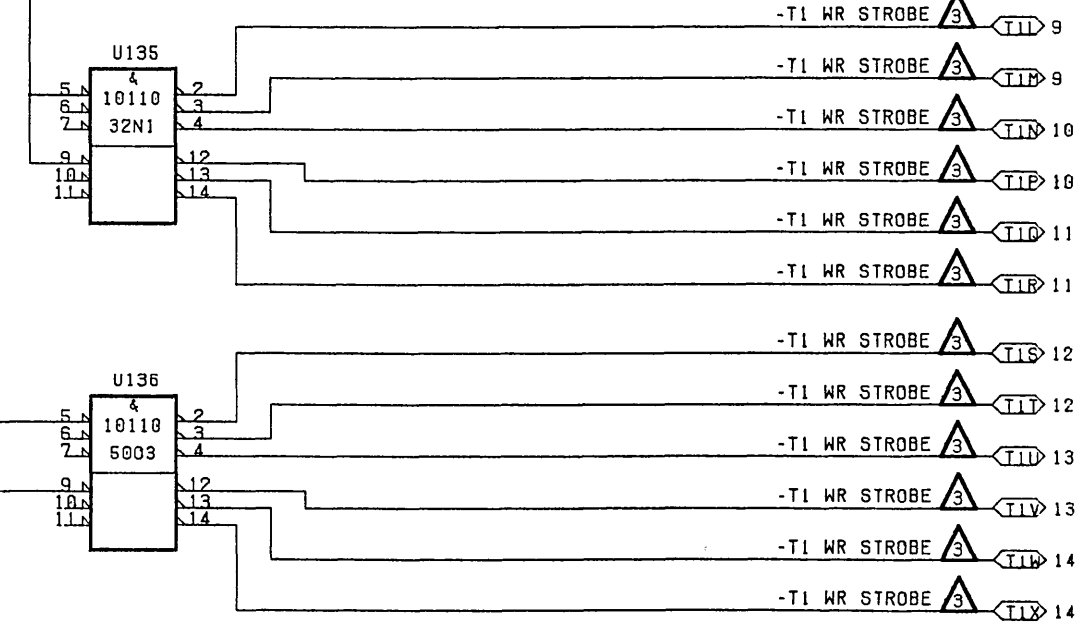
SQ WAVE GEN



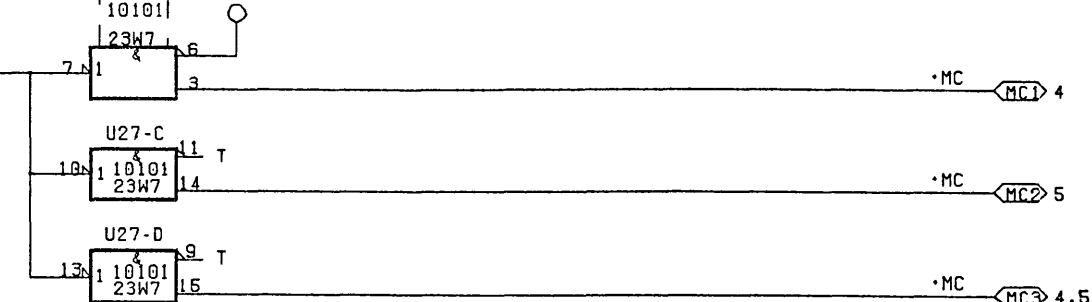
CLK F/O



T1 WRITE STROBE F/O



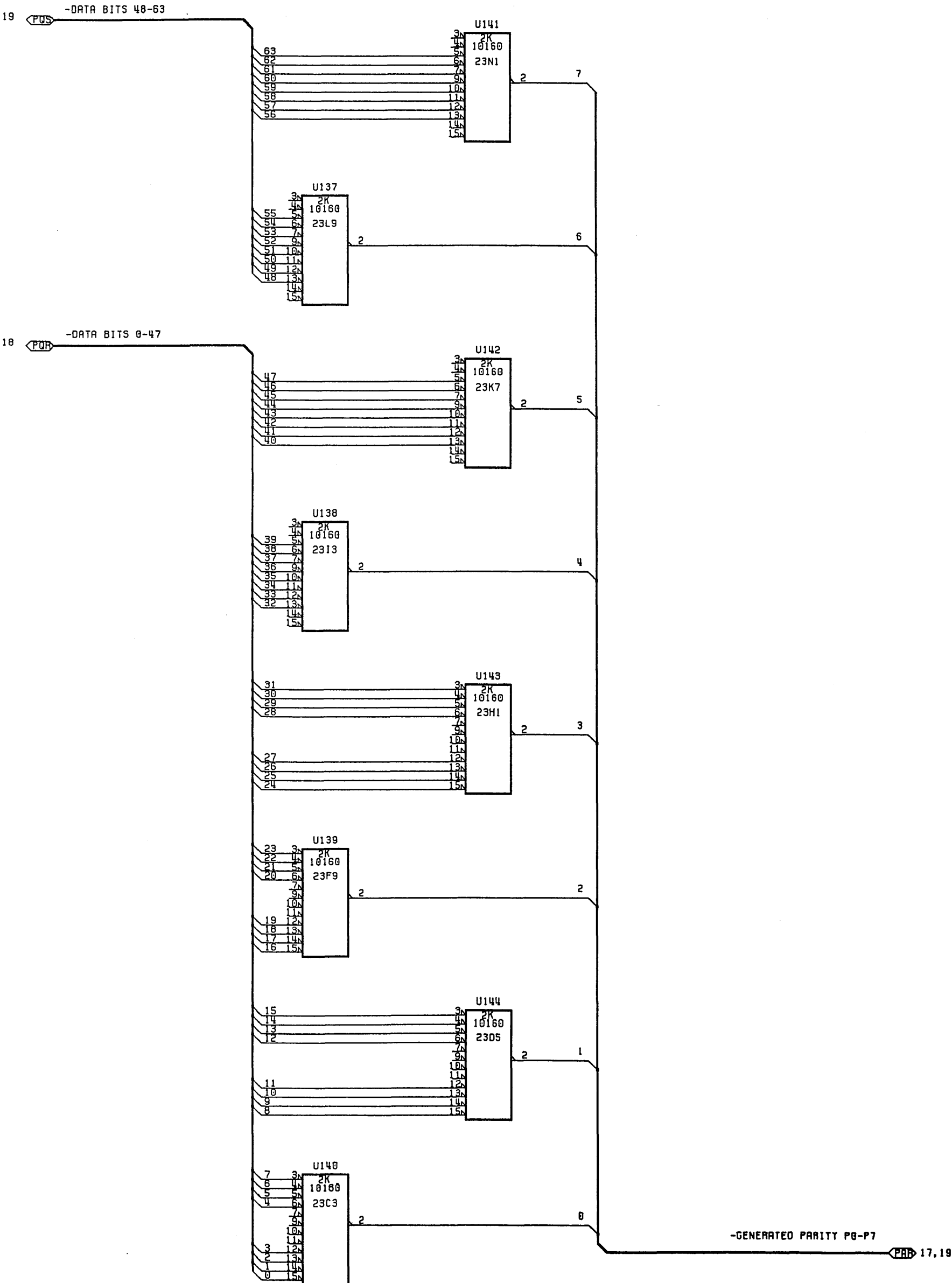
MASTER CLEAR F/O



- A109 JQAUMC -MASTER CLEAR
- B070 JHRD60 TERM
- A079 JHRD61 TERM
- B079 JHRD62 TERM
- A090 JHRD63 TERM
- B090 JHRD64 TERM
- A081 JHRD65 TERM
- B081 JHRD66 TERM
- A082 JHRD67 TERM
- B082 JHRD68 TERM
- A093 JHRD69 TERM
- B093 JHRD70 TERM
- A094 JHRD71 TERM
- B094 JHRD72 TERM
- A095 JHRD73 TERM
- B095 JHRD74 TERM
- OPEN A095 JHRD75 TERM
- OPEN B098 JHRD76 TERM
- OPEN A098 JHRD77 TERM
- OPEN B099 JHRD78 TERM
- OPEN A099 JHRD79 TERM
- OPEN B103 JHRD80 TERM
- OPEN B111 JHRD81 TERM
- OPEN

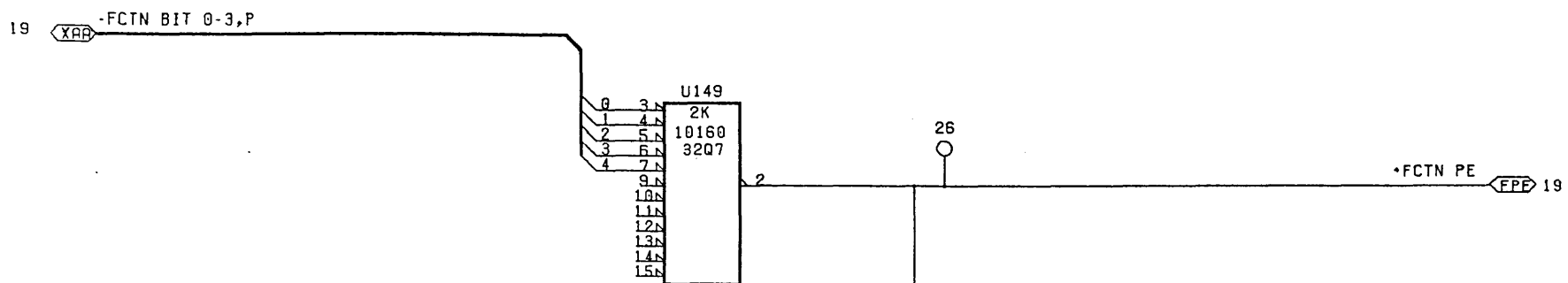
- 3 MAX LENGTH 12"
- 4 MAX LENGTH 4"
- 6 NOT TERMINATED AND MAX LENGTH 12"
- 7 MAX LENGTH 7"
- 8 ROUTE TO 10110 FIRST, MAX LENGTH 7"

DATA PAR GEN

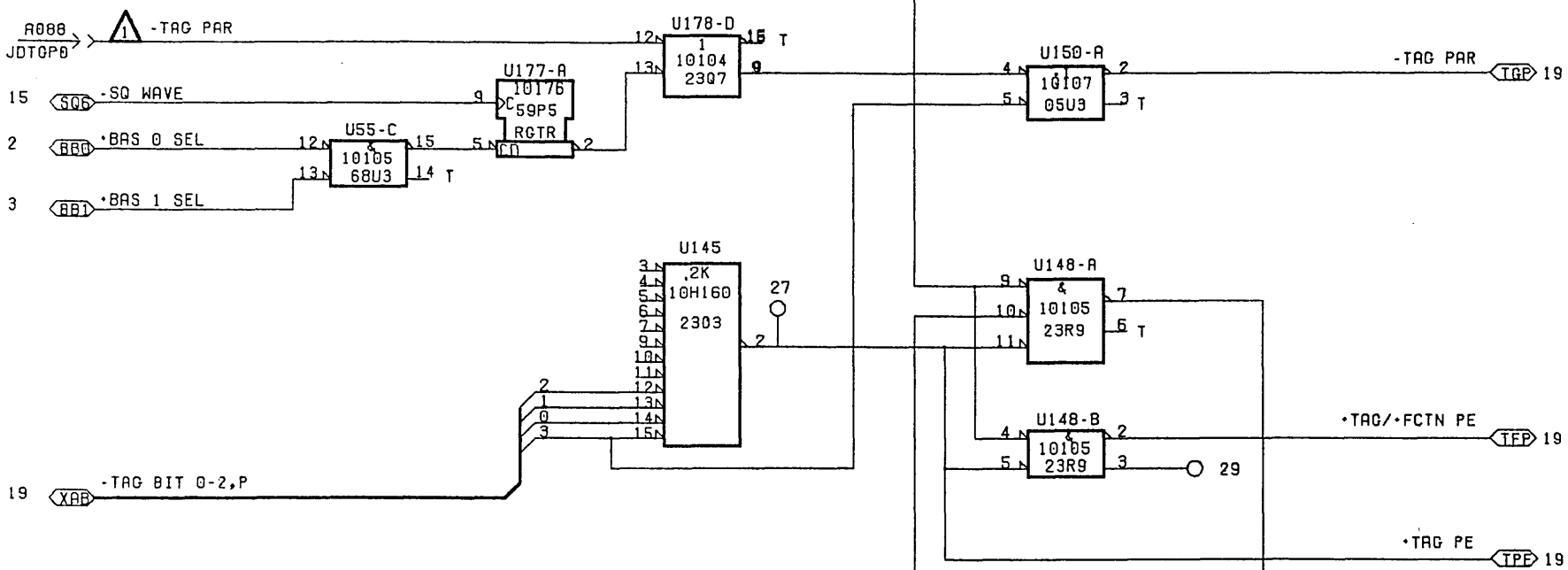


GD CONTROL DATA	ADU WRITE BOARD DATA PARITY GENERATE P8-P7		DWG NO. B	22105672	DATE 11/01/85	REV A
	TYPE 1JEH/1JVH		SHEET NO. 16	60462210	PAGE JE-10	

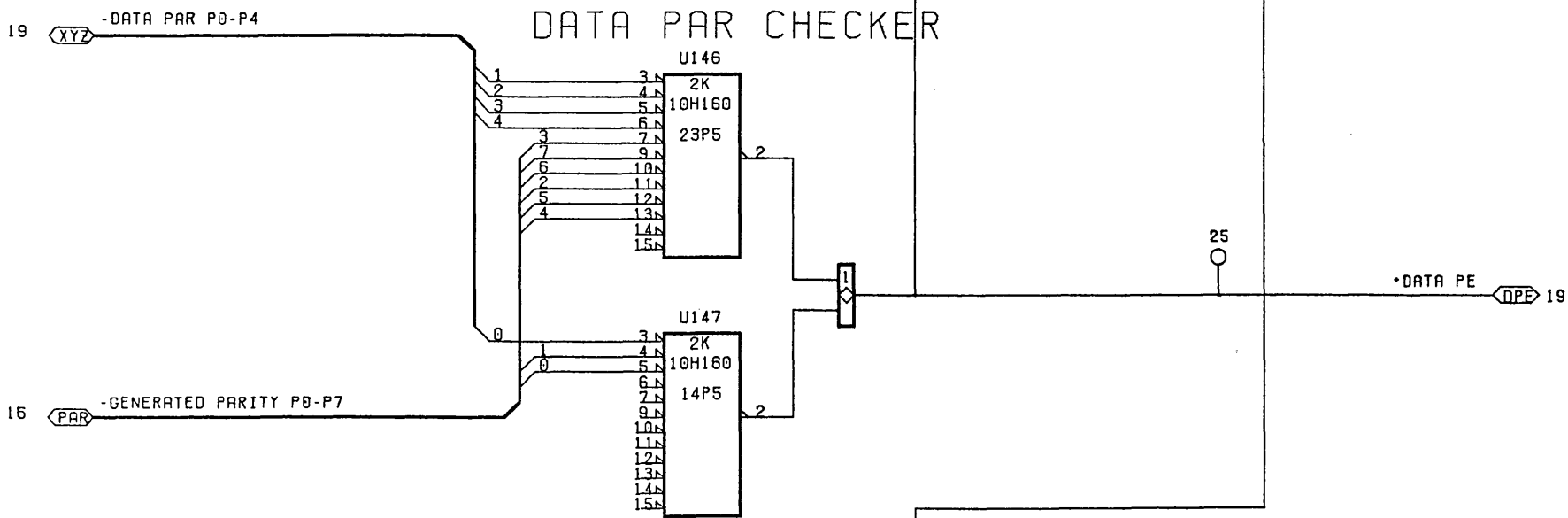
FCTN PAR CHECKER



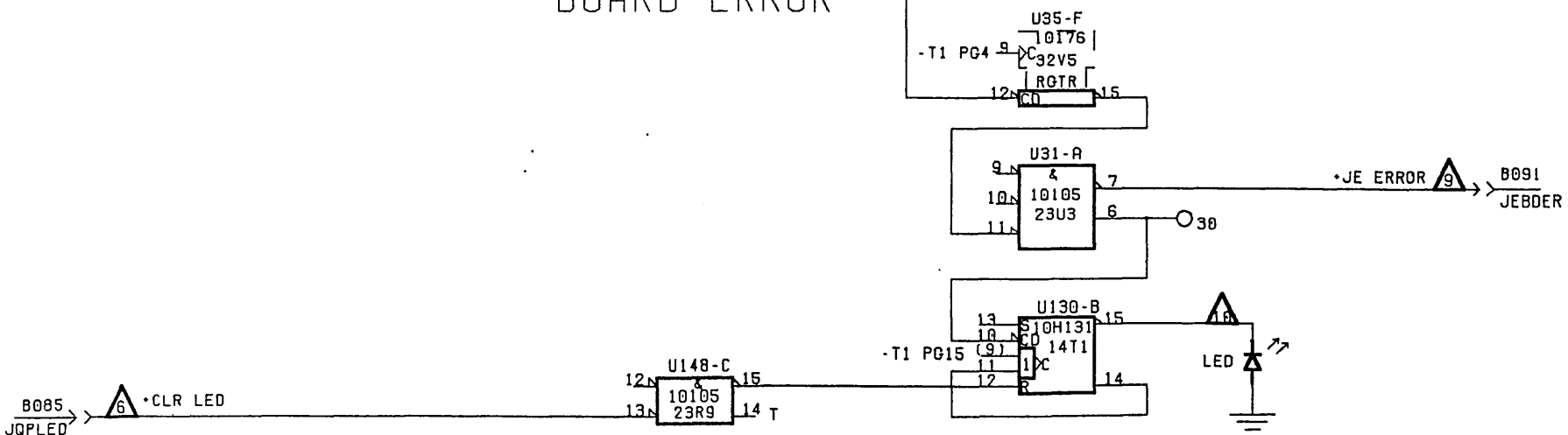
TAG PAR CHECKER AND GEN




DATA PAR CHECKER



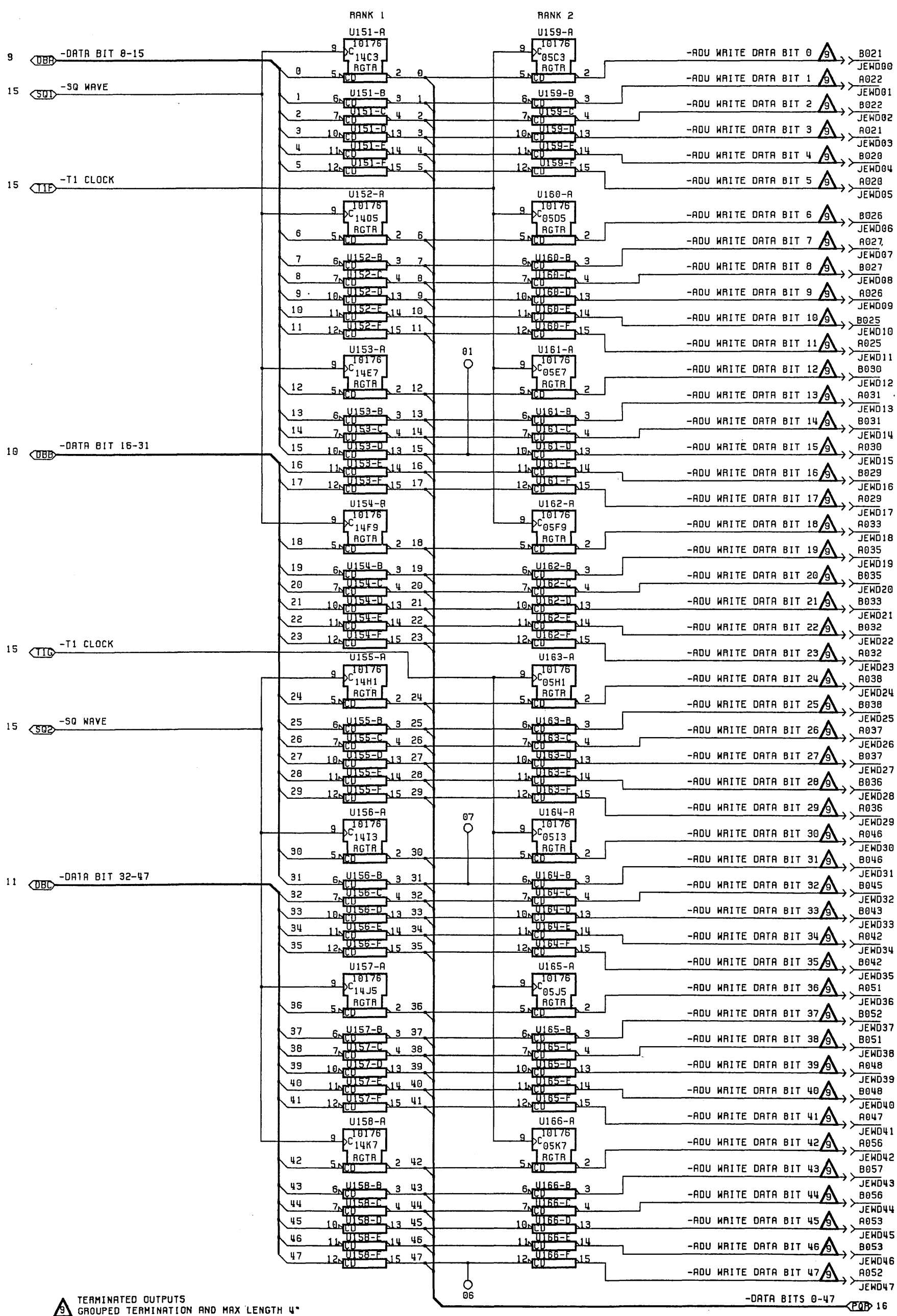
BOARD ERROR




- | | |
|----|--|
| 1 | NOT TERMINATED AND MAX LENGTH 4" |
| 6 | NOT TERMINATED AND MAX LENGTH 12" |
| 9 | TERMINATED OUTPUT
GROUPED TERMINATION AND MAX LENGTH 4" |
| 10 | TERMINATED |

 CONTROL DATA	ADU WRITE BOARD DATA, FCTN AND TAG PAR CHECKERS AND BOARD ERROR	B	DWG NO. 22105672	DATE 08/21/87	REV 0
	TYPE 1JEH/1JVH		SHEET NO. 17	60462210	PAGE 17

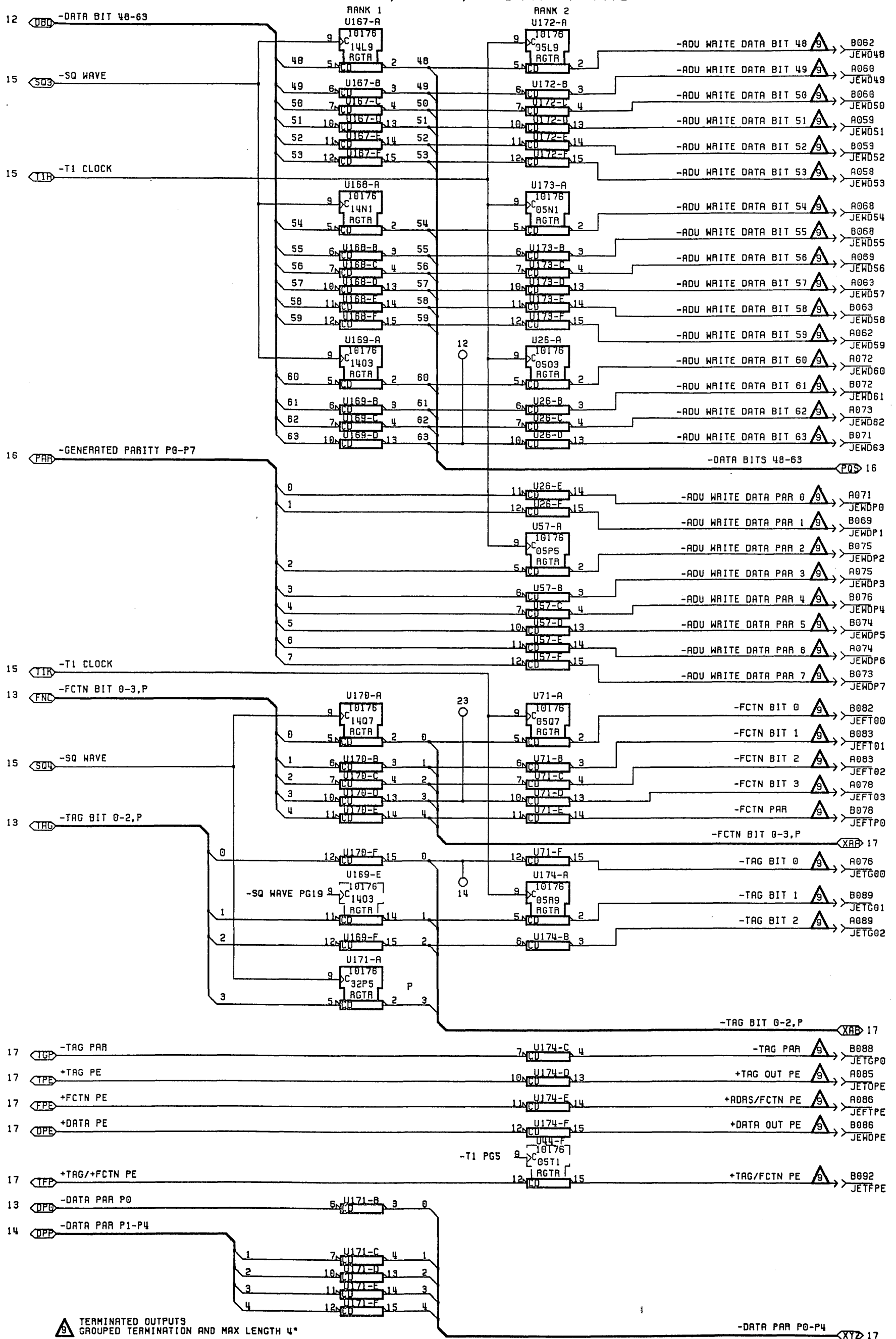
OUT RGTR BITS 0-47




9 TERMINATED OUTPUTS
GROUPED TERMINATION AND MAX LENGTH 4"

 CONTROL DATA	ADU WRITE BOARD OUTPUT REGISTER DATA BITS 0-47 TYPE 1JEH/1JVH	8	DWG NO. 22105672	DATE 11/01/85	REV A
		SHEET NO. 18		60462210	PAGE JE-10

OUT RGTR BITS 48-63, PAR, FCTN & TAG



9 TERMINATED OUTPUTS
GROUPED TERMINATION AND MAX LENGTH 4"

 CONTROL DATA	ADU WRITE BOARD OUTPUT REGISTER FOR DATA, PAR, FCTN AND TAG TYPE 1JH/1JVH	B	DWG NO.	DATE	REV
			22105672	11/01/85	A
		N	SHEET NO. 19	60462210	PAGE 15-19

TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	18	-DATA BT 15 OUT RGTF	27	17	+TAG PAR ERROR
02	09	-DATA BT 15 ASY RGTF	28	07	-BAS N+1 WRITE BIT
03	02	-RD/WRT ADRS BIT 1	29	17	-TAG/FCTN PAR ERR
04	02	-RD/WRT ADRS BIT 0	30	17	-BOARD ERROR
05	02	-RD/WRT ADRS BIT 2	31	06	-BAS N WRITE BIT
06	18	-DATA BT 47 OUT RGTF	32	15	-SQUARE WAVE
07	18	-DATA BT 31 OUT RGTF	33	05	-BAS N+1 ADU EX ACPT
08	10	-DATA BT 31 ASY RGTF	34	05	-BAS N+1 EX RESPONCE
09			35	04	-BAS N ADU EX ACCEPT
10			36	15	-T1 CLOCK
11	11	-DATA BT 47 ASY RGTF	37	06	-BAS N 16 BIT WRITE
12	19	-DATA BT 63 OUT RGTF	38	05	-BAS N+1 EX BUSY
13	12	-DATA BT 63 ASY RGTF	39	05	+BAS N+1 PPM PAR ERR
14	19	-TAG BIT 0 OUT RGTR	40	07	-BAS N+1 16 BIT WRT
15	02	-BAS N PPM D BIT 63	41	04	-BAS N EX BUSY
16	03	-BBL N+1 PPM D BT63	42	04	+BAS N PPM PAR ERR
17			43	04	-BAS N EX RESP
18			44	15	-MASTER CLEAR
19	13	-TAG BIT 0 ASY RGTR	45	06	-BAS N READ BIT
20	13	-FCTN BIT 3 ASY RGTF	46	05	-BAS N+1 BOUNDS ERR
21	05	-BAS N+1 EXCH FLAG	47	07	-BAS N+1 READ BIT
22	08	-BAS N+1 TAG BIT 0	48	04	-BAS N BOUNDS ERR
23	19	-FCTN BIT 3 OUT RGTF	49	03	+BARREL N+1 SELECT
24	08	-BAS N TAG BIT 0	50	04	-BAS N EX FLAG
25	17	+DATA PAR ERROR	51	02	+BARREL N SELECT
26	17	+FCTN PAR ERROR			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [USED FOR TERMINATION]
TERM	A017,B017,A018,B018,A019,B019,A039,B039,A040,A041,B041,B047,A049,B049,A061,B061,A070,B070,A079,B079,A080,B080,A081,B081,A082,A093,B093,A094,B094,A095,B095,A098,B098,A099,B099,B103,B111
UNUSED	NONE

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.


ADU READ BOARD

[illegible]

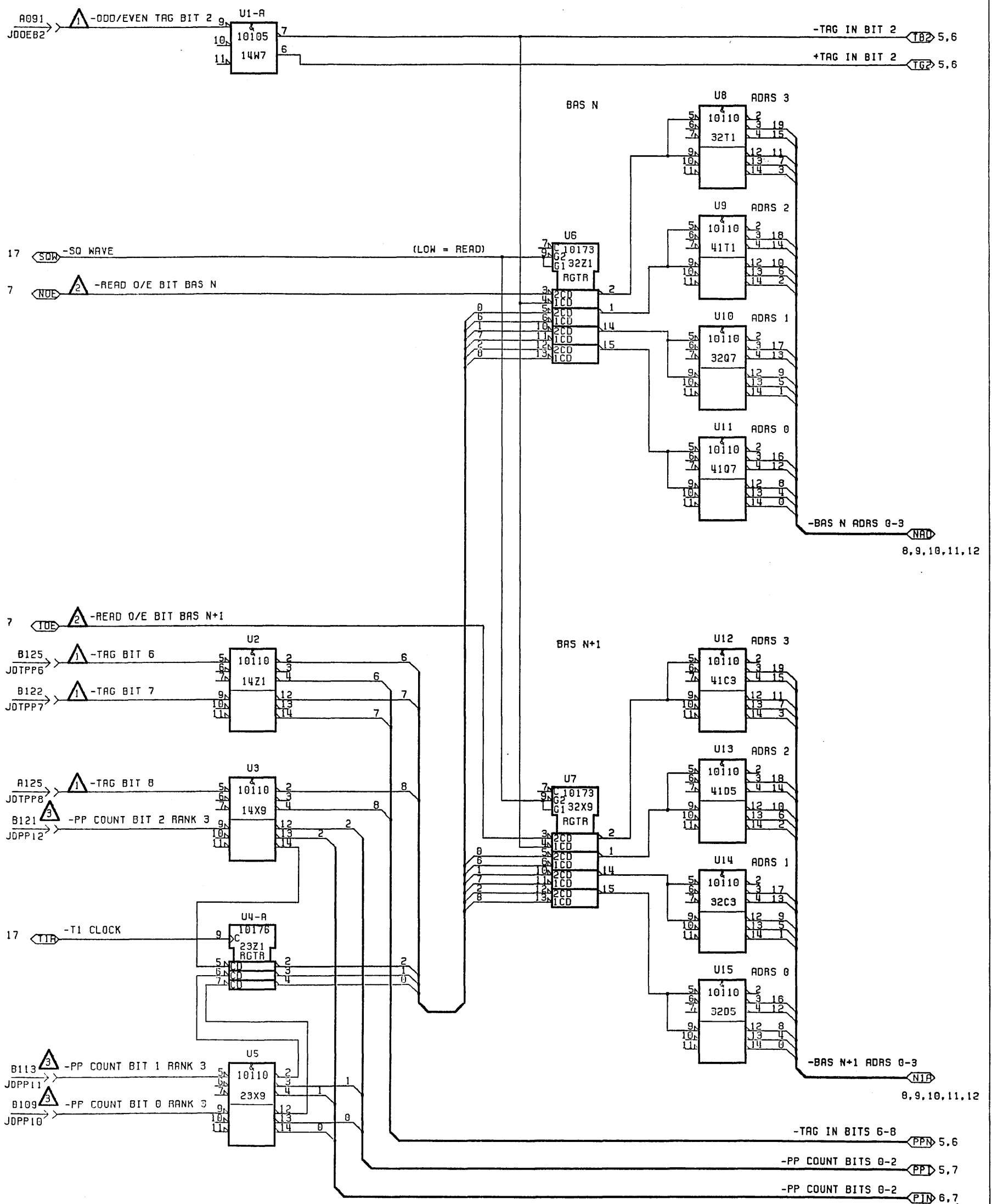
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED

LOC: A18, A17, A16

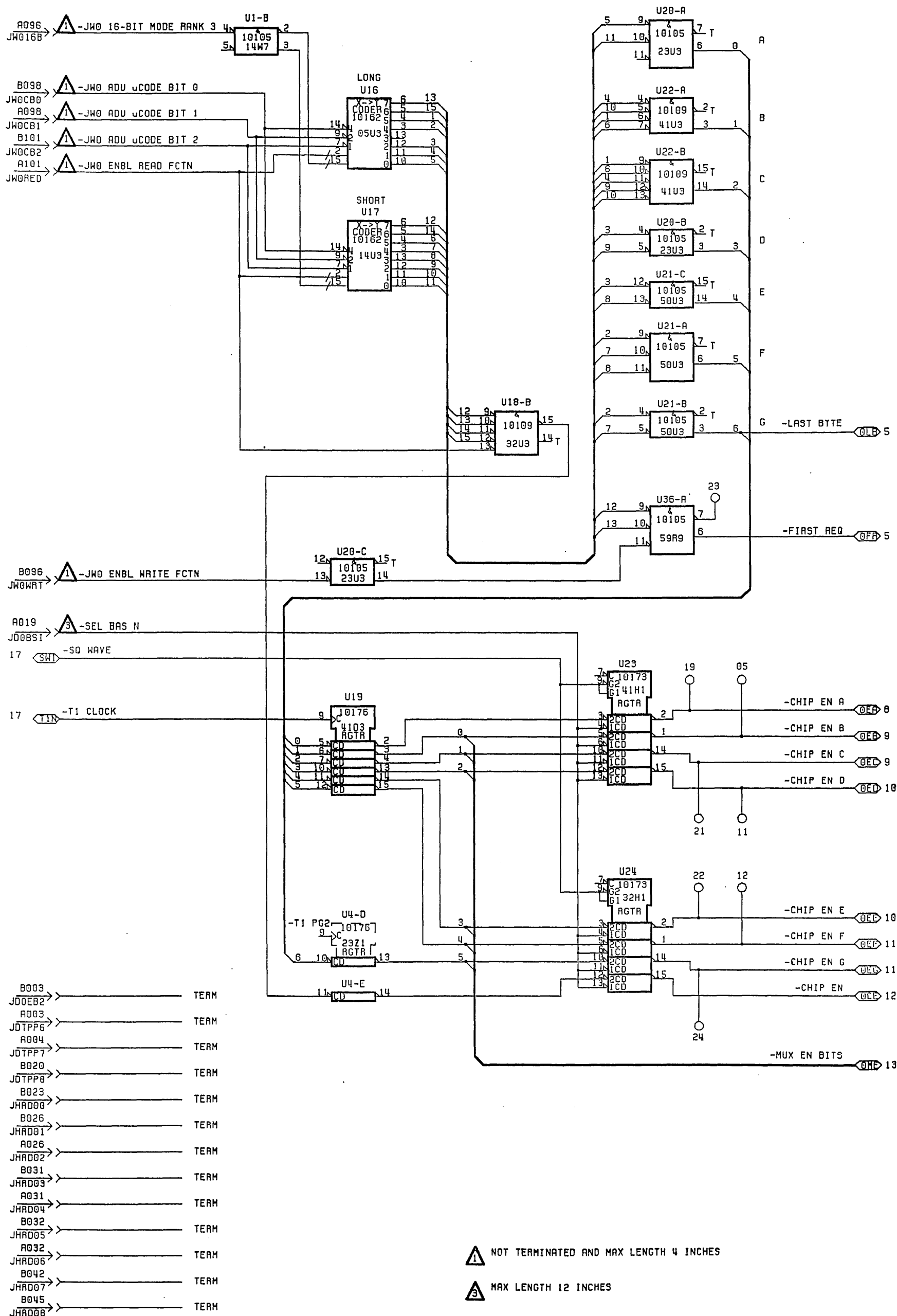
DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	W E DIETHART	12/05/85
PUBS	R K BONDE	12/05/85
APP	W E DIETHART	12/05/85

 CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575505	DATE 03/30/88	REV D
	TYPE 1JFH	SHEET NO. 1	60462210	PAGE 1F-01	

ADRS MUX

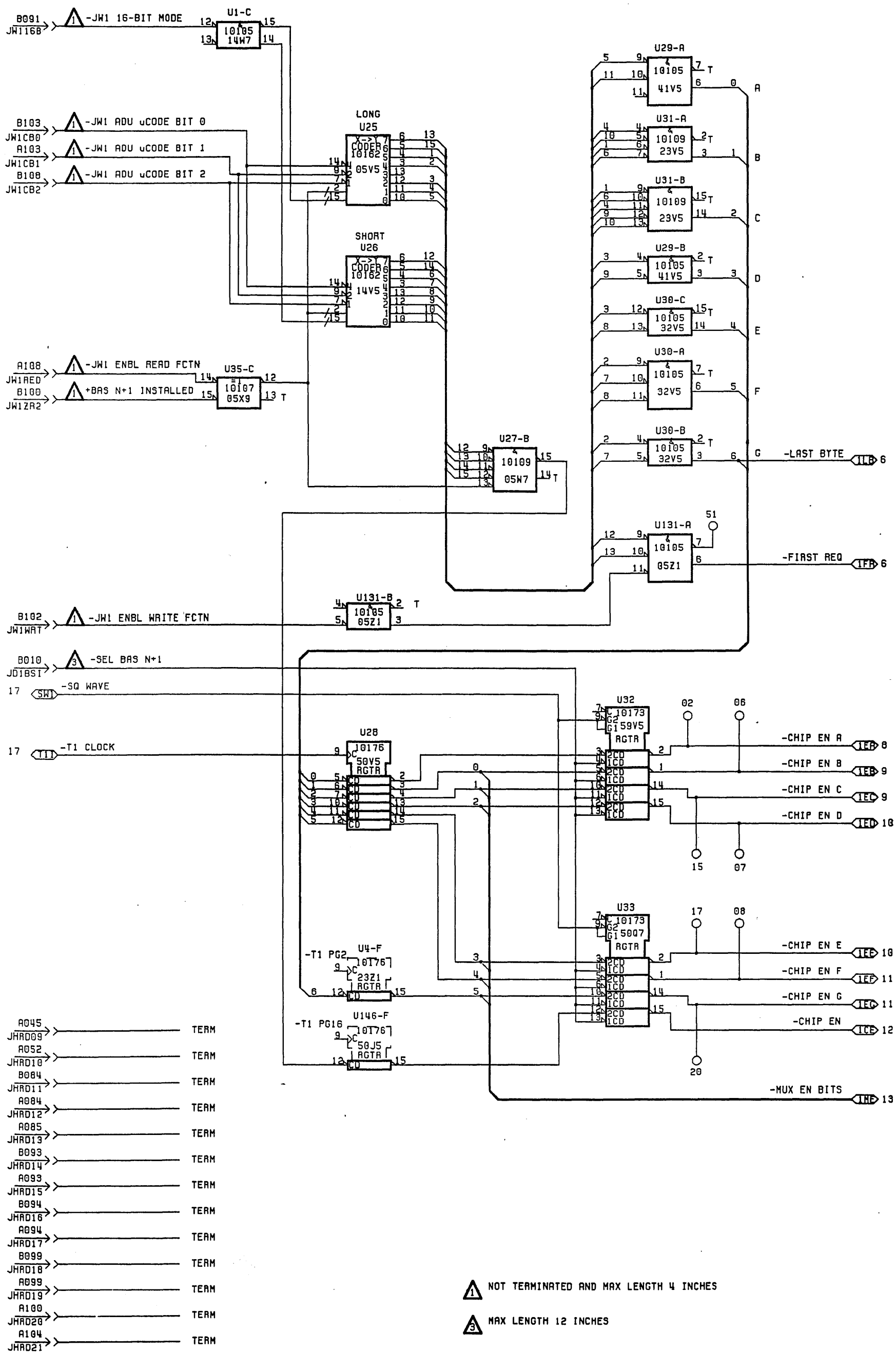


BAS N GEN CHIP ENBLS



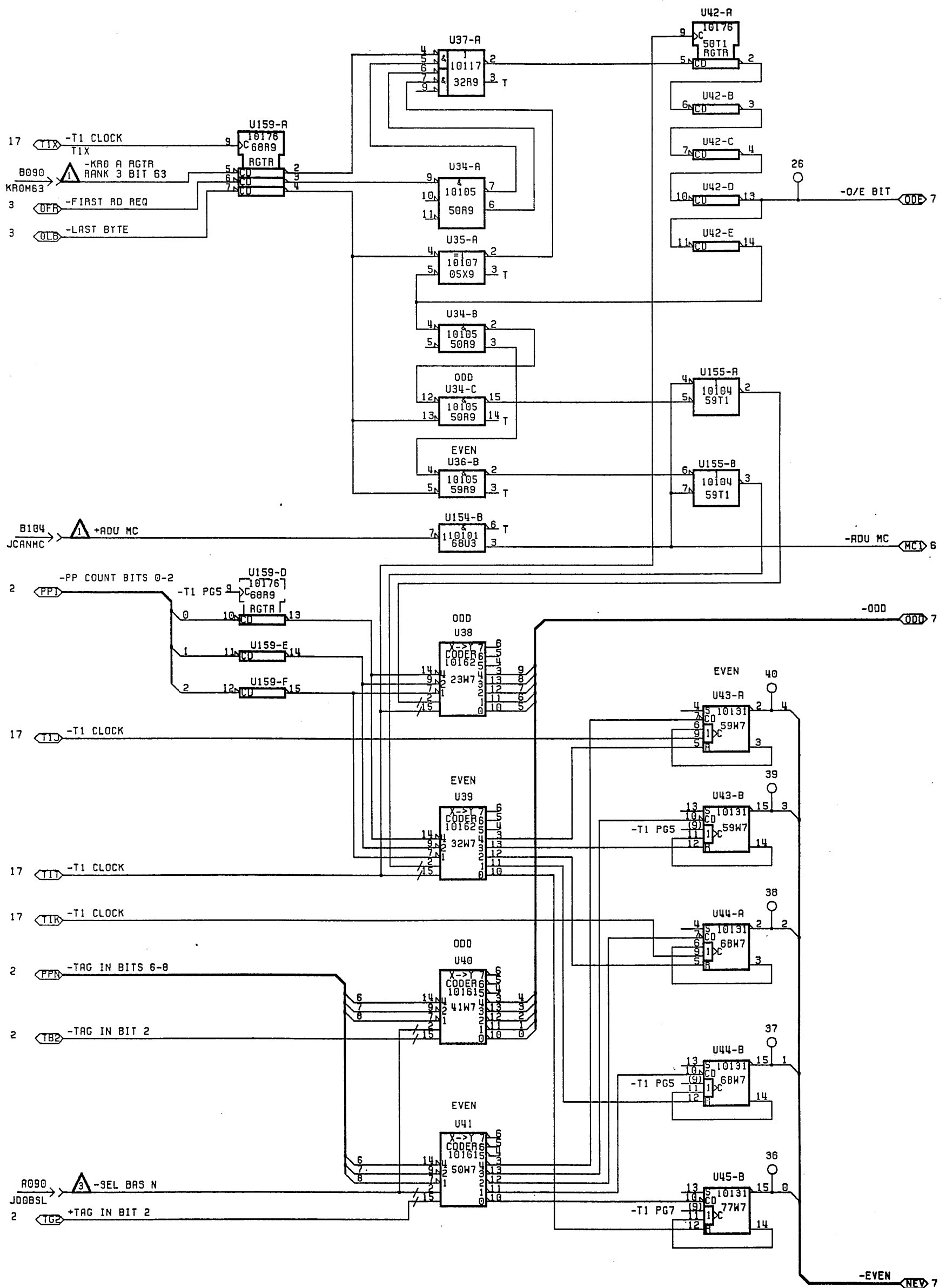
	ADU READ BOARD BAS N GENERATE CHIP ENABLES TYPE 1JFH	B	DWG NO. 53575505	DATE 11/01/85	REV A

BAS N+1 GEN CHIP ENBLS




CONTROL DATA	ADU READ BOARD BAS N+1 GENERATE CHIP ENABLES		DWG NO. B	DATE 11/01/85	REV A
	TYPE 1JFH		SHEET NO. 4	PAGE 60462210	REV JF-04

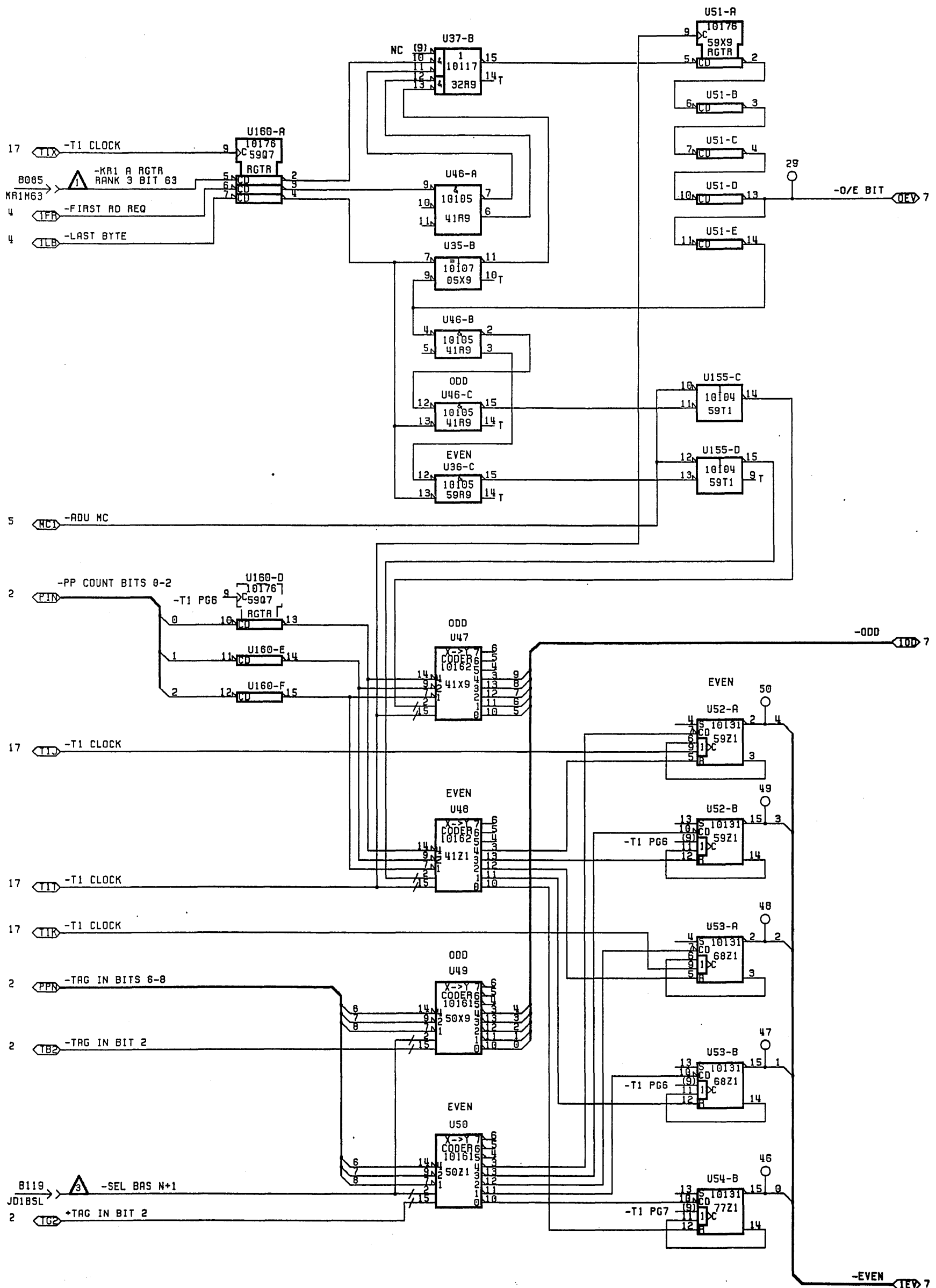
BAS N DATA RDY



- 1 NOT TERMINATED AND MAX LENGTH 4 INCHES
- 3 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD DATA READY BAS N	8	DRG NO. 53575505	DATE 11/01/85	REV A
	TYPE 1JFH	N	SHEET NO. 5	60462210	PAGE 1F-05

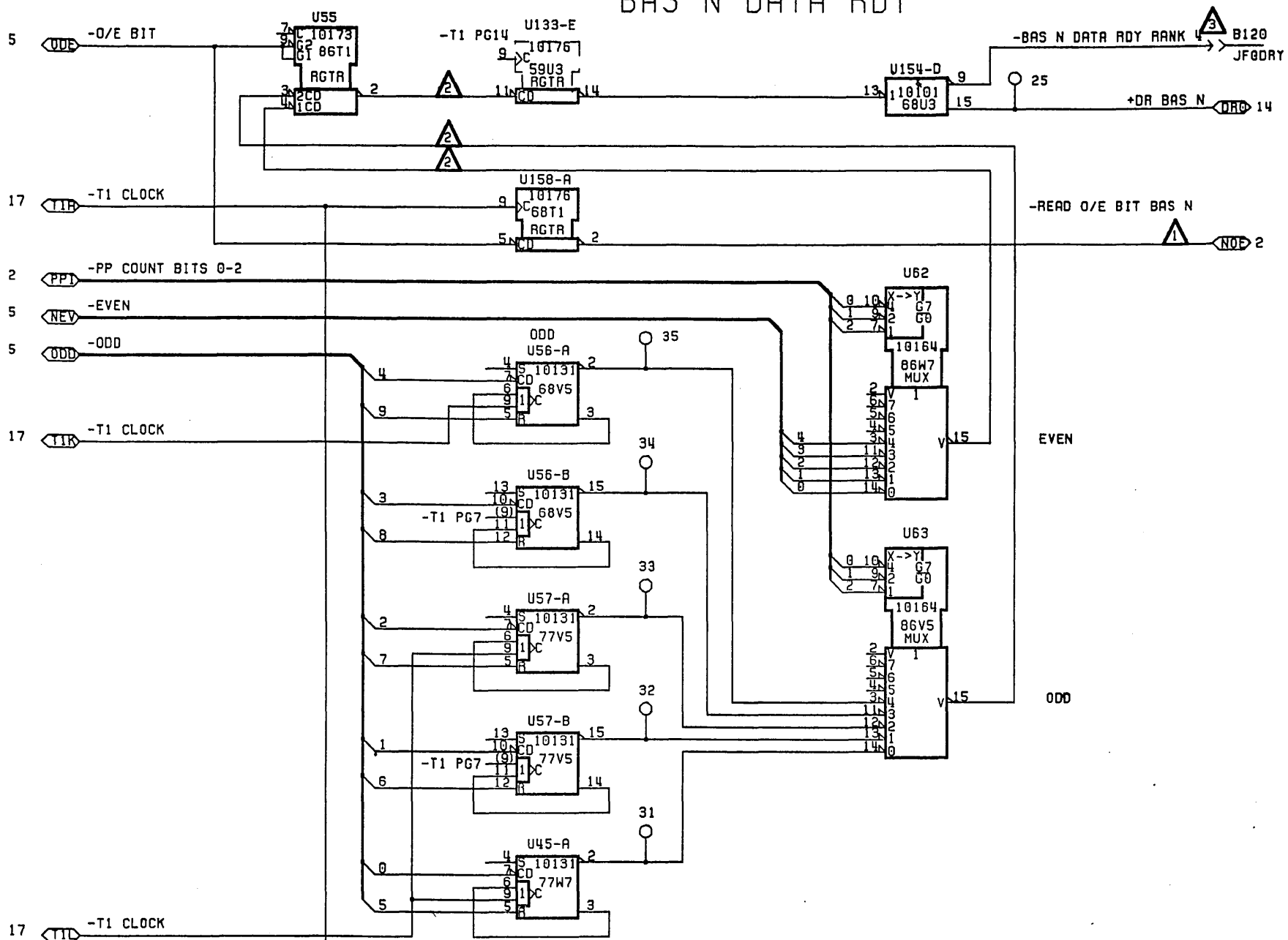
BAS N+1 DATA RDY



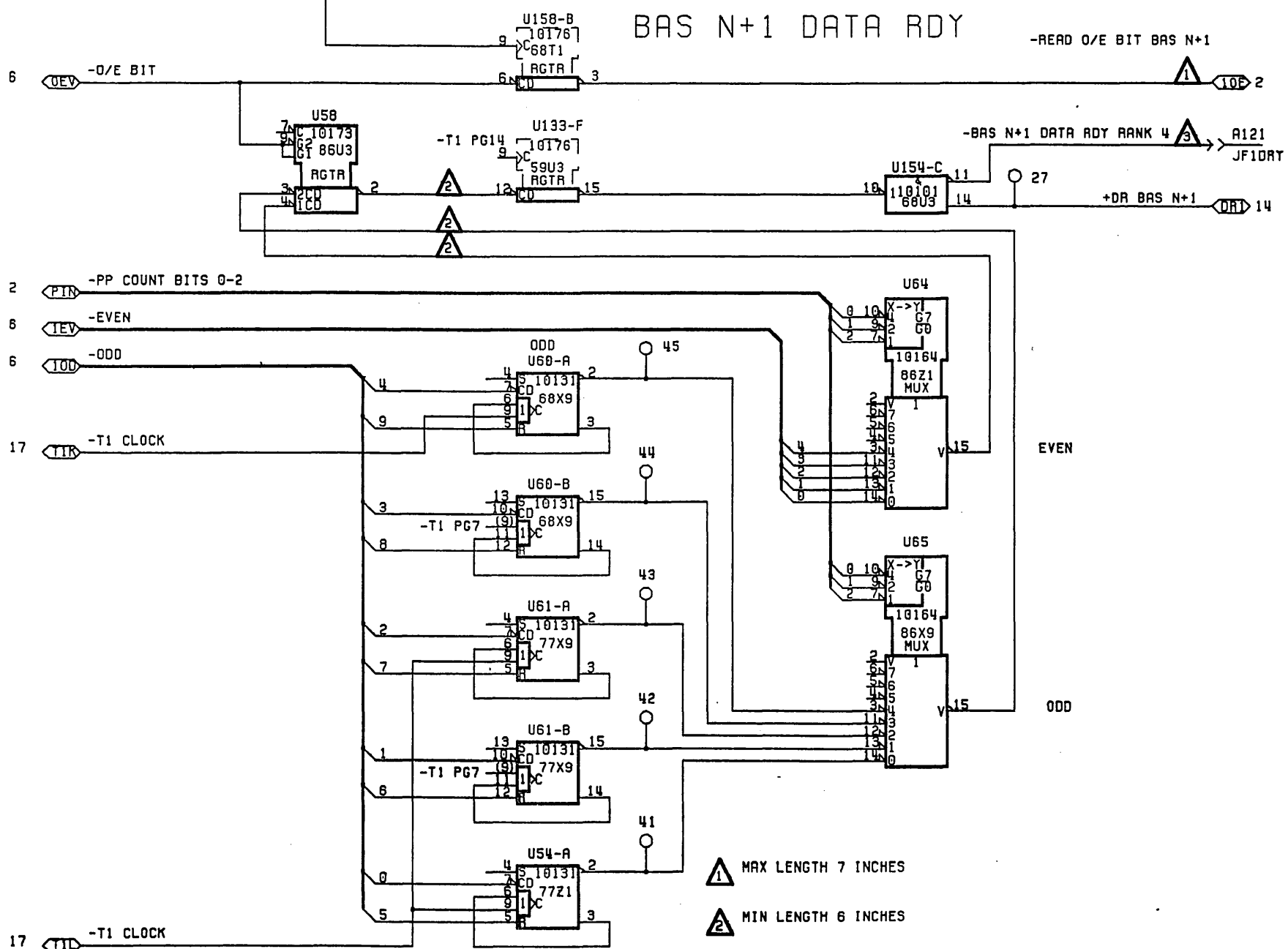
1 NOT TERMINATED AND MAX LENGTH 4 INCHES
 2 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD DATA READY BAS N+1		B	DWG NO. 53575505	DATE 11/01/85	REV A
	TYPE 1JFH			SHEET NO. 6	68462210	PAGE
			N			JF-08


BAS N DATA RDY



BAS N+1 DATA RDY

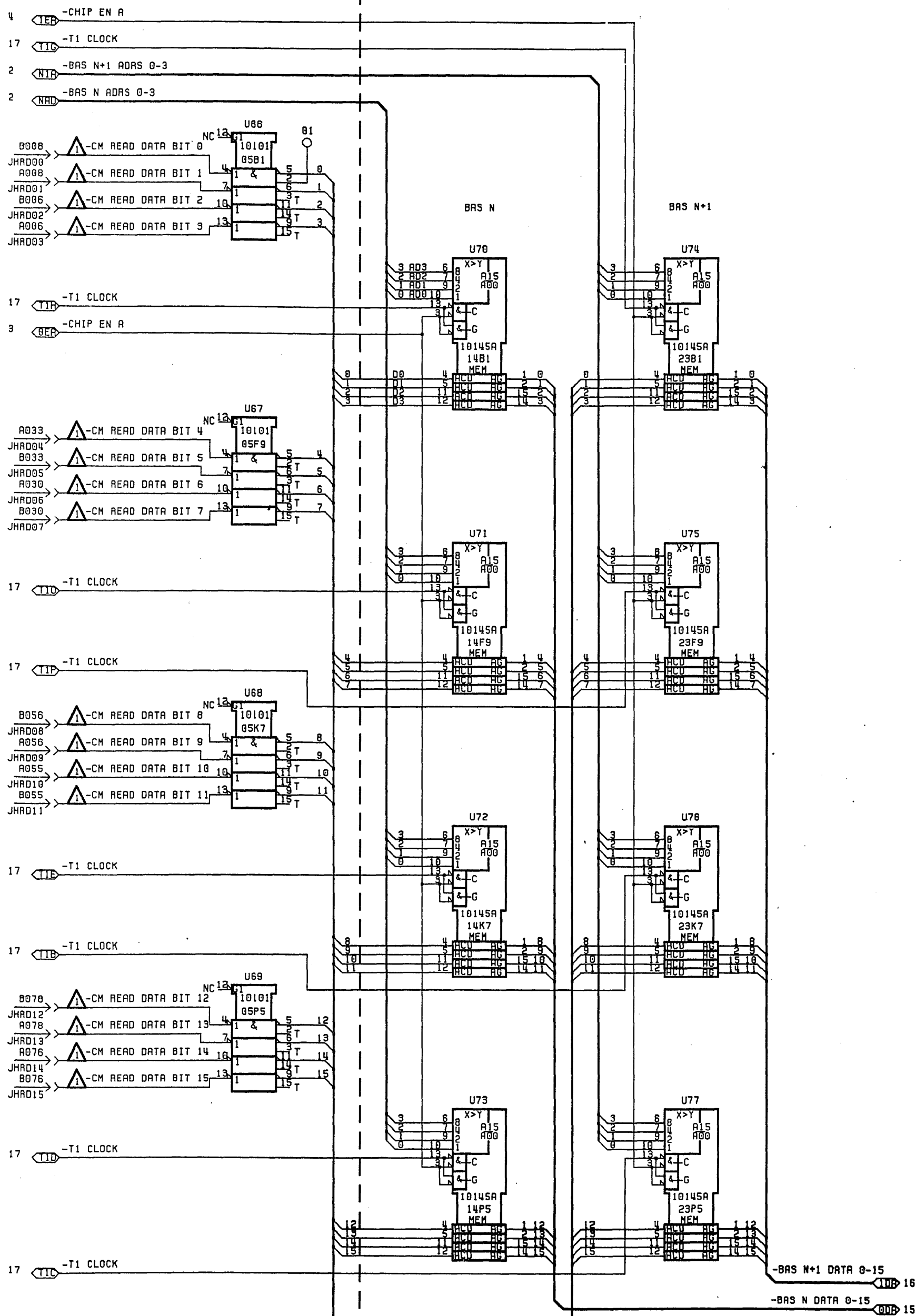


- MAX LENGTH 7 INCHES
- MIN LENGTH 6 INCHES
- MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD DATA READY BAS N AND N+1		B	DWG NO.	DATE	REV
				53575505	11/01/85	A
	TYPE 1JFH		N	SHEET NO. 7	60462210	PAGE

DATA-IN BUFFER
BITS 0-15

DISASSEMBLY RGTR BITS 0-15

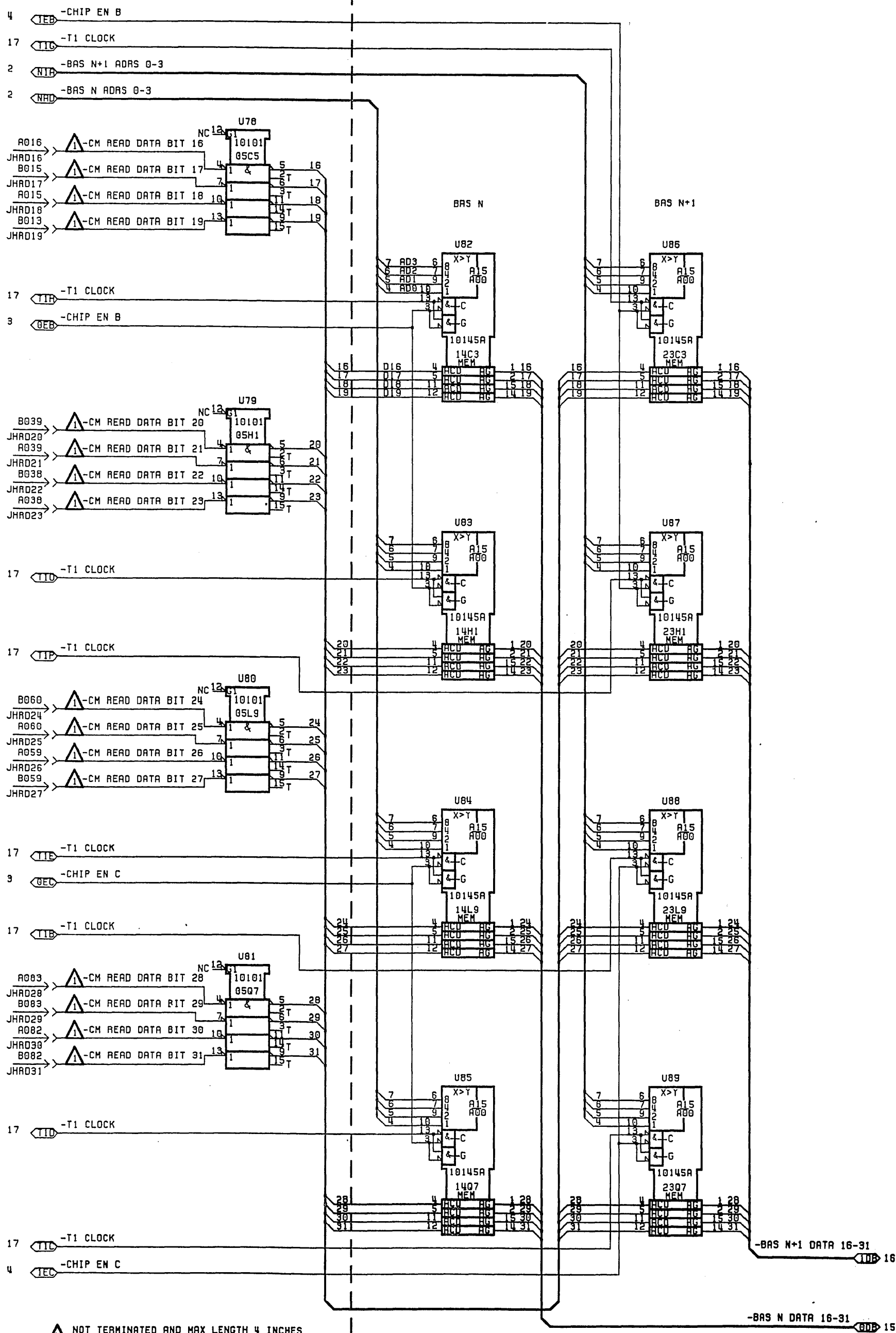


NOT TERMINATED AND MAX LENGTH 4 INCHES

CONTROL DATA	ADV READ BOARD DATA-IN BUFFER AND DISASSEMBLY REG BITS 0-15 TYPE 1JFH		DWG NO. B 53575505	DATE 11/01/85	REV A
	SHEET NO. 8		60462210	PAGE	JF-00

DATA-IN BUFFER BITS 16-31

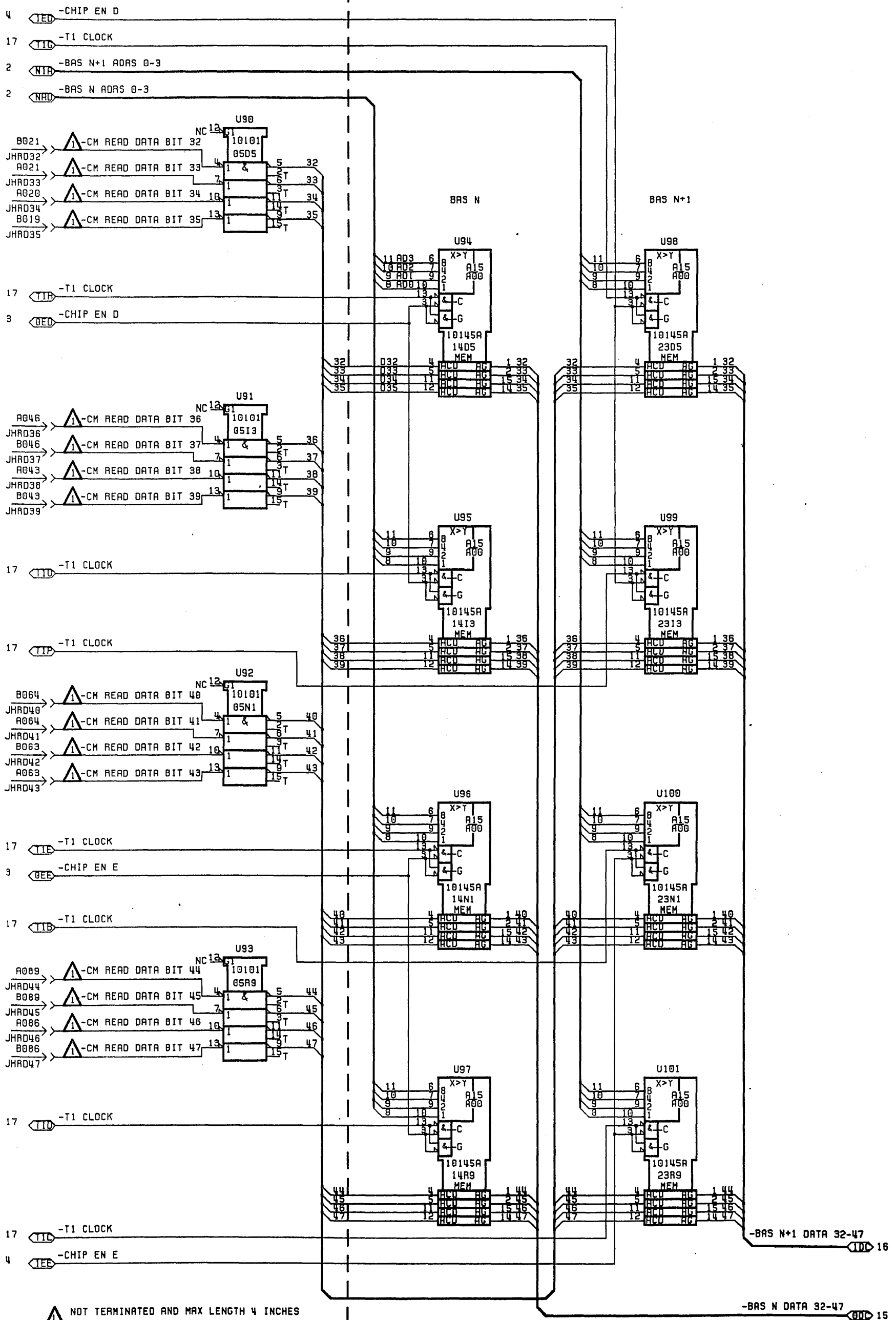
DISASSEMBLY RGTR BITS 16-31




	ADU READ BOARD		DWG NO.	DATE	REV
	DATA-IN BUFFER AND		8	53575505	11/01/85
	DISASSEMBLY REG BITS 16-31		SHEET NO. 9	60462210	PAGE 1F-08
TYPE 1JFH					

DATA-IN BUFFER BITS 32-47

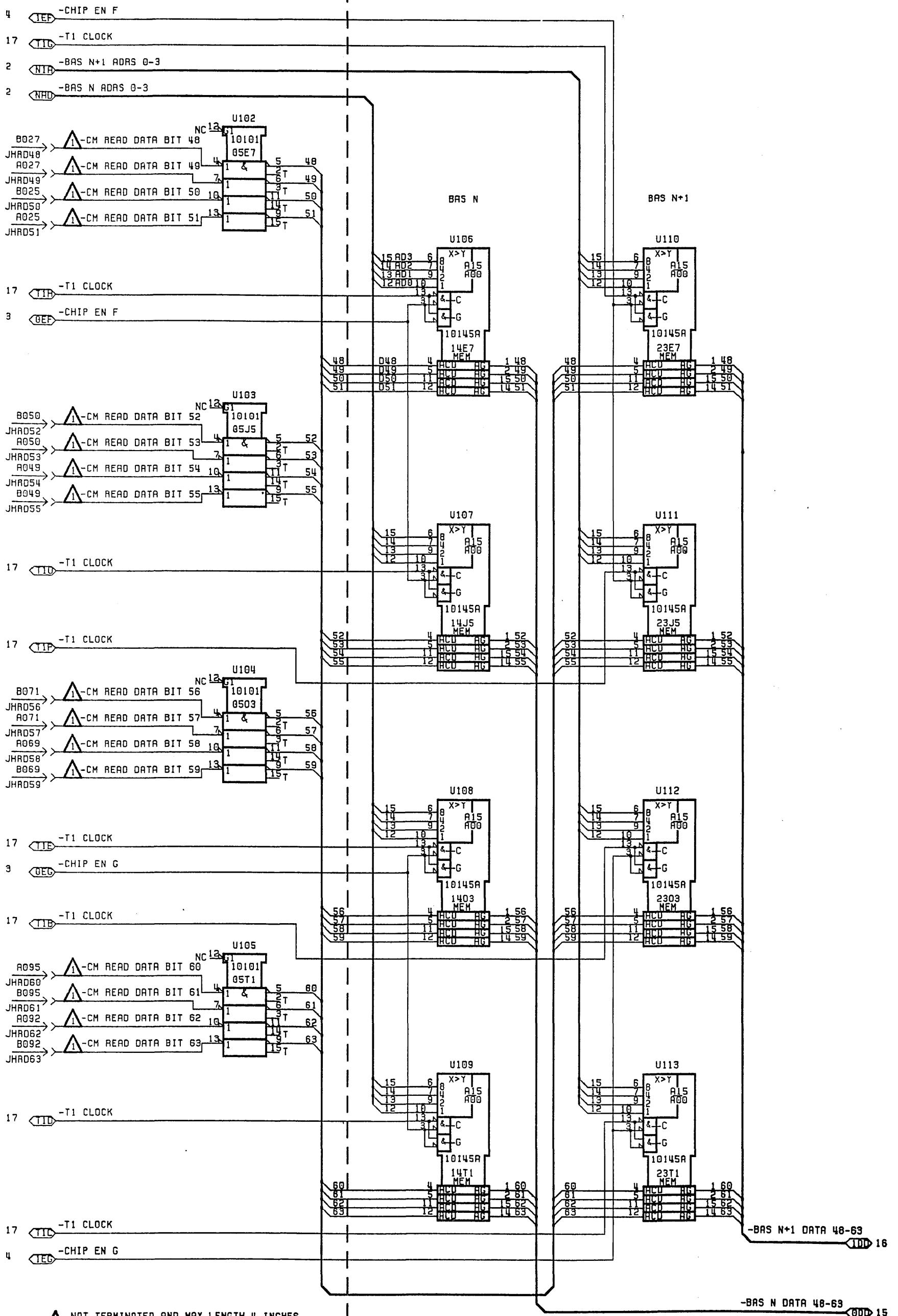
DISASSEMBLY RGTR BITS 32-47




 CONTROL DATA	ADU READ BOARD		B	DWG NO.	DATE	REV
	DATA-IN BUFFER AND			53575505	11/01/85	A
	DISASSEMBLY REG BITS 32-47					
	TYPE 1JFH		N	SHEET NO. 10	60462210	PAGE F-10

DATA-IN BUFFER BITS 48-63

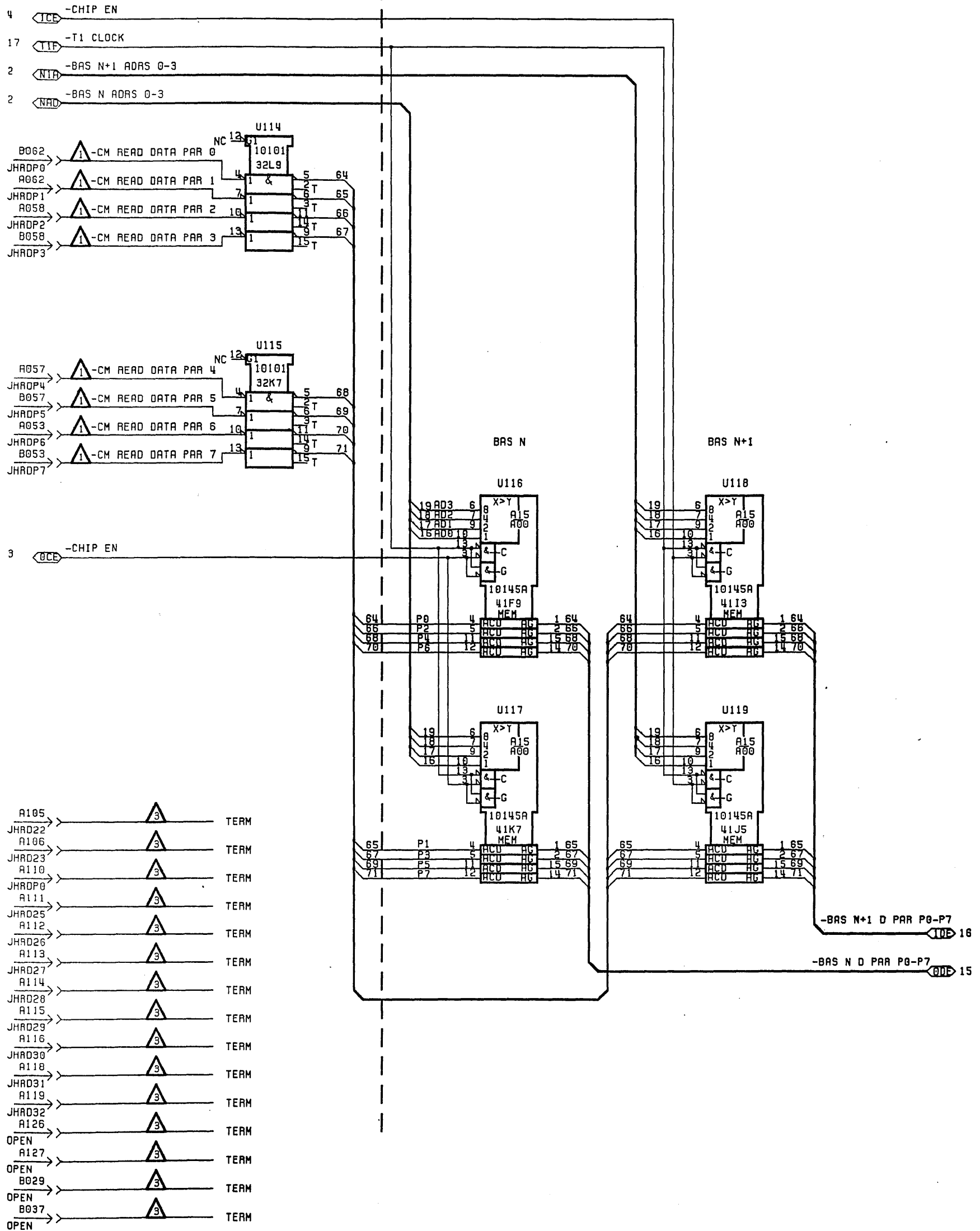
DISASSEMBLY REGTR BITS 48-63




 CONTROL DATA	ADU READ BOARD		8	DWG NO.	DATE	REV
	DATA-IN BUFFER AND			53575505	11/01/85	A
	DISASSEMBLY REG BITS 48-63					
	TYPE 1JFH	N	SHEET NO. 11	60462210	PAGE	JF-11

DATA-IN BUFFER PAR BITS 0-7

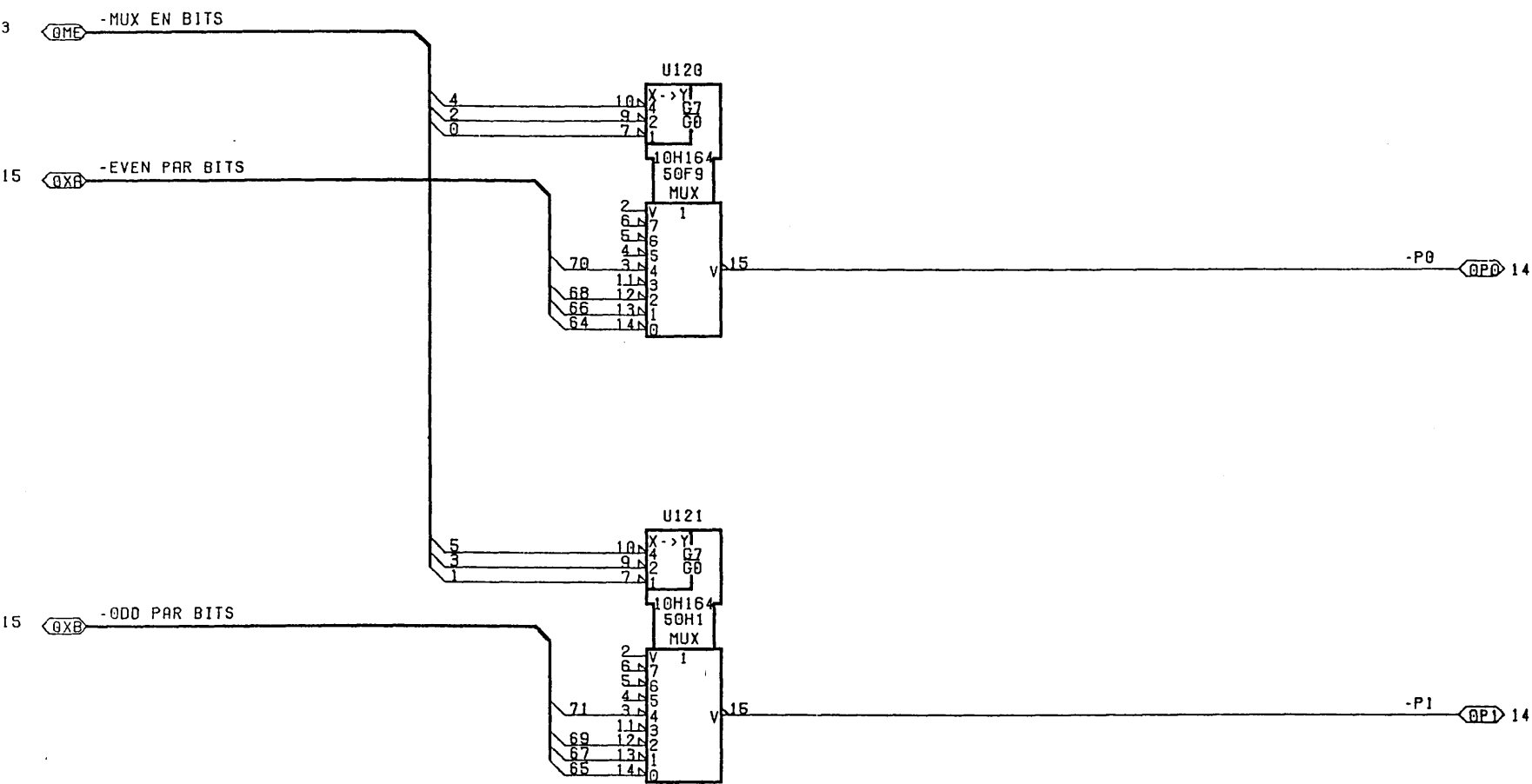
DISASSEMBLY RGTR PAR BITS 0-7



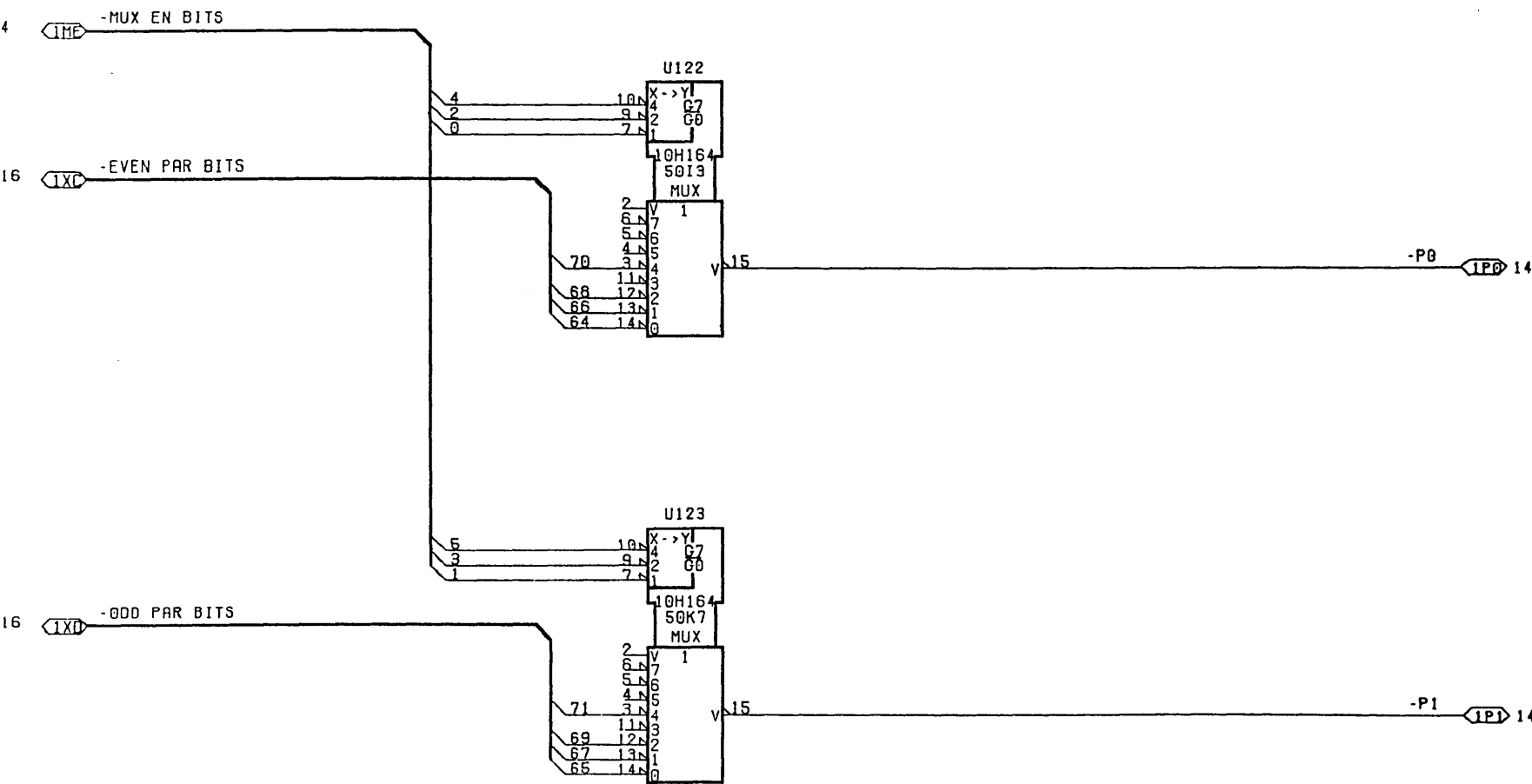
△ NOT TERMINATED AND MAX LENGTH 4 INCHES
 △ MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD DATA-IN BUFFER AND DISASSEMBLY REG PAR BITS P0-P7 TYPE 1JFH	8	DWG NO.	DATE	REV
			53575505	11/01/85	A
			SHEET NO. 12	60462210	PAGE JF-12

BAS N PAR CHECK & GEN

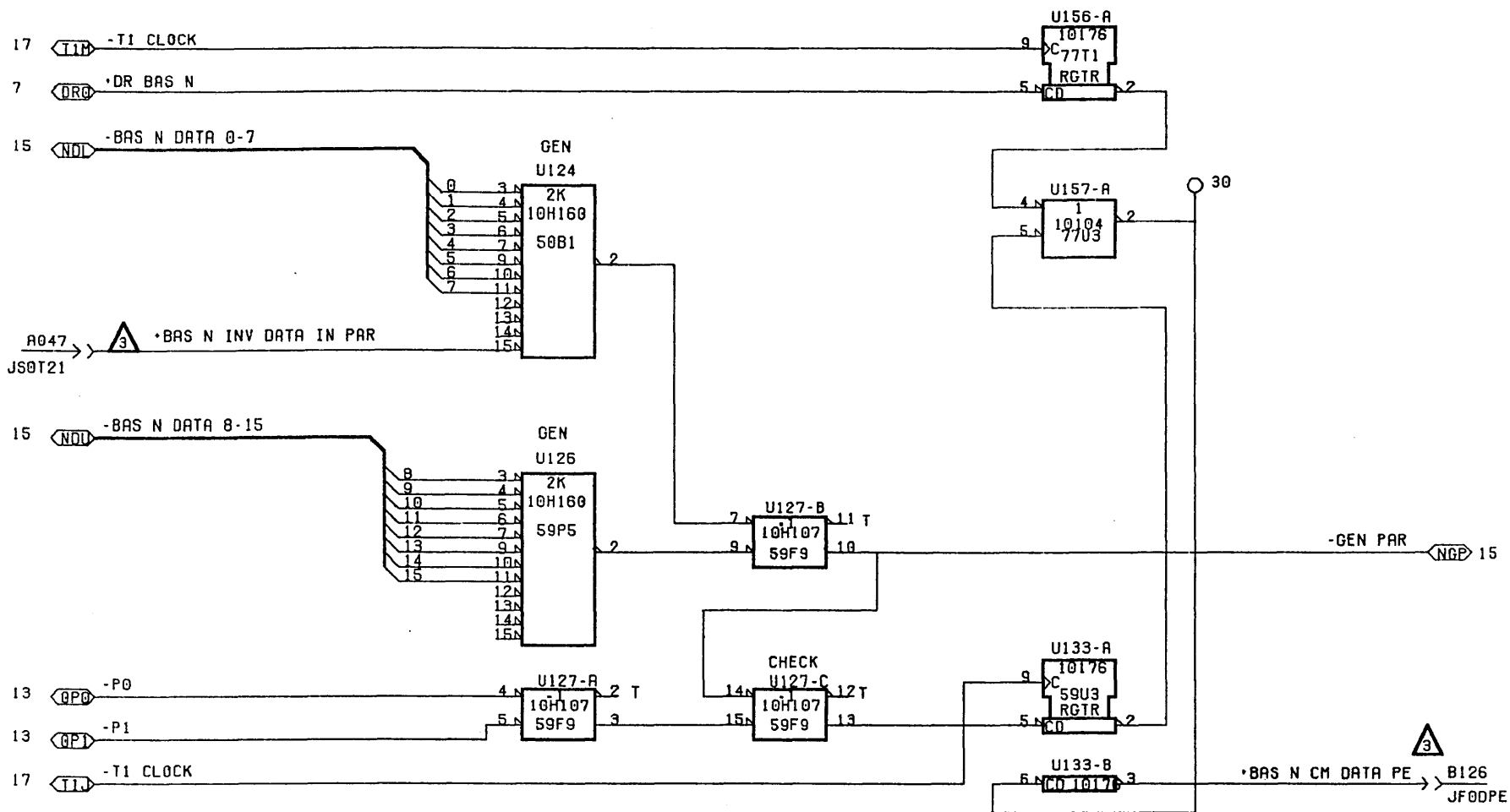


BAS N+1 PAR CHECK & GEN

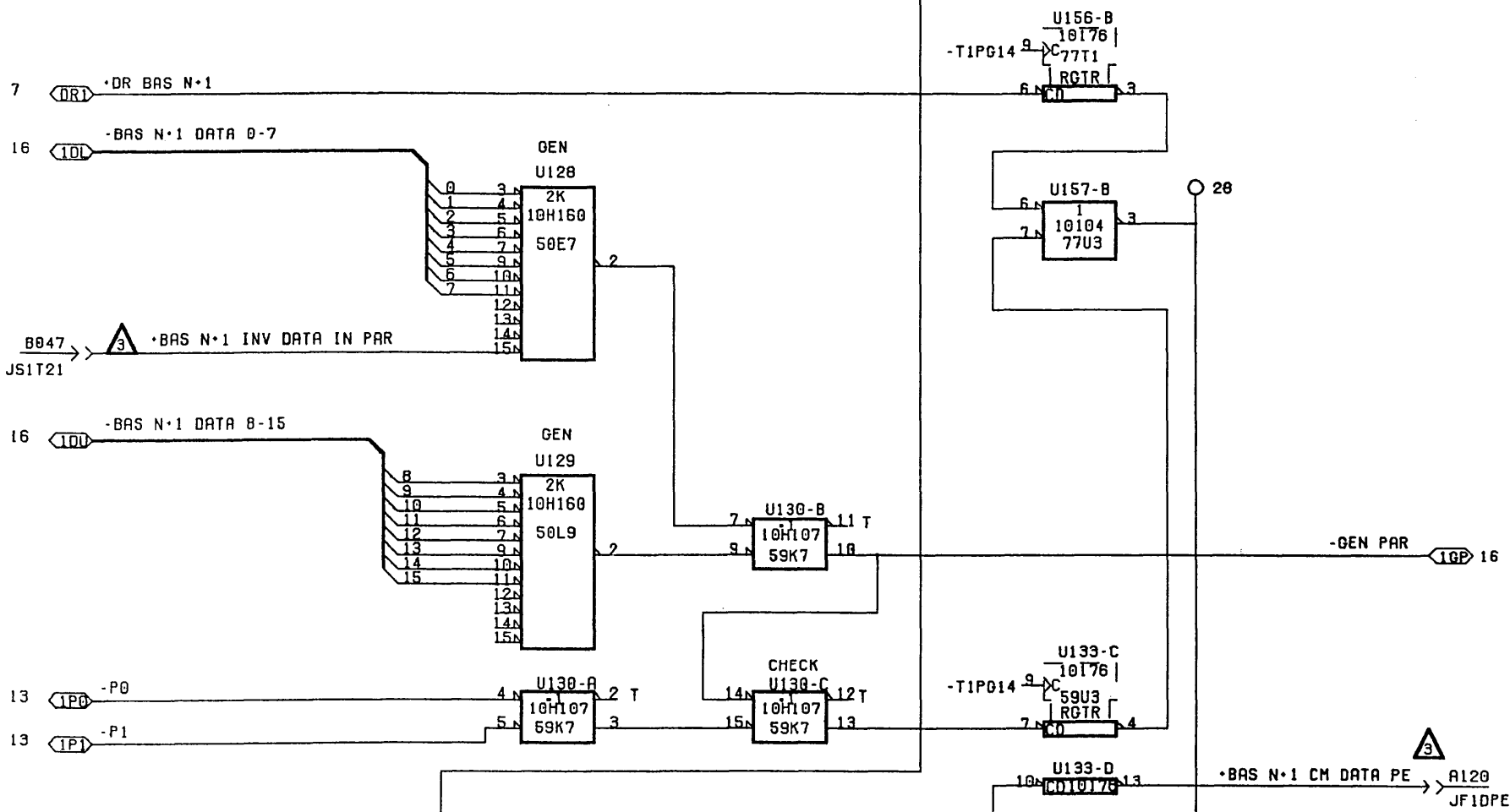


CONTROL DATA	ADU READ BOARD		DWG NO.	DATE	REV
	BAS N AND N+1		8	53575505 03/30/88	D
	PARITY CHECK & GENERATE		SHEET NO. 13	60462210	PAGE 13
TYPE 1JFH					

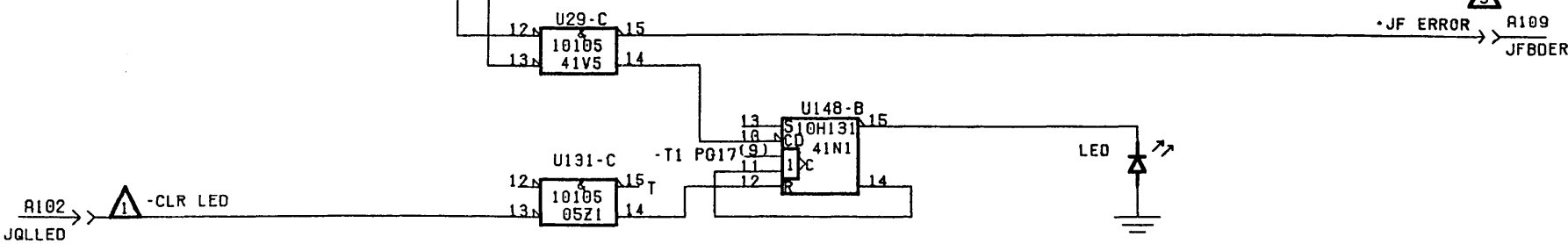
BAS N PAR CHECK & GEN




BAS N+1 PAR CHECK & GEN



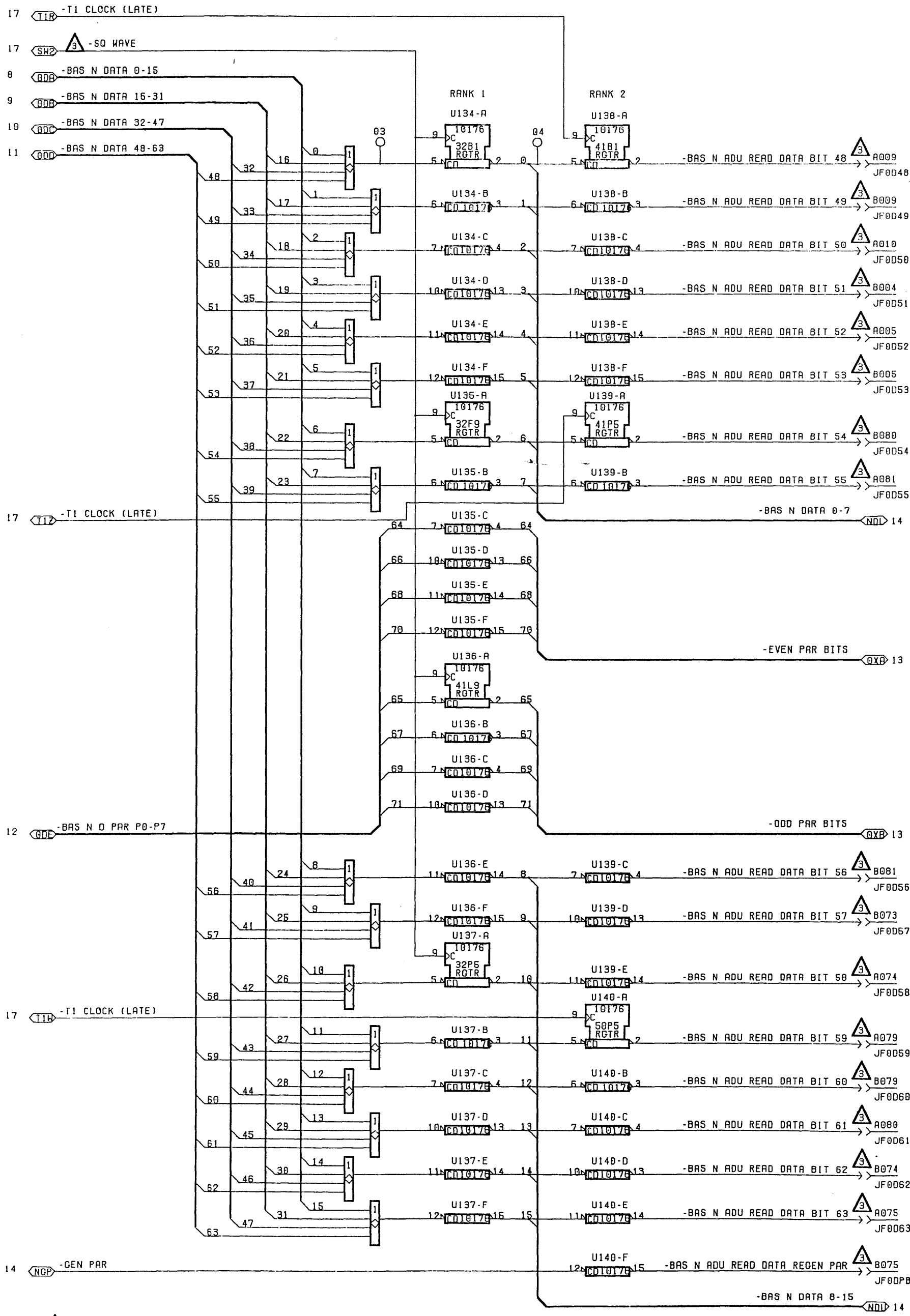
BOARD ERROR



- NOT TERMINATED AND MAX LENGTH 4 INCHES
- MAX LENGTH 12 INCHES

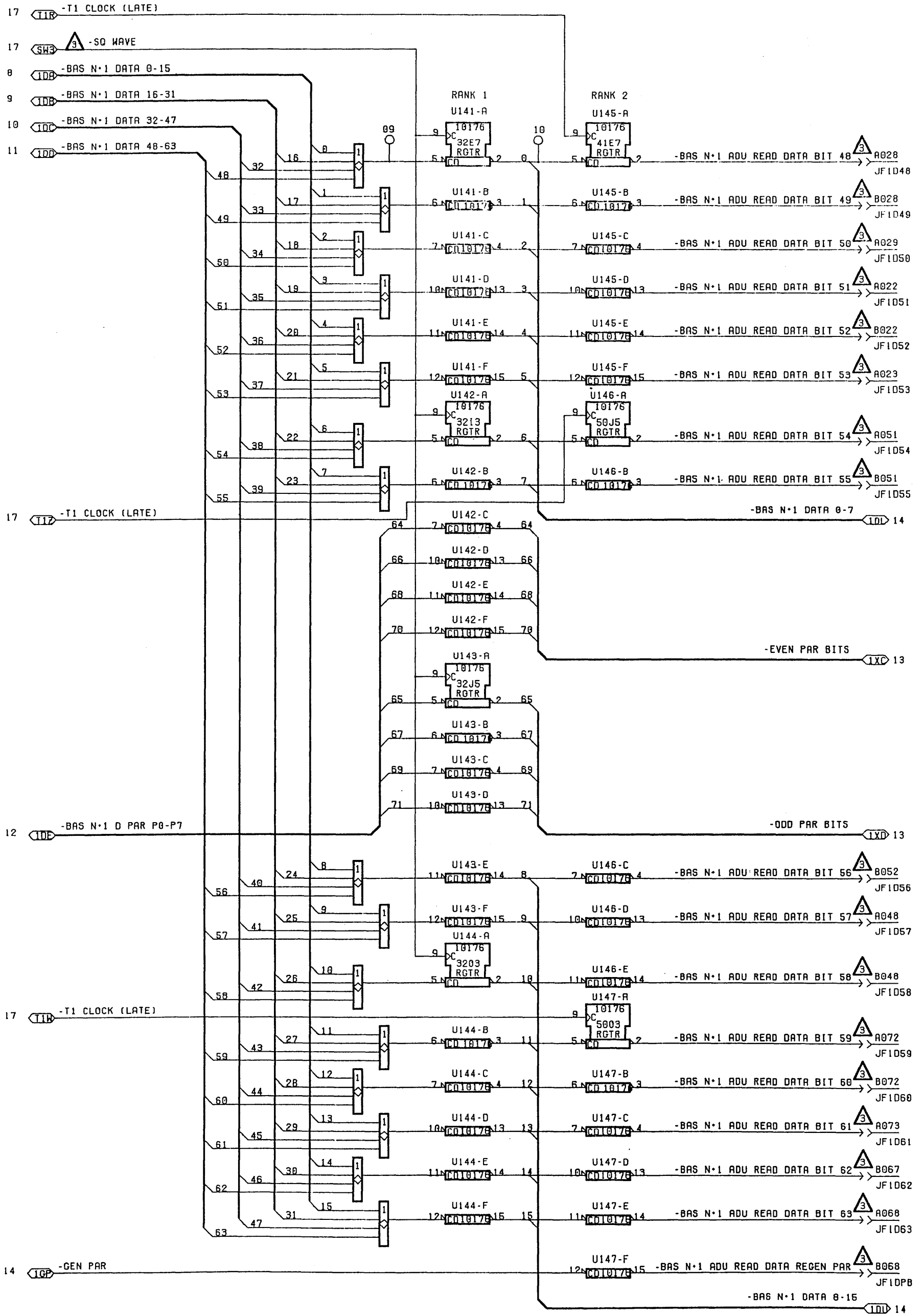
 CONTROL DATA	ADU READ BOARD DATA PAR CHECK AND GENERATE AND BOARD ERROR TYPE 1JFH	B	DWG NO.	DATE	REV
			53575505	03/30/88	D
			SHEET NO. 14		

BAS N DATA OUT RGTR




CD CONTROL DATA	ADU READ BOARD BAS N DATA OUT REGISTER TYPE 1JFH	8	DWG NO. 53575505	DATE 03/30/88	REV D
			SHEET NO. 15	60462210	PAGE JF-15

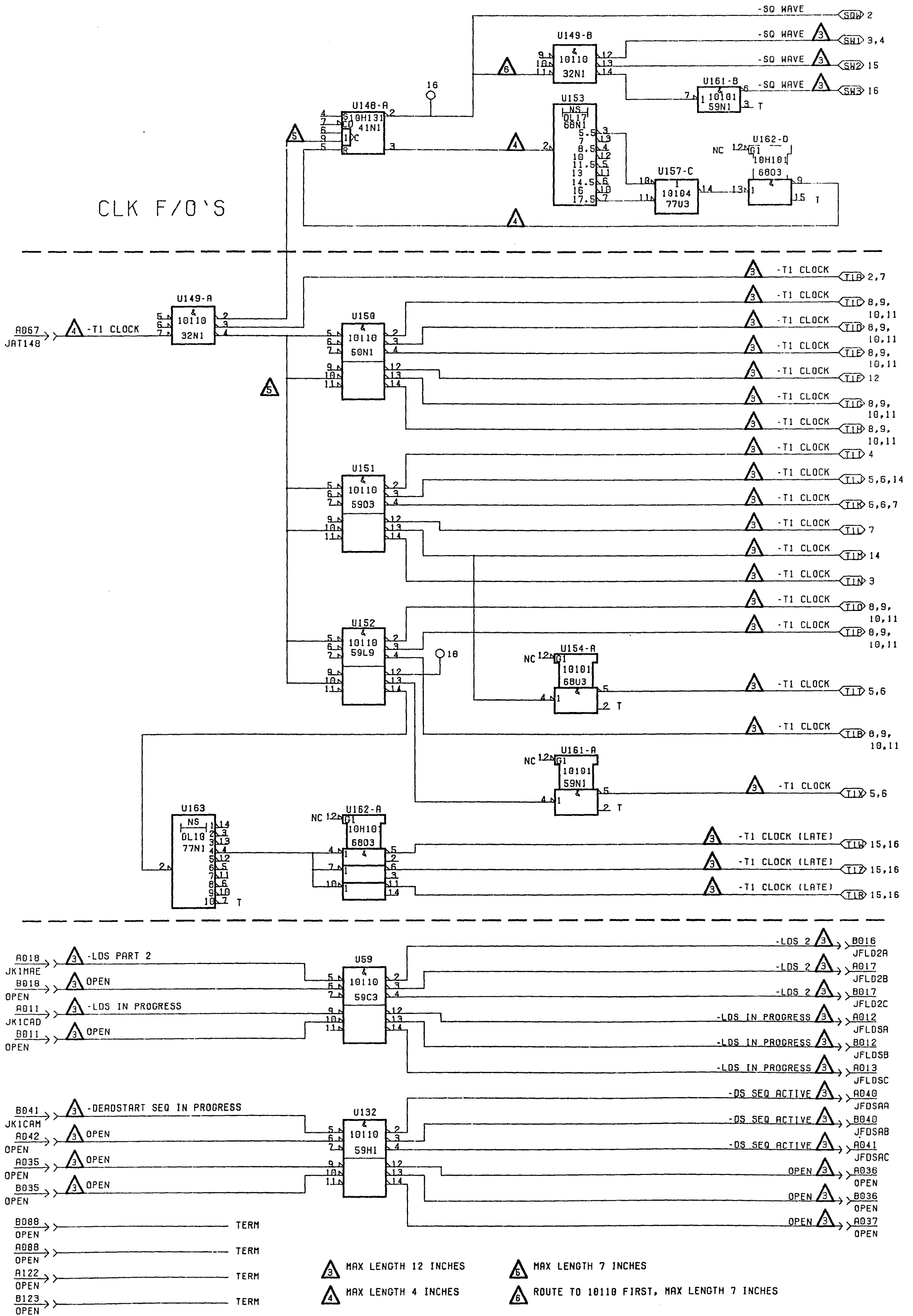
BAS N+1 DATA OUT RGTR



 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD	B	DWG NO.	DATE	REV
	BAS N-1 DATA OUT REGISTER TYPE 1JFH		53575505	03/30/88	D
			SHEET NO. 16	60462210	PAGE 16

SQ WAVE GEN



TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	08	+DATA BIT 0 IN	27	07	+BAS N+1 DATA RDY
02	04	-BAS N+1 CHIP EN A	28	14	+BAS N+1 DATA PE
03	15	-BAS N DATA BIT 48	29	06	-BAS N+1 ODD/EVEN
04	15	-BAS N DATA 48 OUT	30	14	+BAS N DATA PE
05	03	-BAS N CHIP EN B	31	07	-N P0 0 DATA RDY
06	04	-BAS N+1 CHIP EN B	32	07	-N P1 0 DATA RDY
07	04	-BAS N+1 CHIP EN D	33	07	-N P2 0 DATA RDY
08	04	-BAS N+1 CHIP EN F	34	07	-N P3 0 DATA RDY
09	16	-BAS N+1 DATA 48	35	07	-N P4 0 DATA RDY
10	16	-BAS N+1 DATA 48 OUT	36	05	-N P0 E DATA RDY
11	03	-BAS N CHIP EN D	37	05	-N P1 E DATA RDY
12	03	-BAS N CHIP EN F	38	05	-N P2 E DATA RDY
13			39	05	-N P3 E DATA RDY
14			40	05	-N P4 E DATA RDY
15	04	-BAS N+1 CHIP EN C	41	07	-N+1 P0 0 DATA RDY
16	17	-SQUARE WAVE	42	07	-N+1 P1 0 DATA RDY
17	04	-BAS N+1 CHIP EN E	43	07	-N+1 P2 0 DATA RDY
18	17	-T1 CLOCK	44	07	-N+1 P3 0 DATA RDY
19	03	-BAS N CHIP EN A	45	07	-N+1 P4 0 DATA RDY
20	04	-BAS N+1 CHIP EN G	46	06	-N+1 P0 E DATA RDY
21	03	-BAS N CHIP EN C	47	06	-N+1 P1 E DATA RDY
22	03	-BAS N CHIP EN E	48	06	-N+1 P2 E DATA RDY
23	03	+BAS N FIRST REQ	49	06	-N+1 P3 E DATA RDY
24	03	-BAS N CHIP EN G	50	06	-N+1 P4 E DATA RDY
25	07	+BAS N DATA RDY	51	04	+BAS N+1 FIRST REQ
26	05	-BAS N ODD/EVEN			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 [NOT USED]
TERM	A003, B003, A004, B020, B023, A026, B026, B029, A031, B031, A032, B032, B037, B042, A045, B045, A052, A084, B084, A085, A088, B088, A093, B093, A094, B094, A099, B099, A100, A104, A105, A106, A110, A111, A112, A113, A114, A115, A116, A118, A119, A122, B123, A126, A127
UNUSED	B105, B106, B110, B111, B112, B114, B115, B116, B118, A123, B127, A128, B128

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.


ADU READ BOARD

[illegible]

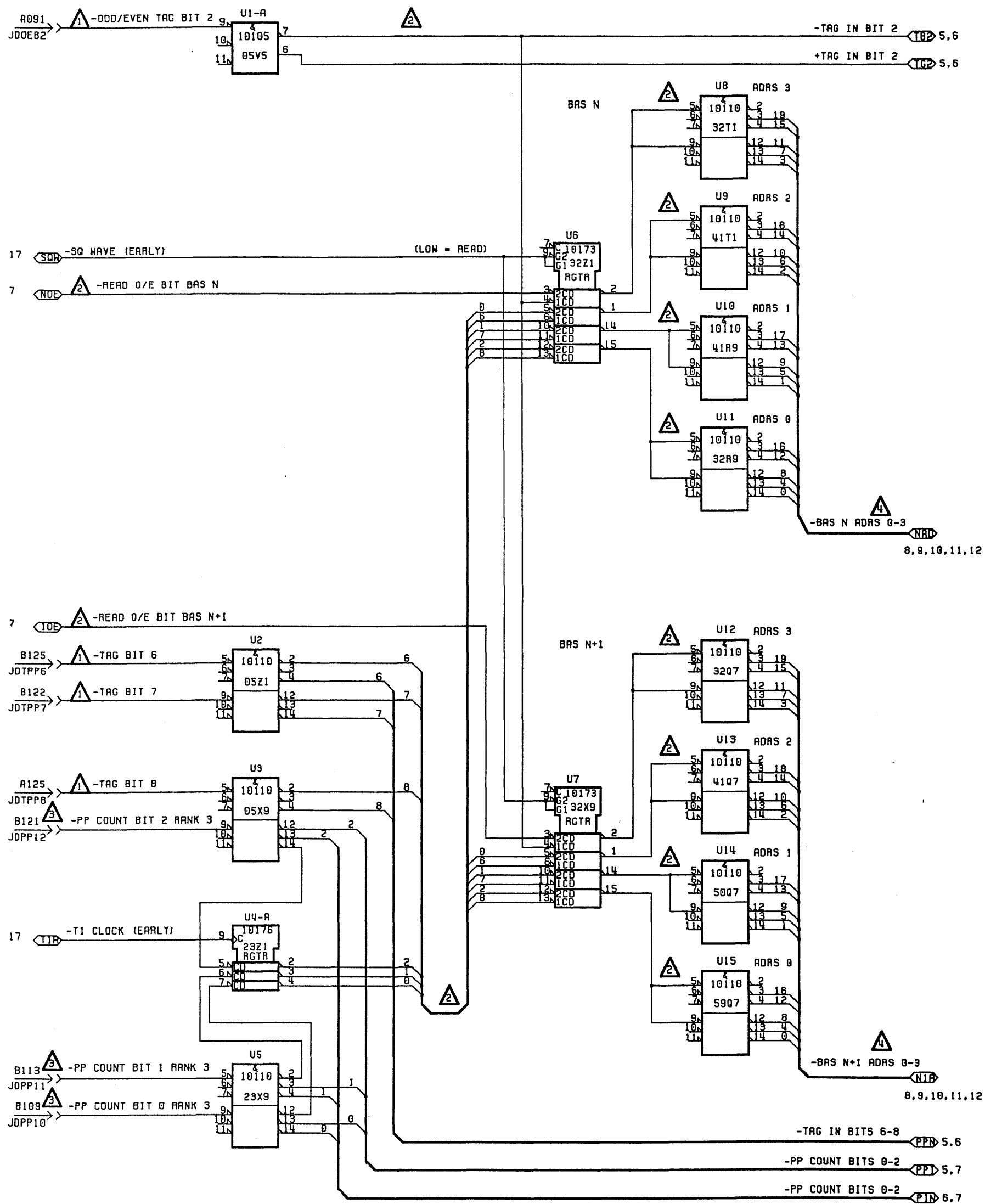
NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED


LOC: A18, A17, A16

DWN	L H JOHNSON	04/04/86
CHKD	D R FORD	04/24/86
ENG	W E DIETHART	04/24/86
PUBS	R K BONDE	04/24/86
APP	W E DIETHART	04/24/86

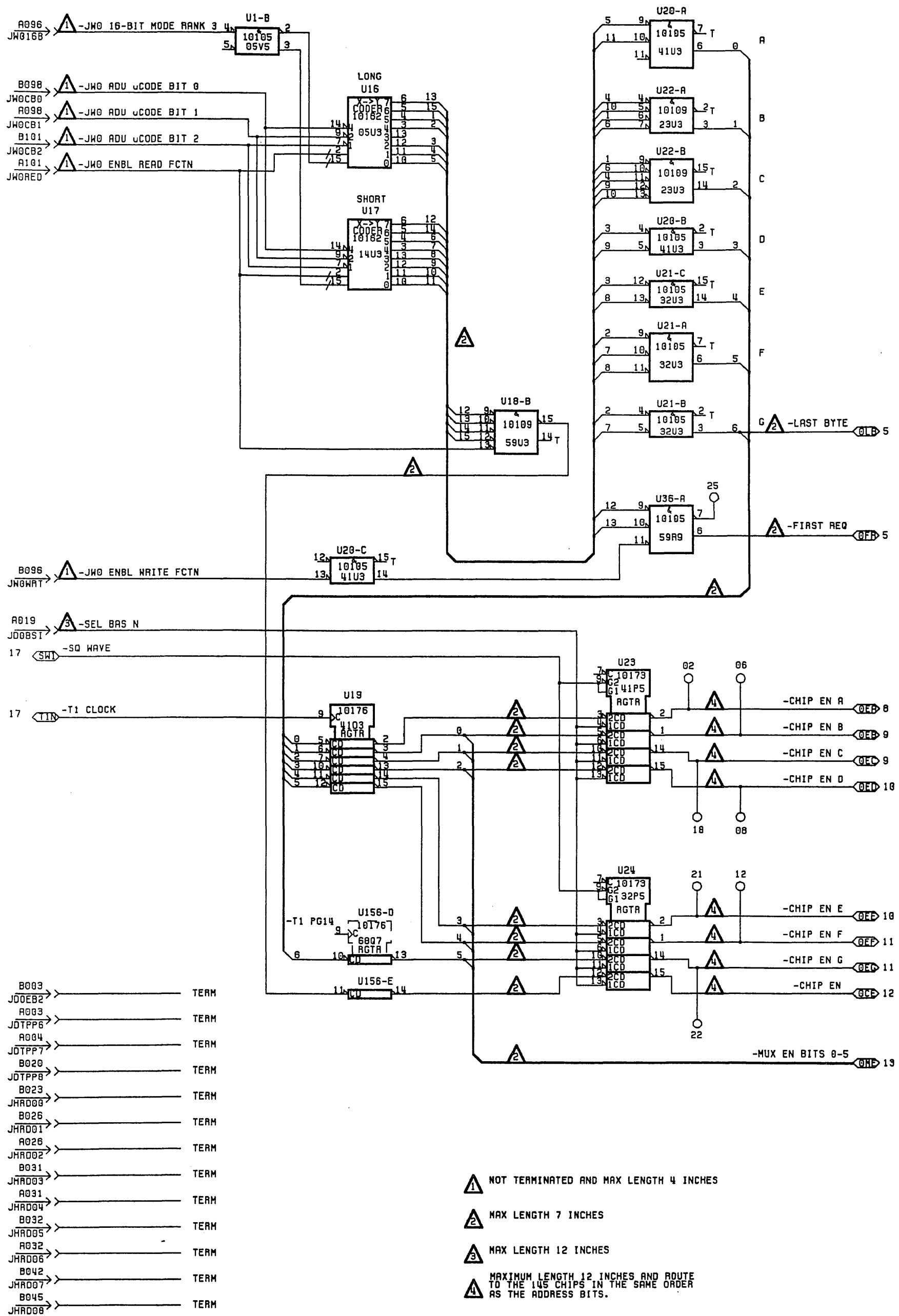
 CONTROL DATA	REVISION HISTORY TYPE 1JFH	B	DWG NO.	DATE	REV
			22105620	03/30/88	C
SHEET NO. 1		60462210		PAGE JF-01	

ADRS MUX



 CONTROL DATA	ADU READ BOARD ADDRESS MUX		B	DWG NO.	DATE	REV
				22105620	04/04/86	A
	TYPE 1JFH			SHEET NO. 2	60462210	PAGE JF-02

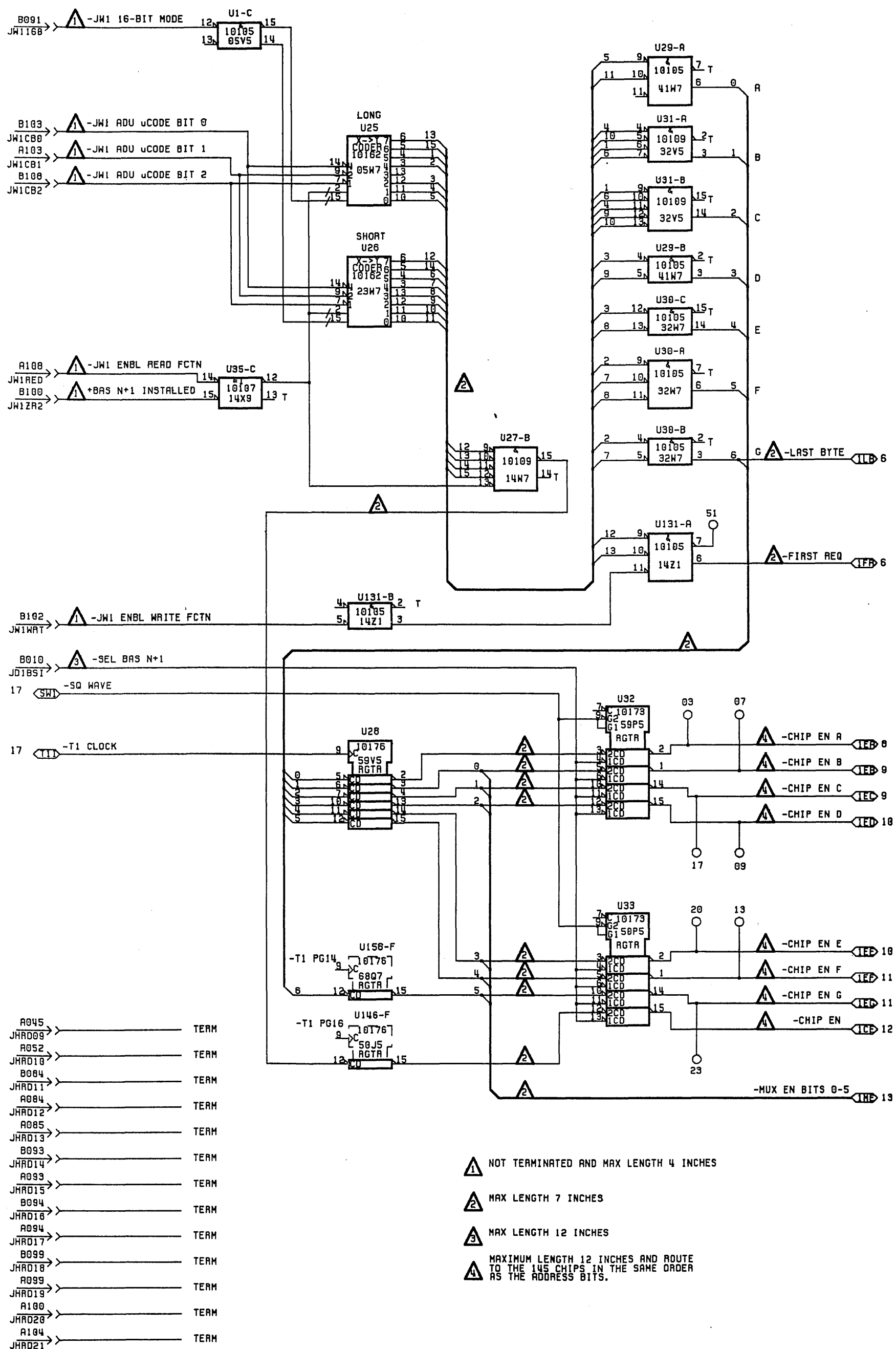
BAS N GEN CHIP ENBLS



B003	J00E02	TEAM
A003	J00E03	TEAM
A004	J00E04	TEAM
A005	J00E05	TEAM
A006	J00E06	TEAM
A007	J00E07	TEAM
A008	J00E08	TEAM
A009	J00E09	TEAM
A010	J00E10	TEAM
A011	J00E11	TEAM
A012	J00E12	TEAM
A013	J00E13	TEAM
A014	J00E14	TEAM
A015	J00E15	TEAM
A016	J00E16	TEAM
A017	J00E17	TEAM
A018	J00E18	TEAM
A019	J00E19	TEAM
A020	J00E20	TEAM
A021	J00E21	TEAM
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A145	J00E145	TEAM

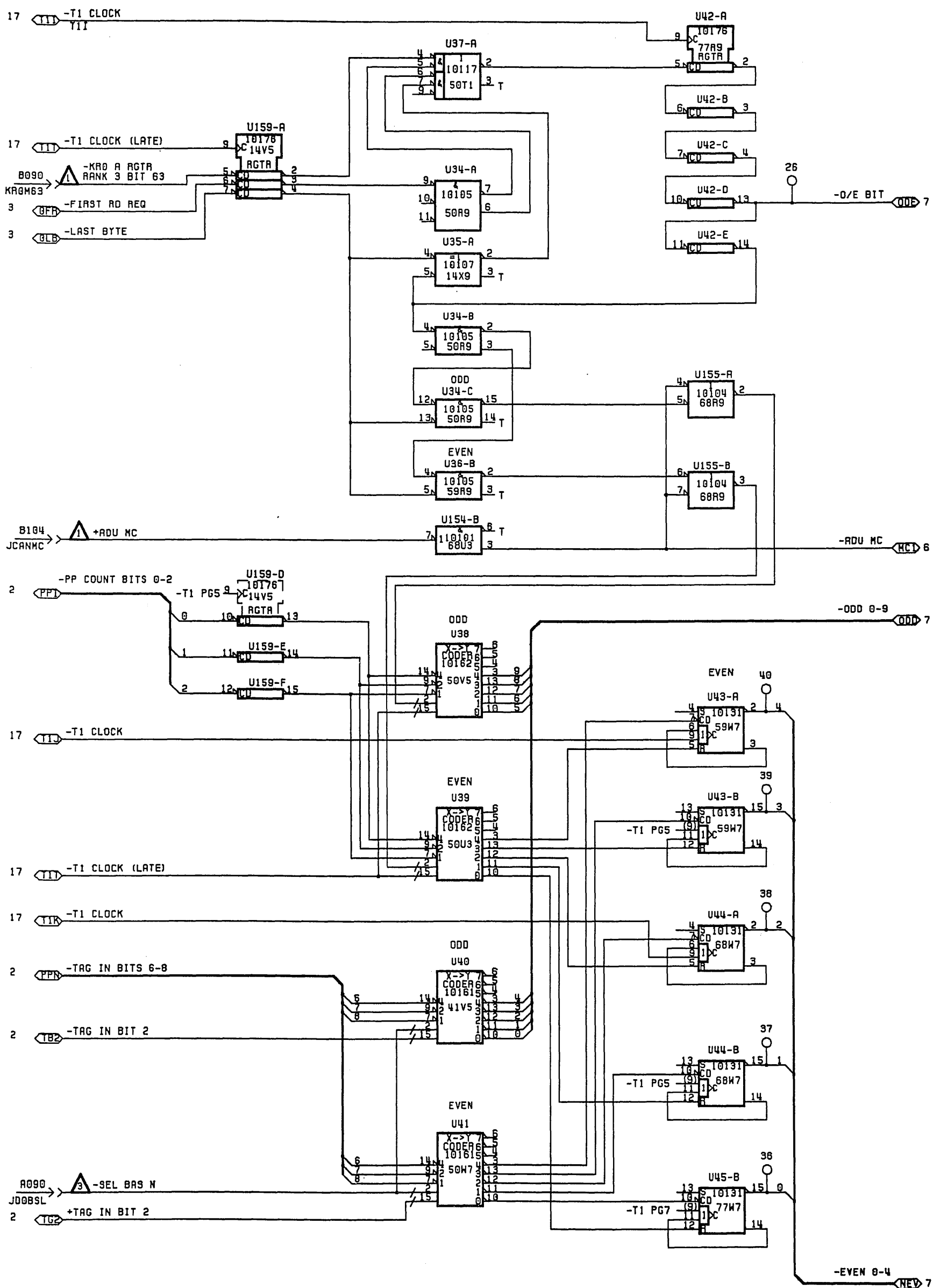
CONTROL DATA	ADU READ BOARD BAS N GENERATE CHIP ENBLS TYPE 1JFH	8	DWG NO.	DATE	REV
			22105620	04/04/86	A
N		SHEET NO.	3	60462210	PAGE JF-09

BAS N+1 GEN CHIP ENBLS




CONTROL DATA	ADU READ BOARD BAS N+1 GENERATE CHIP ENABLES TYPE 1JFH	B	DWG NO. 22105620	DATE 04/04/86	REV A
			SHEET NO. 4	60462210	PAGE JF-04

BAS N DATA RDY

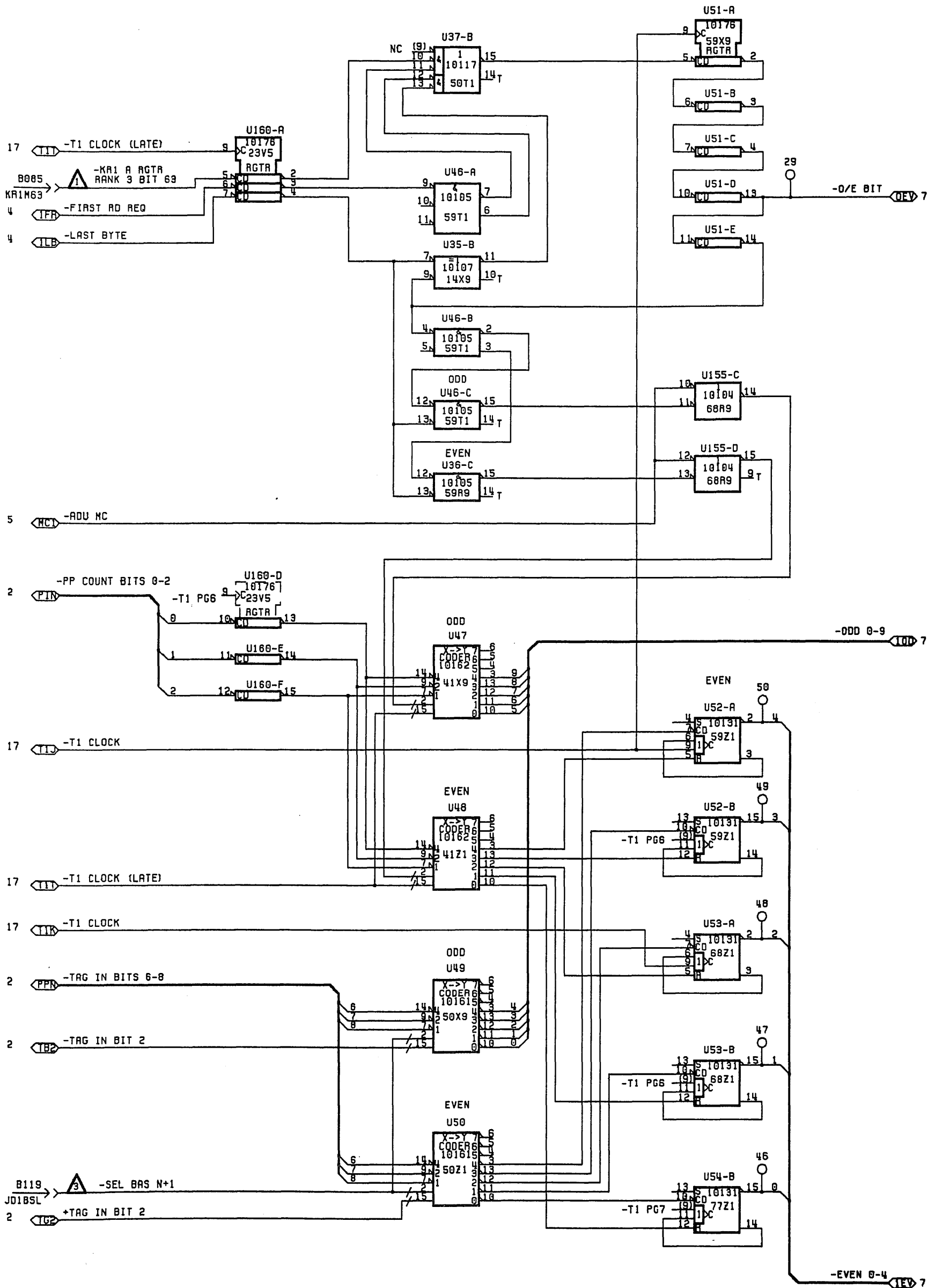


1 NOT TERMINATED AND MAX LENGTH 4 INCHES

3 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD DATA READY BAS N	B	DWG NO. 22105620	DATE 04/04/86	REV A
	TYPE 1JFH	SHEET NO. 5		60462210	PAGE JF-05

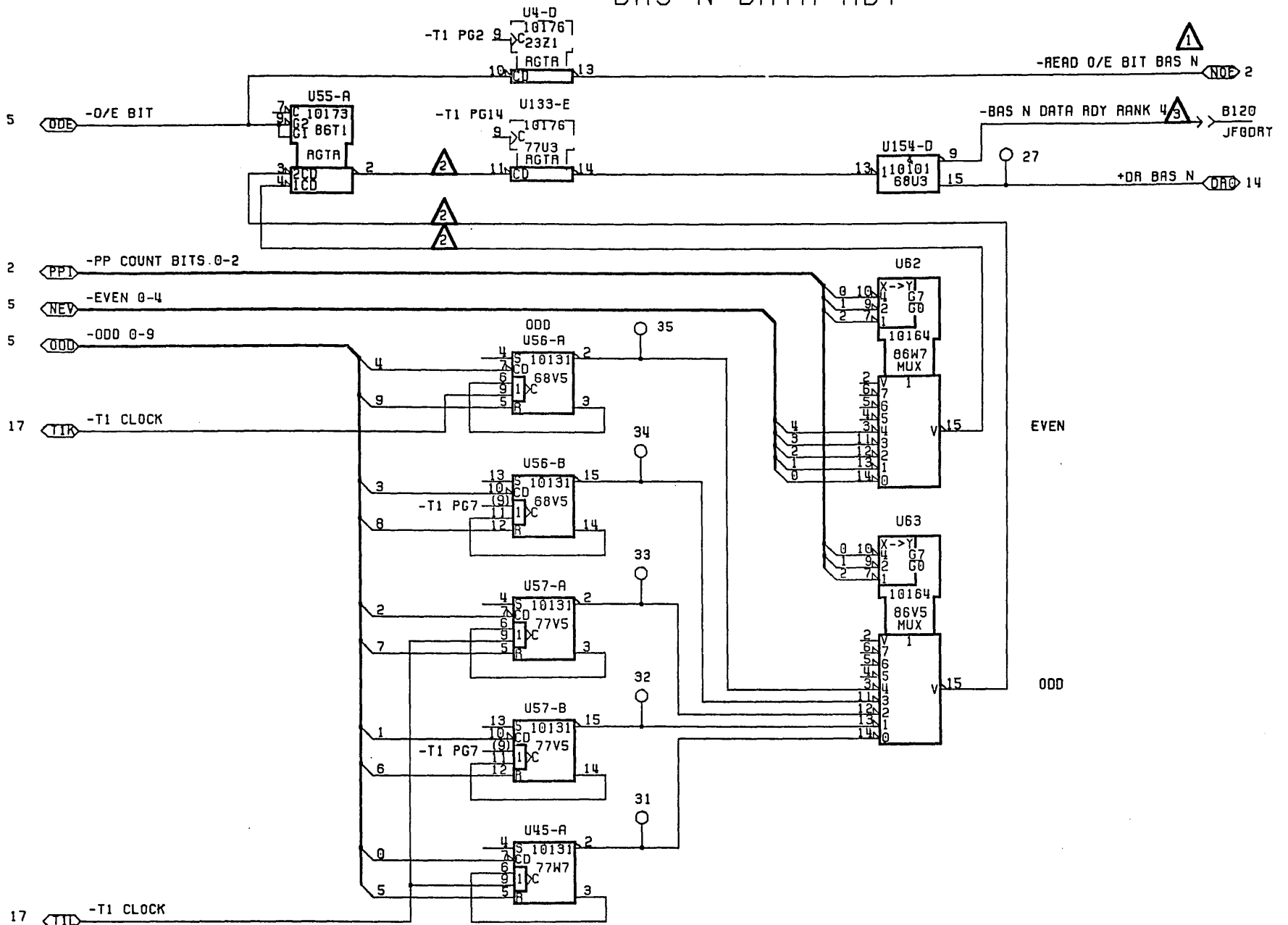
BAS N+1 DATA RDY



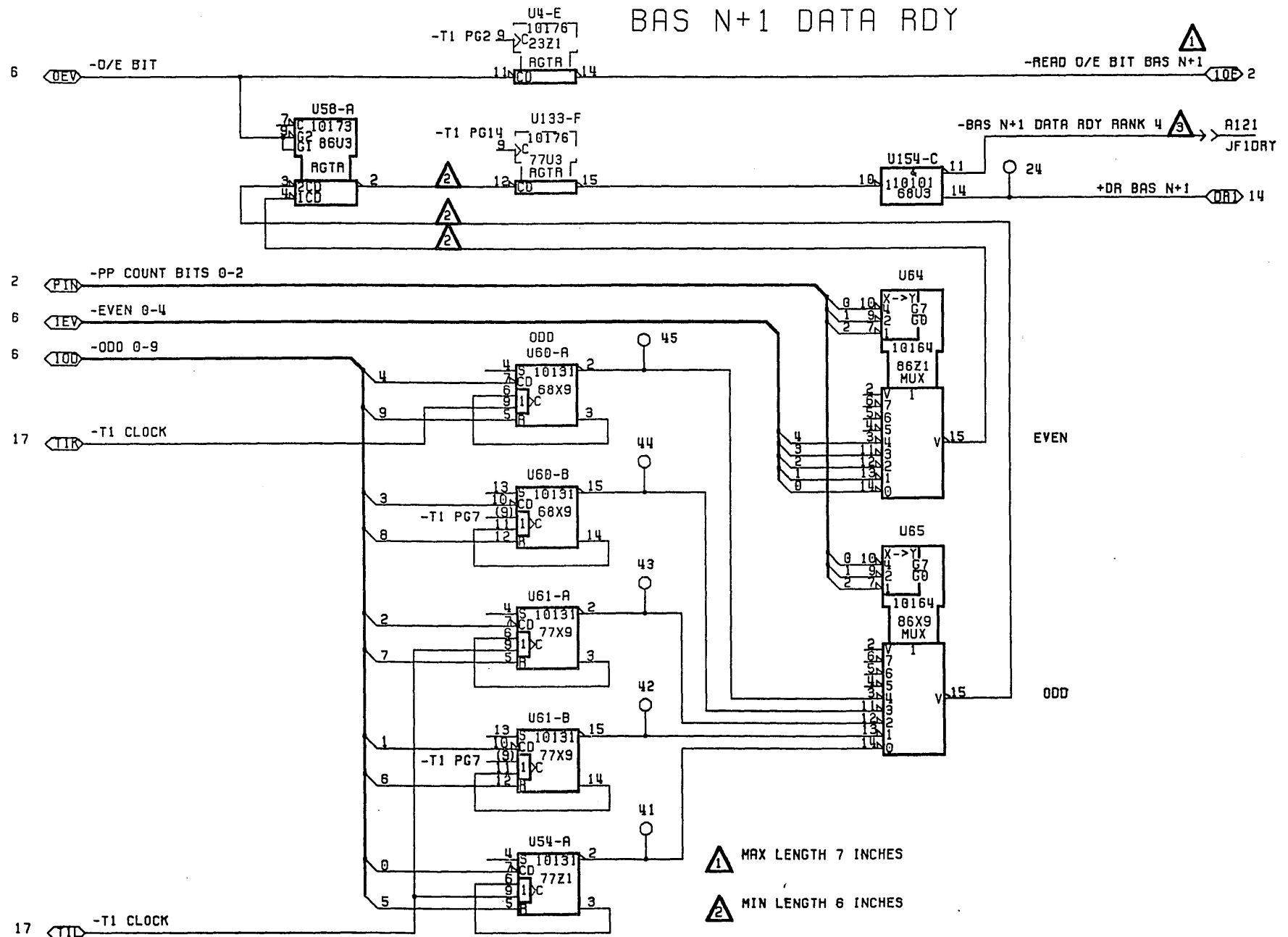
1 NOT TERMINATED AND MAX LENGTH 4 INCHES
 3 MAX LENGTH 12 INCHES

	ADU READ BOARD		DWG NO.	DATE	REV
	DATA READY BAS N+1		22105620	04/04/88	A
TYPE 1JFH	SHEET NO. 8	60462210	PAGE 1F-00		

BAS N DATA RDY



BAS N+1 DATA RDY



MAX LENGTH 7 INCHES

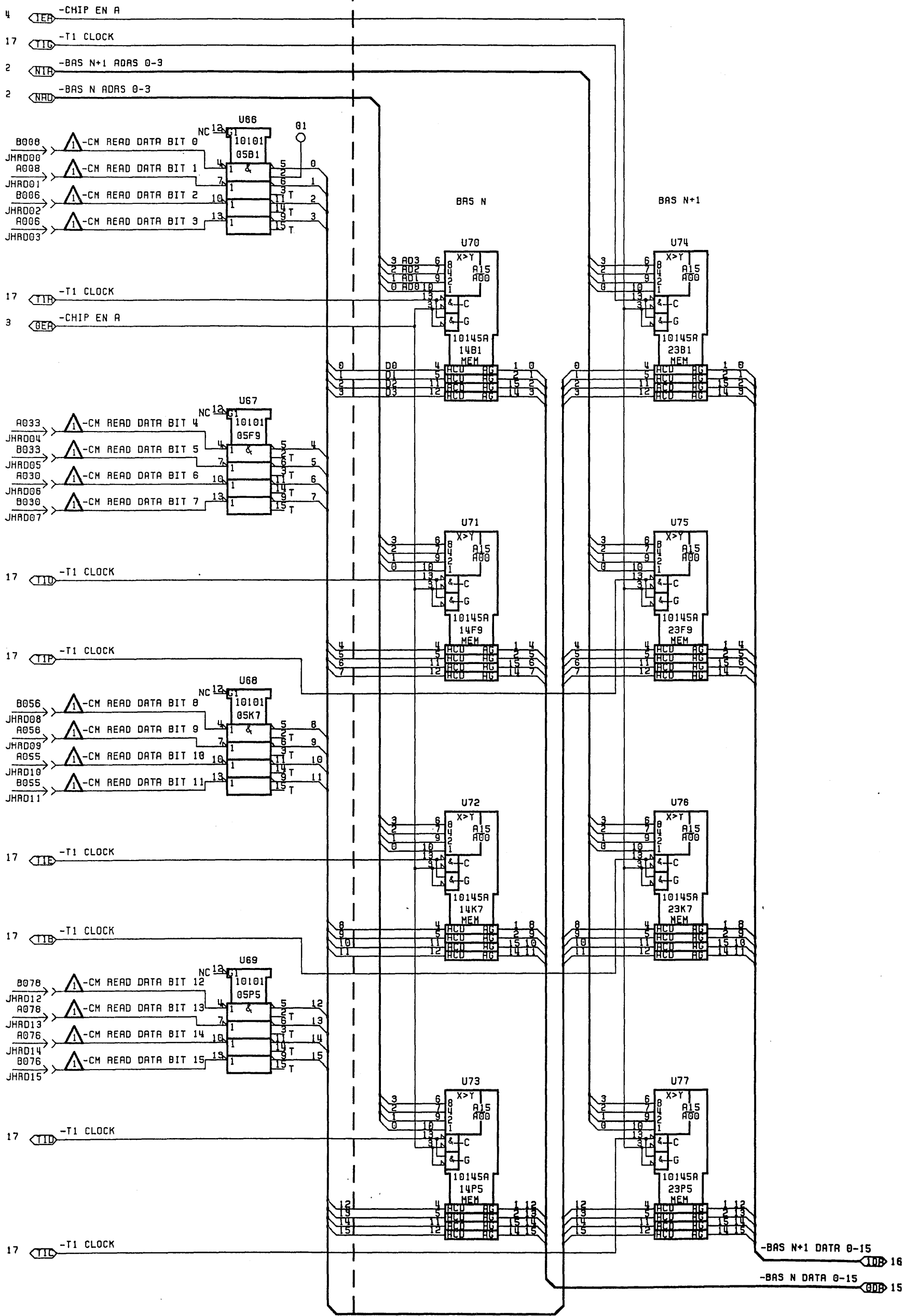
MIN LENGTH 6 INCHES

MAX LENGTH 12 INCHES


<div> <div></div> <div>CONTROL DATA</div> </div>	<div>ADU READ BOARD</div> <div>DATA READY BAS N AND N+1</div> <div>TYPE 1JFH</div>	<div>B</div>	<div>DWG NO.</div> <div>22105620</div>	<div>DATE</div> <div>04/04/86</div>	<div>REV</div> <div>A</div>

DATA-IN BUFFER
BITS 0-15

DISASSEMBLY RGTR BITS 0-15

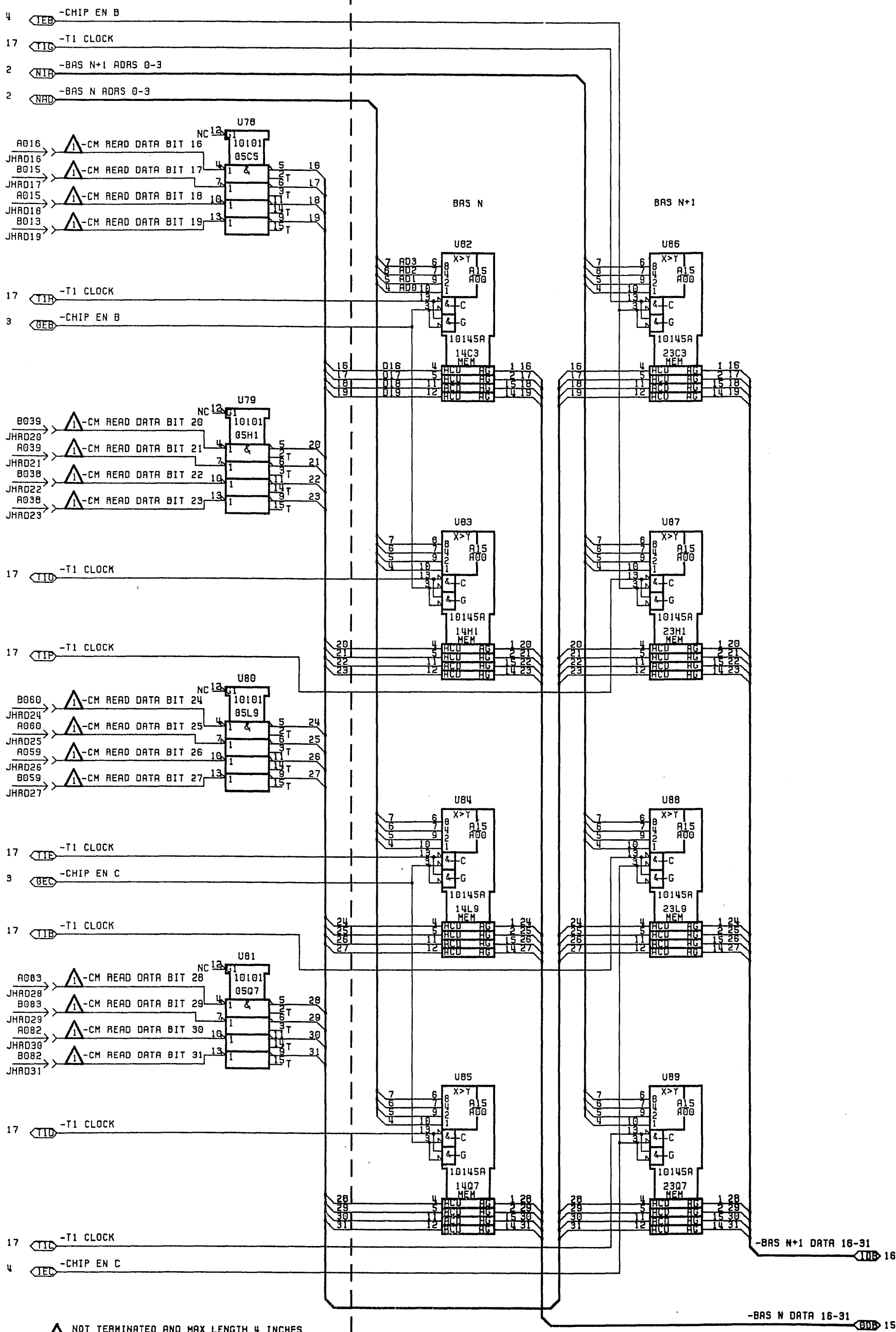


NOT TERMINATED AND MAX LENGTH 4 INCHES


 CONTROL DATA	ADU READ BOARD DATA-IN BUFFER AND DISASSEMBLY REG BITS 0-15 TYPE 1JFH	B	DWG NO.	DATE	REV
			22105620	04/04/86	A
		SHEET NO. 8		60462210	PAGE

DATA-IN BUFFER
BITS 16-31

DISASSEMBLY RGTR BITS 16-31

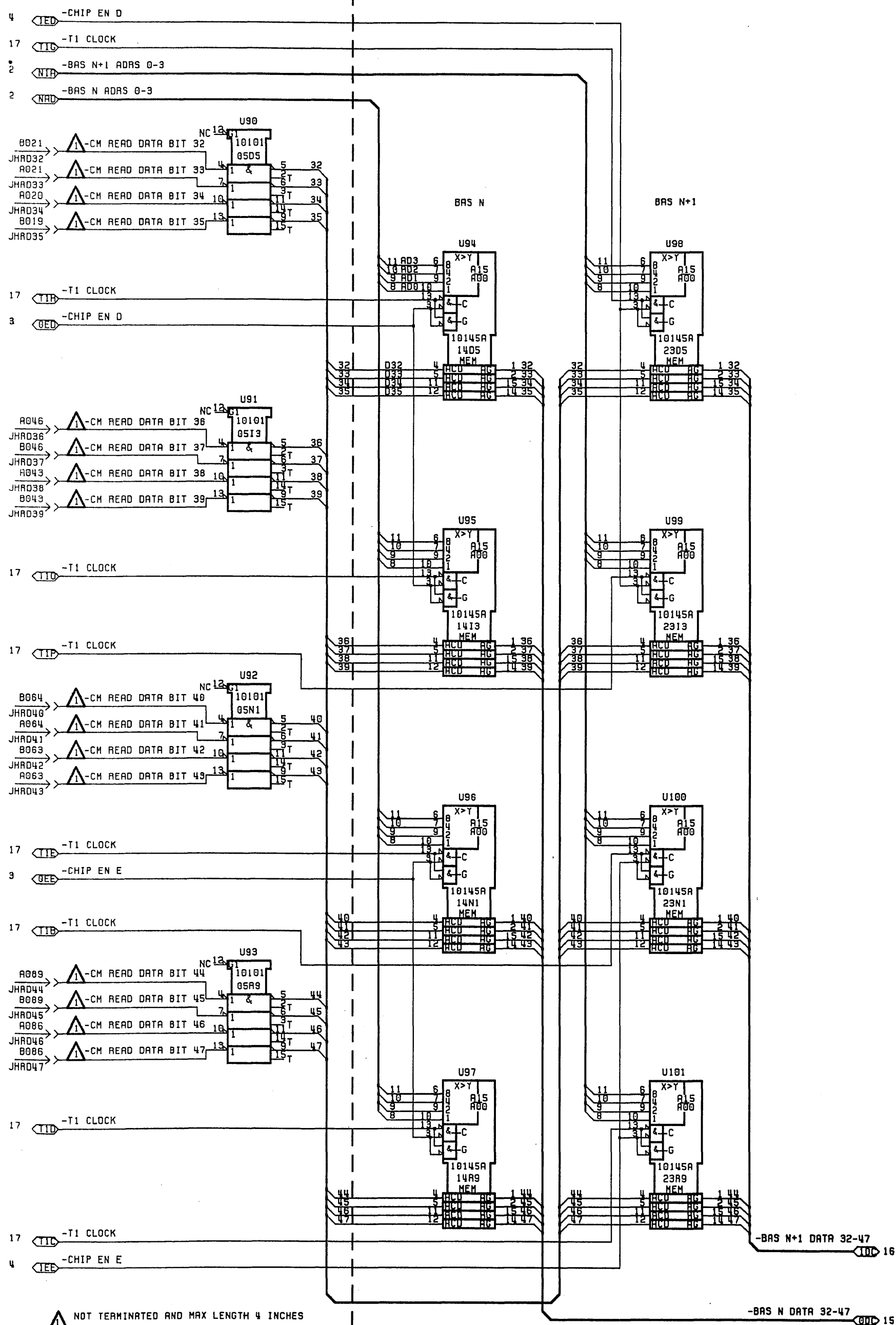


NOT TERMINATED AND MAX LENGTH 4 INCHES

 CONTROL DATA	ADU READ BOARD DATA-IN BUFFER AND DISASSEMBLY REG BITS 16-31 TYPE 1JFH	8	DWG NO. 22105620	DATE 04/04/86	REV A
	N		SHEET NO. 9	60462210	PAGE
			JF-09		

DATA-IN BUFFER BITS 32-47

DISASSEMBLY RGTR BITS 32-47



NOT TERMINATED AND MAX LENGTH 4 INCHES

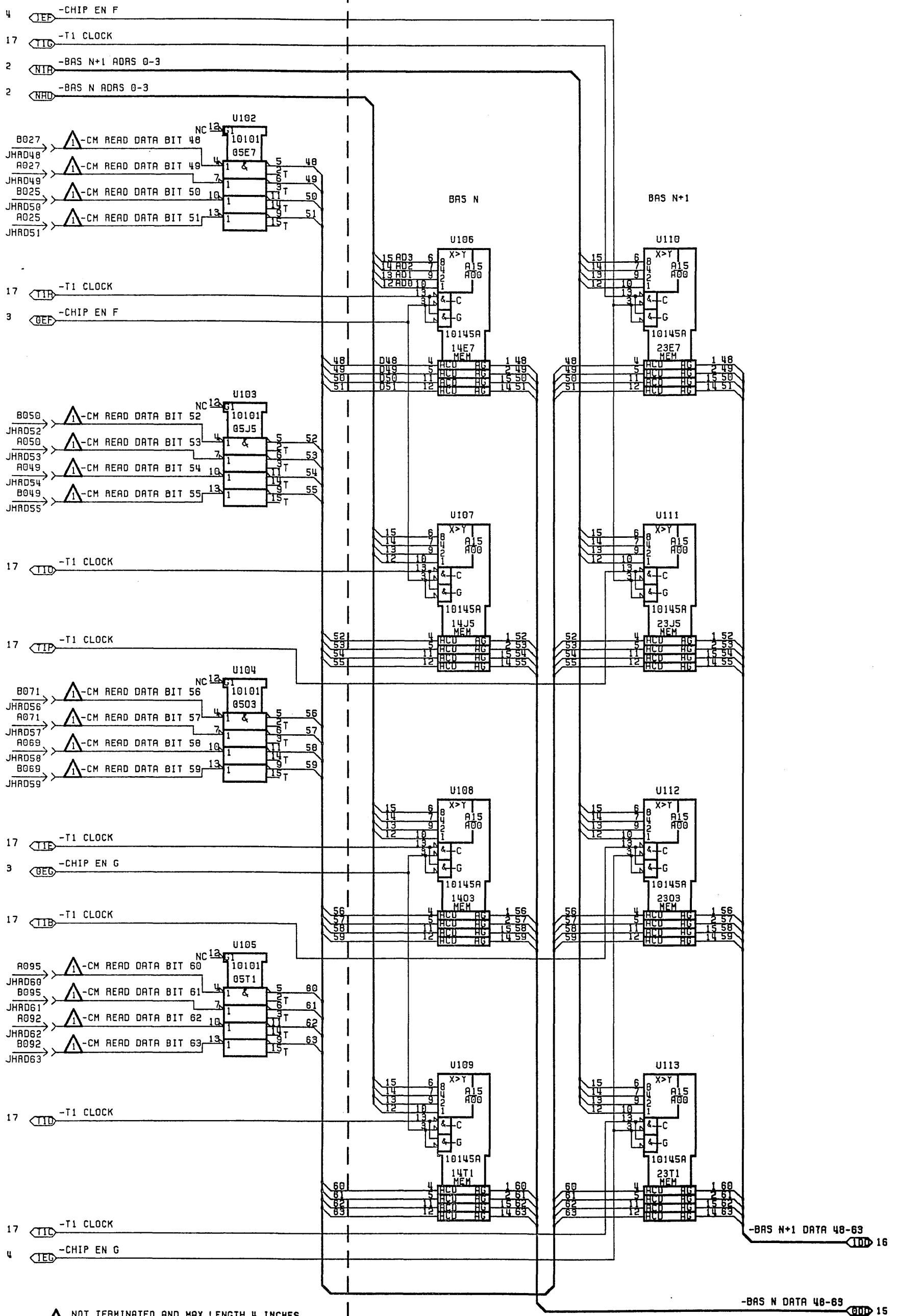


ADU READ BOARD
DATA-IN BUFFER AND
DISASSEMBLY REG BITS 32-47
TYPE 1JFH

DWG NO.	DATE	REV
22105620	04/04/86	A
SHEET NO.	PAGE	
10	50462210	10

DATA-IN BUFFER BITS 48-63

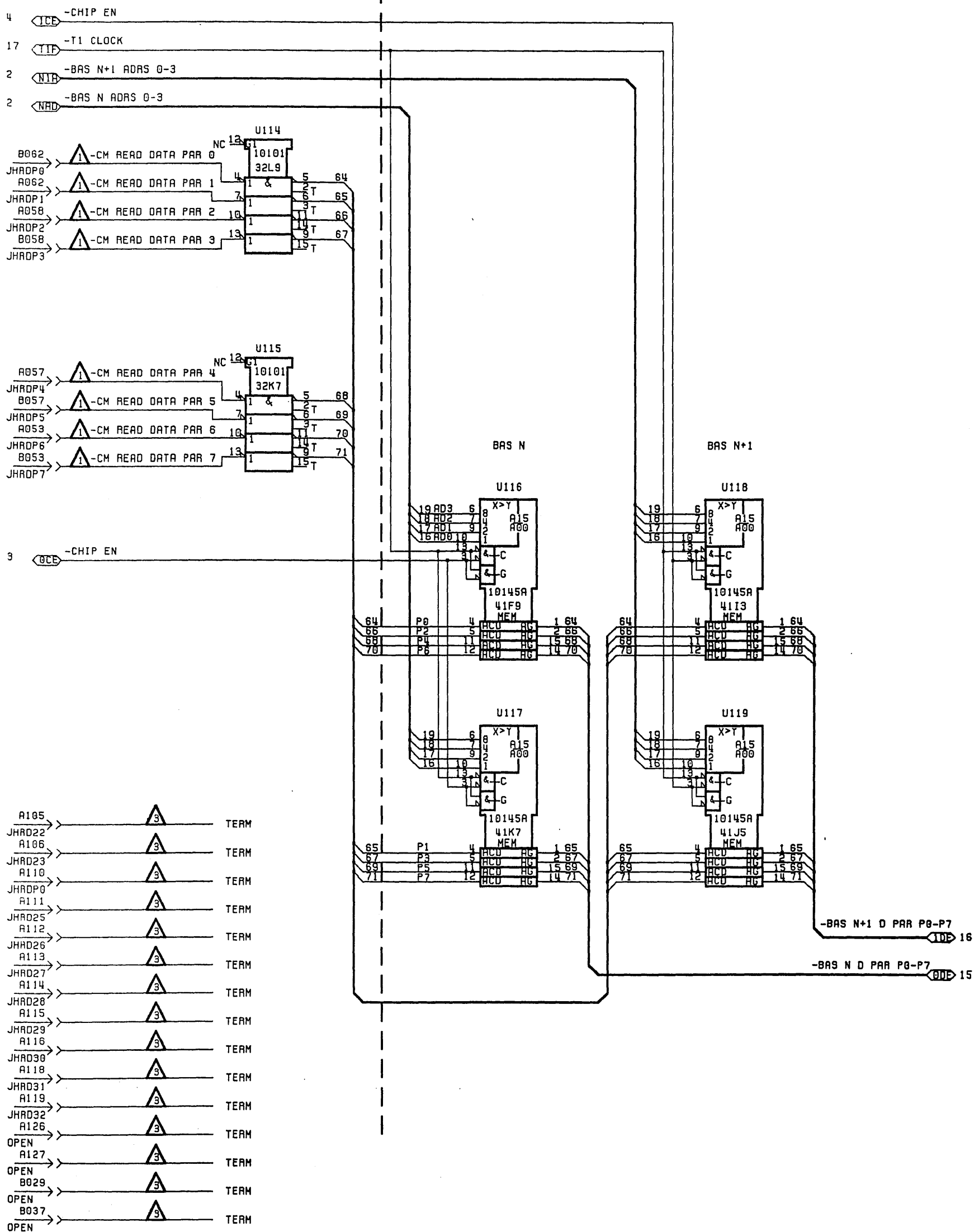
DISASSEMBLY RGTR BITS 48-63




	ADU READ BOARD		DWG NO.	DATE	REV
	DATA-IN BUFFER AND		8	22105620	04/04/86
DISASSEMBLY REG BITS 48-63		SHEET NO.	11	60462210	PAGE
TYPE 1JFH		N		JF-11	

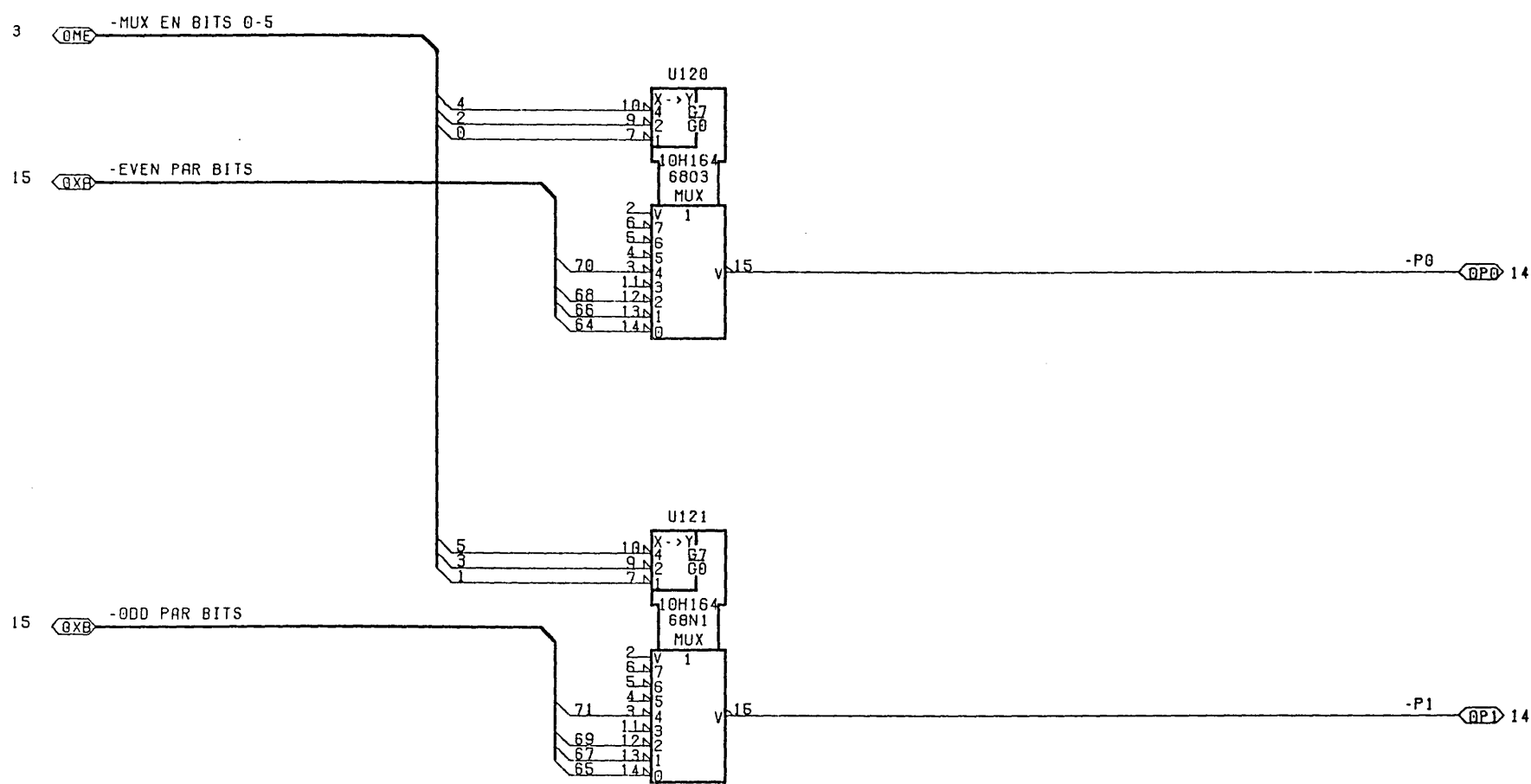
DATA-IN BUFFER PAR BITS 0-7

DISASSEMBLY RGTR PAR BITS 0-7

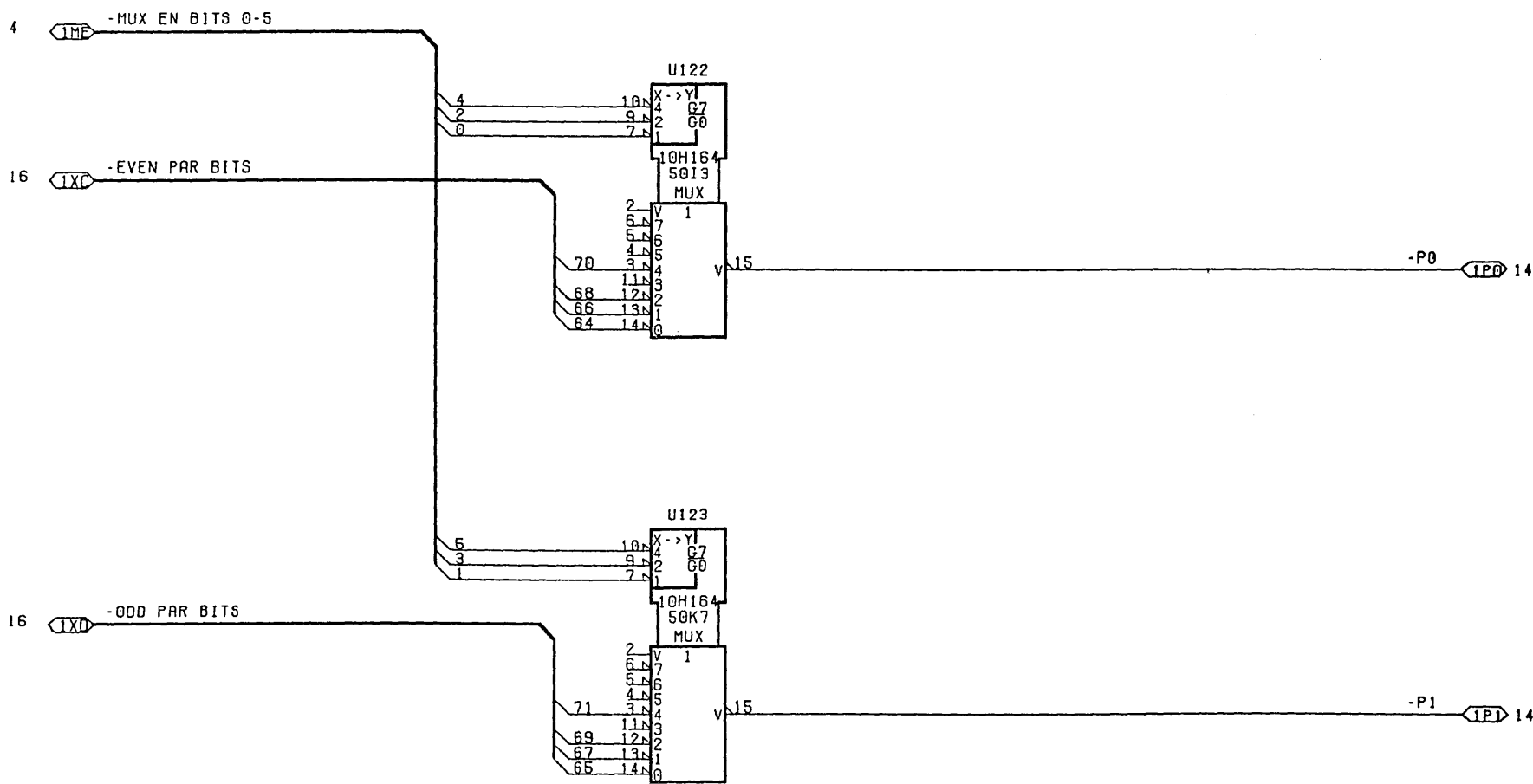



 CONTROL DATA	ADU READ BOARD	8	DWG NO.	DATE	REV
	DATA-IN BUFFER AND		22105620	04/04/86	A
	DISASSEMBLY REG PAR BITS P0-P7				
	TYPE 1JFH		SHEET NO. 12	60462210	PAGE JF-12

BAS N PAR CHECK & GEN

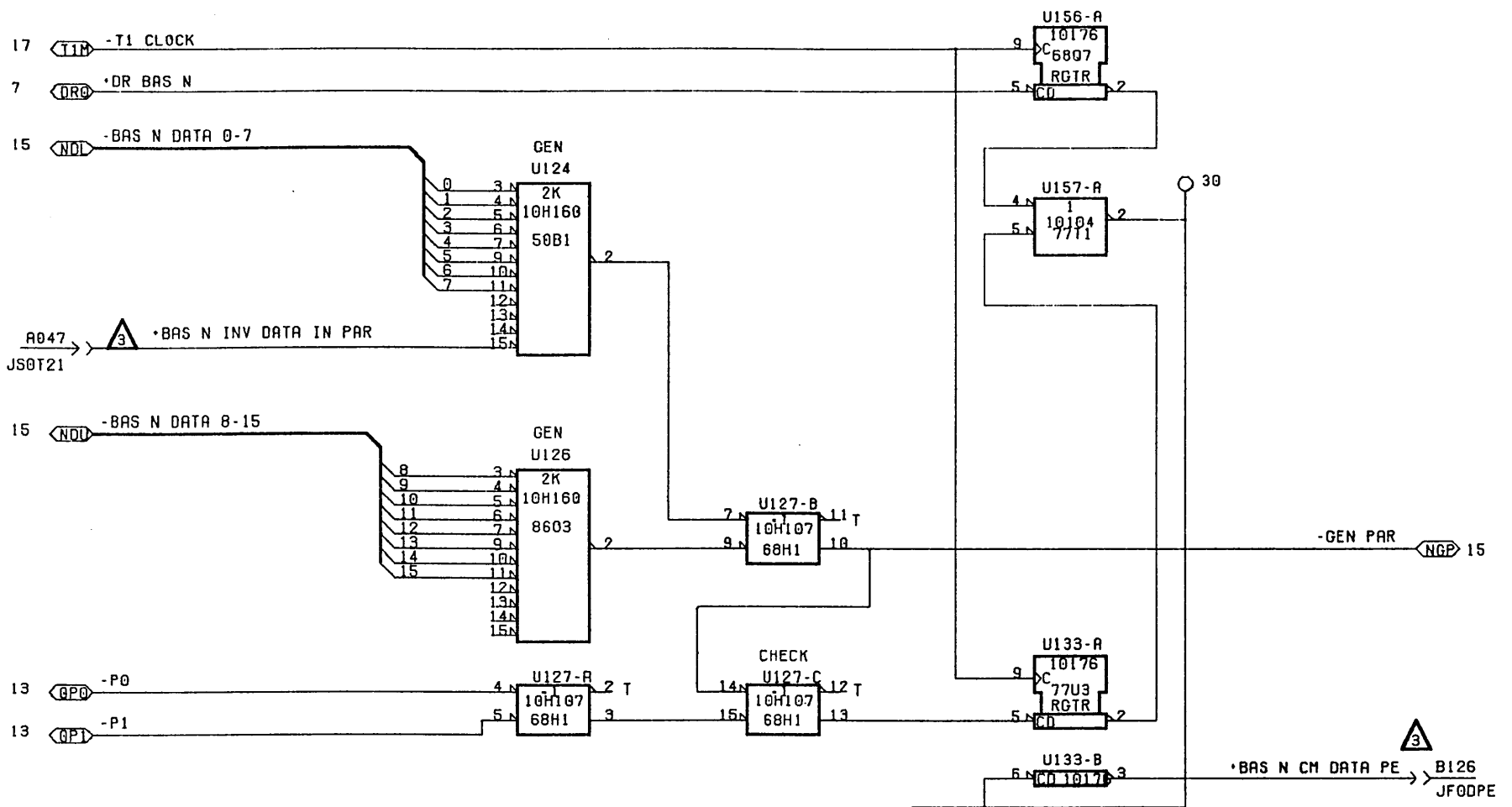


BAS N+1 PAR CHECK & GEN

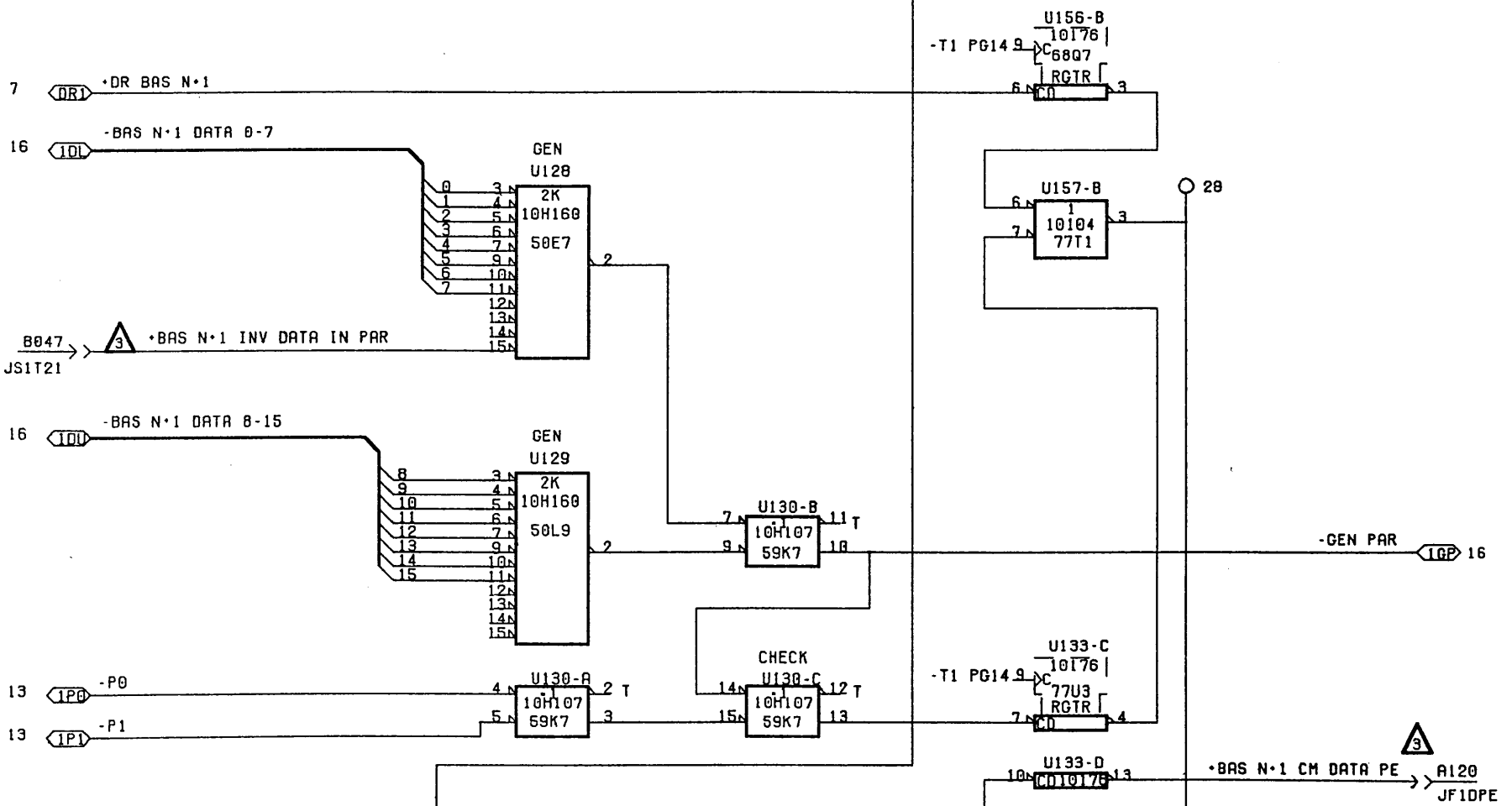


 CONTROL DATA	ADU READ BOARD	B	DWG NO.	DATE	REV
	BAS N AND N+1		22105620	03/30/88	C
	PARITY CHECK & GENERATE				
TYPE 1JFH			SHEET NO. 13	60462210	PAGE 13

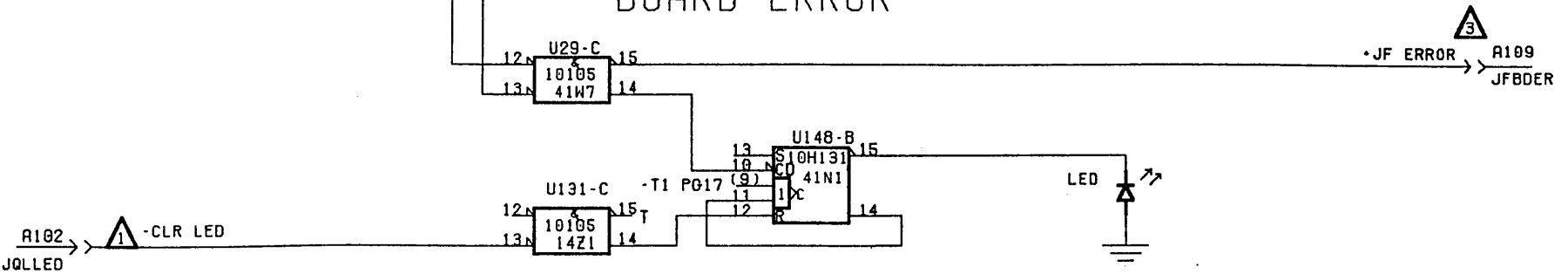
BAS N PAR CHECK & GEN



BAS N+1 PAR CHECK & GEN




BOARD ERROR

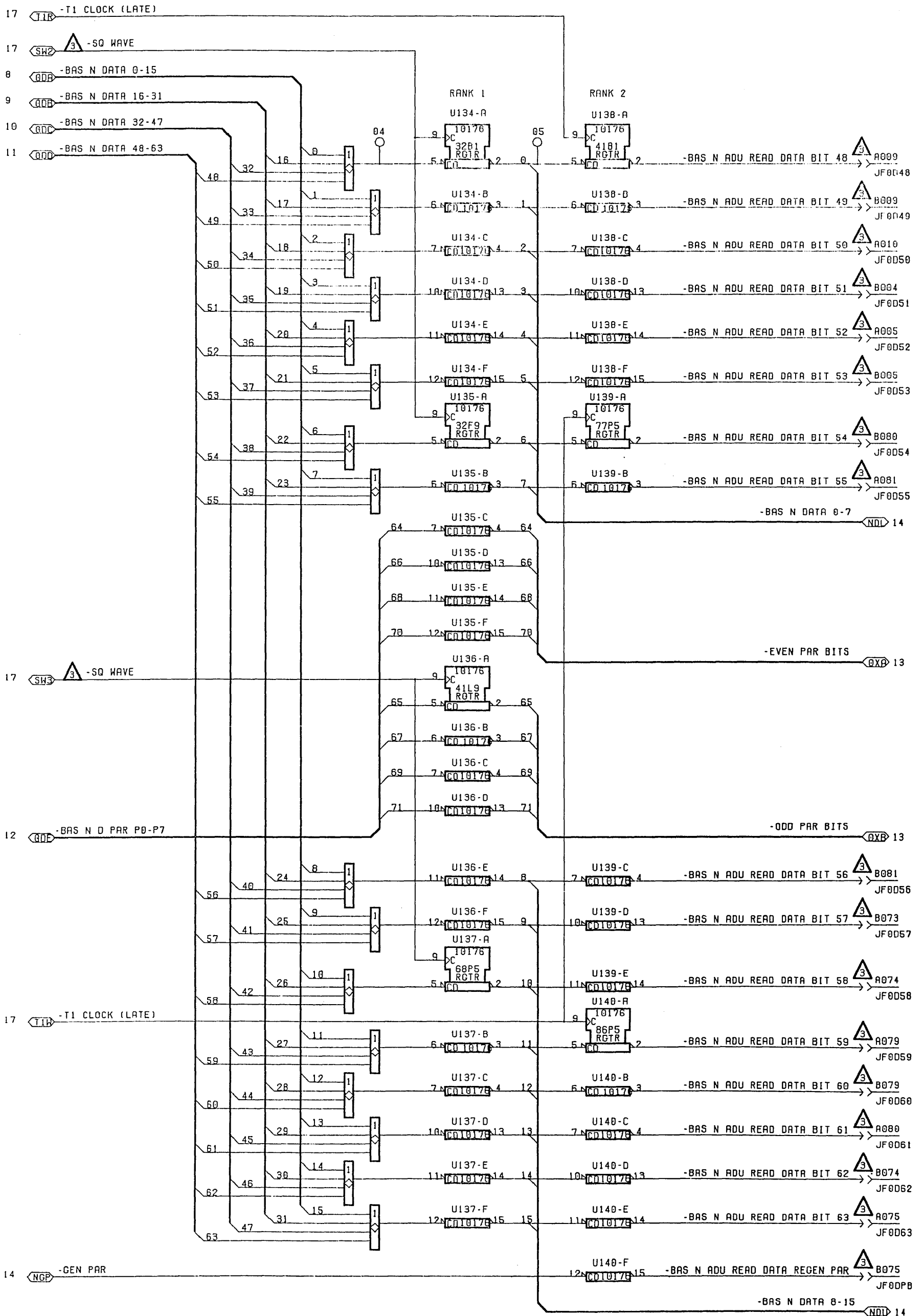


NOT TERMINATED AND MAX LENGTH 4 INCHES

3 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD	8	DWG NO.	DATE	REV
	DATA PAR CHECK AND GENERATE AND BOARD ERROR TYPE 1JFH		22105620	03/30/88	C
			SHEET NO. 14	60462210	PAGE 14

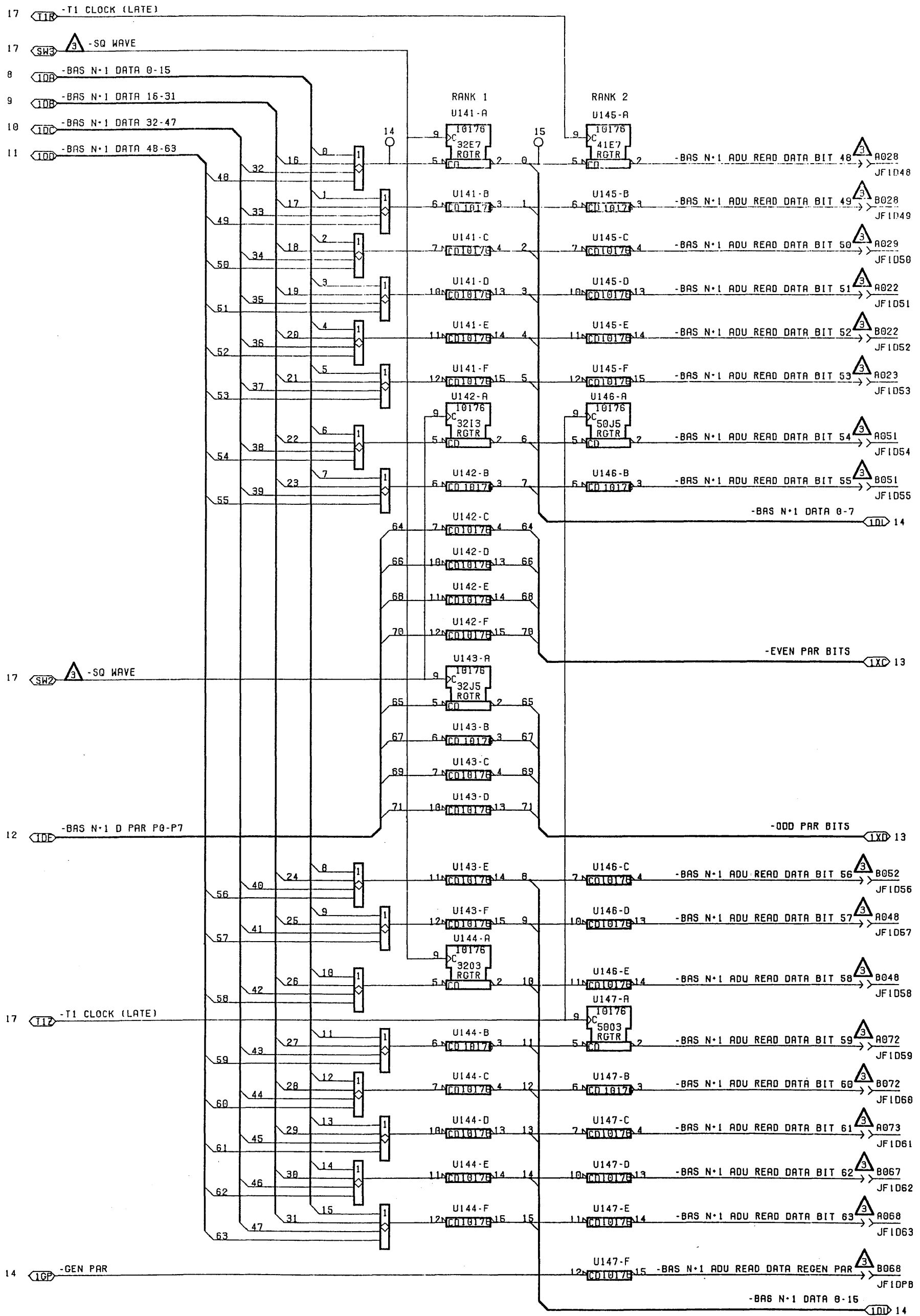
BAS N DATA OUT RGTR




MAX LENGTH 12 INCHES

CD CONTROL DATA	ADU READ BOARD BAS N DATA OUT REGISTER TYPE 1JFH	8	DWG NO. 22105620	DATE 03/30/88	REV C
			SHEET NO. 15	60462210	PAGE JF-15

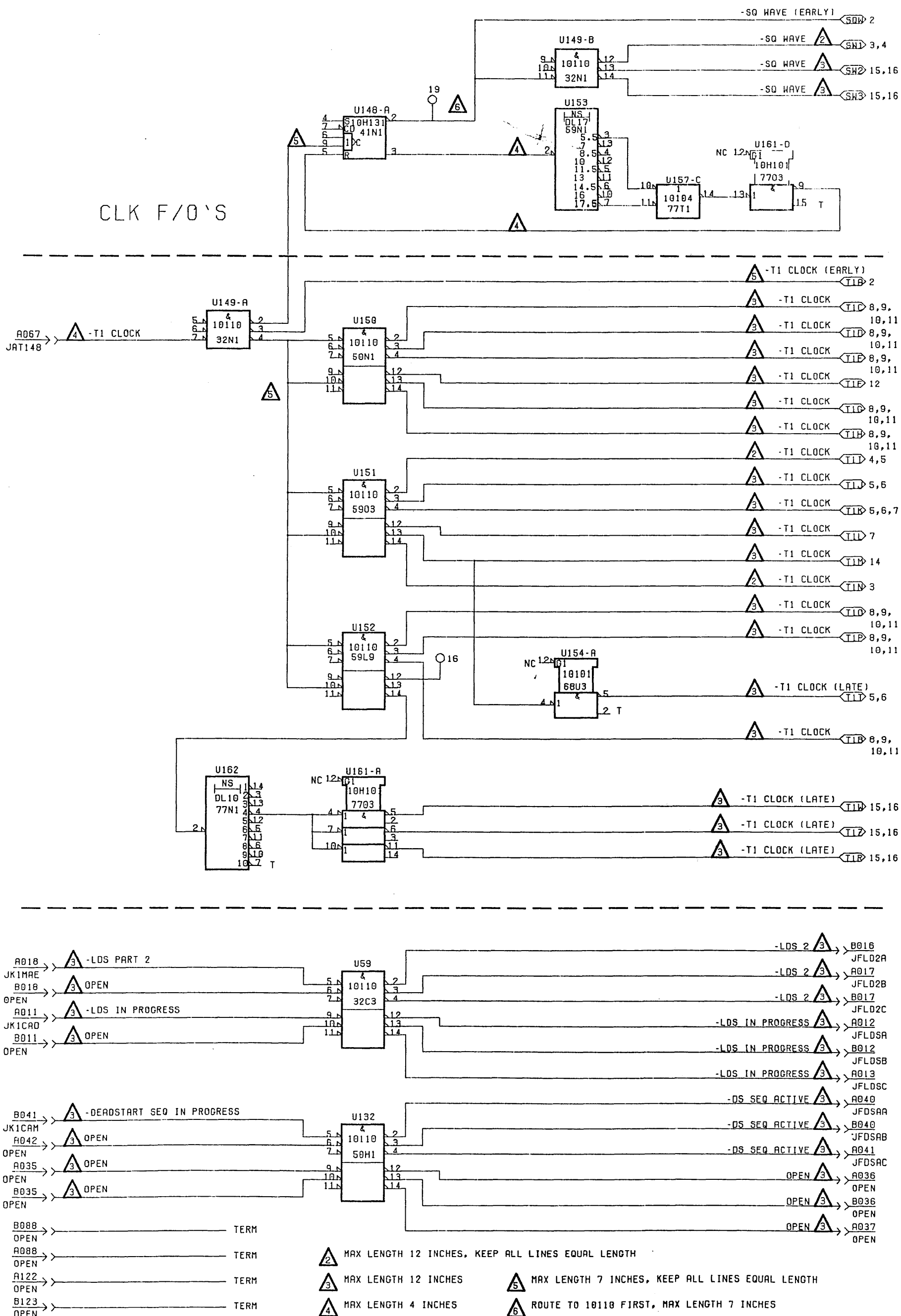
BAS N+1 DATA OUT RGTR




3 MAX LENGTH 12 INCHES

 CONTROL DATA	ADU READ BOARD		8	DWG NO.	DATE	REV
	BAS N+1			22105620	03/30/88	C
	DATA OUT REGISTER					
TYPE 1JFH		N	SHEET NO. 16		60462210	PAGE
					JF-16	


SQ WAVE GEN



 CONTROL DATA	ADU READ BOARD CLOCK FANOUT AND SQ WAVE GENERATOR & F/O TYPE 1JFH	B	DWG NO.	DATE	REV
			22105620	03/30/88	C
			SHEET NO. 17		60462210

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	08	+DATA BIT 0 IN	27	07	+BAS N DATA RDY
02	03	-BAS N CHIP EN A	28	14	+BAS N+1 DATA PE
03	04	-BAS N+1 CHIP EN A	29	06	-BAS N+1 ODD/EVEN
04	15	-BAS N DATA BIT 48	30	14	+BAS N DATA PE
05	15	-BAS N DATA 48 OUT	31	07	-N P0 0 DATA RDY
06	03	-BAS N CHIP EN B	32	07	-N P1 0 DATA RDY
07	04	-BAS N+1 CHIP EN B	33	07	-N P2 0 DATA RDY
08	03	-BAS N CHIP EN D	34	07	-N P3 0 DATA RDY
09	04	-BAS N+1 CHIP EN D	35	07	-N P4 0 DATA RDY
10			36	05	-N P0 E DATA RDY
11			37	05	-N P1 E DATA RDY
12	03	-BAS N CHIP EN F	38	05	-N P2 E DATA RDY
13	04	-BAS N+1 CHIP EN F	39	05	-N P3 E DATA RDY
14	16	-BAS N+1 DATA 48	40	05	-N P4 E DATA RDY
15	16	-BAS N+1 DATA 48 OUT	41	07	-N+1 P0 0 DATA RDY
16	17	-T1 CLOCK	42	07	-N+1 P1 0 DATA RDY
17	04	-BAS N+1 CHIP EN C	43	07	-N+1 P2 0 DATA RDY
18	03	-BAS N CHIP EN C	44	07	-N+1 P3 0 DATA RDY
19	17	-SQUARE WAVE	45	07	-N+1 P4 0 DATA RDY
20	04	-BAS N+1 CHIP EN E	46	06	-N+1 P0 E DATA RDY
21	03	-BAS N CHIP EN E	47	06	-N+1 P1 E DATA RDY
22	03	-BAS N CHIP EN G	48	06	-N+1 P2 E DATA RDY
23	04	-BAS N+1 CHIP EN G	49	06	-N+1 P3 E DATA RDY
24	07	+BAS N+1 DATA RDY	50	06	-N+1 P4 E DATA RDY
25	03	+BAS N FIRST REQ	51	04	+BAS N+1 FIRST REQ
26	05	-BAS N ODD/EVEN			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 [NOT USED]
TERM	A003, B003, A004, B020, B023, A026, B026, B029, A031, B031, A032, B032, B037, B042, A045, B045, A052, A084, B084, A085, A088, B088, A093, B093, A094, B094, A099, B099, A100, A104, A105, A106, A110, A111, A112, A113, A114, A115, A116, A118, A119, A122, B123, A126, A127
UNUSED	B105, B106, B110, B111, B112, B114, B115, B116, B118, A123, B127, A128, B128

 CONTROL DATA	ADU READ BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JFH	B	DWG NO. 22105620	DATE 04/04/86	REV A
		SHEET NO. 18	60462210	PAGE	JF-10

CAUTION

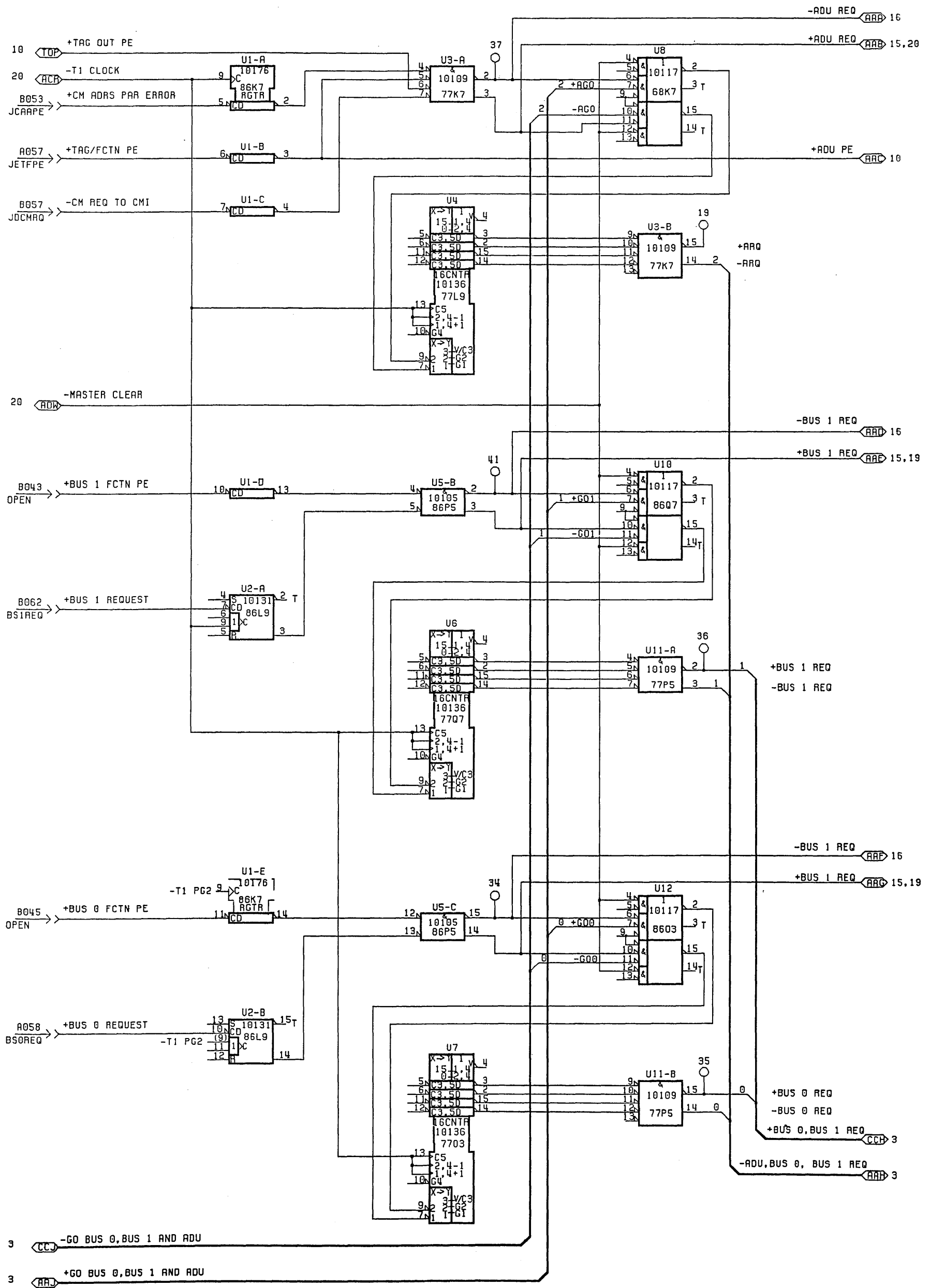
There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

CMI CONTROL BOARD

[illegible]

DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	J P STROMBECK	12/04/85
PUBS	R K BONDE	12/04/85
APP	J P STROMBECK	12/04/85

REQ CONTROL



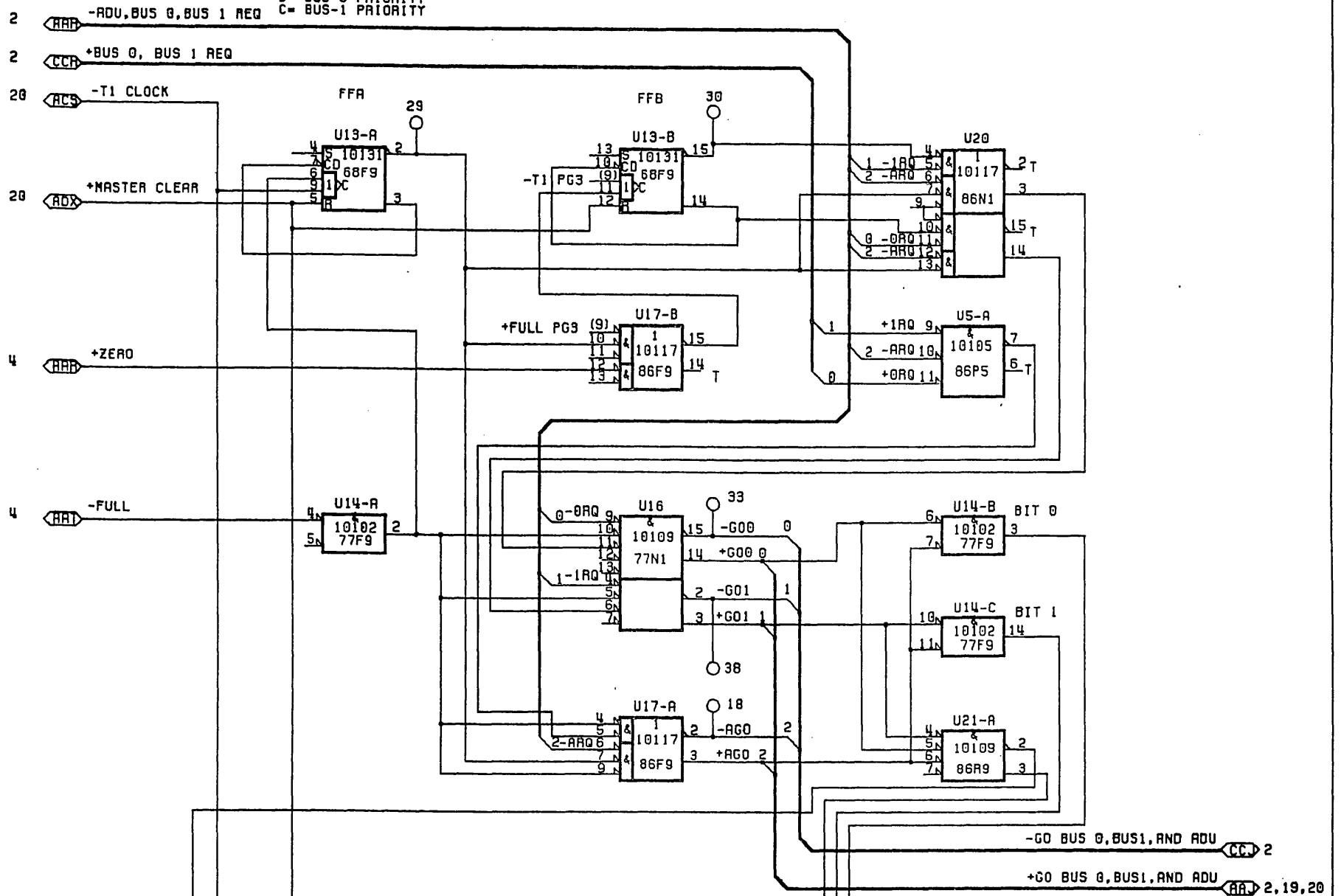
 CONTROL DATA	CHI CONTROL BOARD REQUEST CONTROL		B	DWG NO. 53575506	DATE 11/01/85	REV A
	TYPE 1JGH		SHEET NO. 2	60462210	PAGE	JG-02

FFA= C A B A C A B

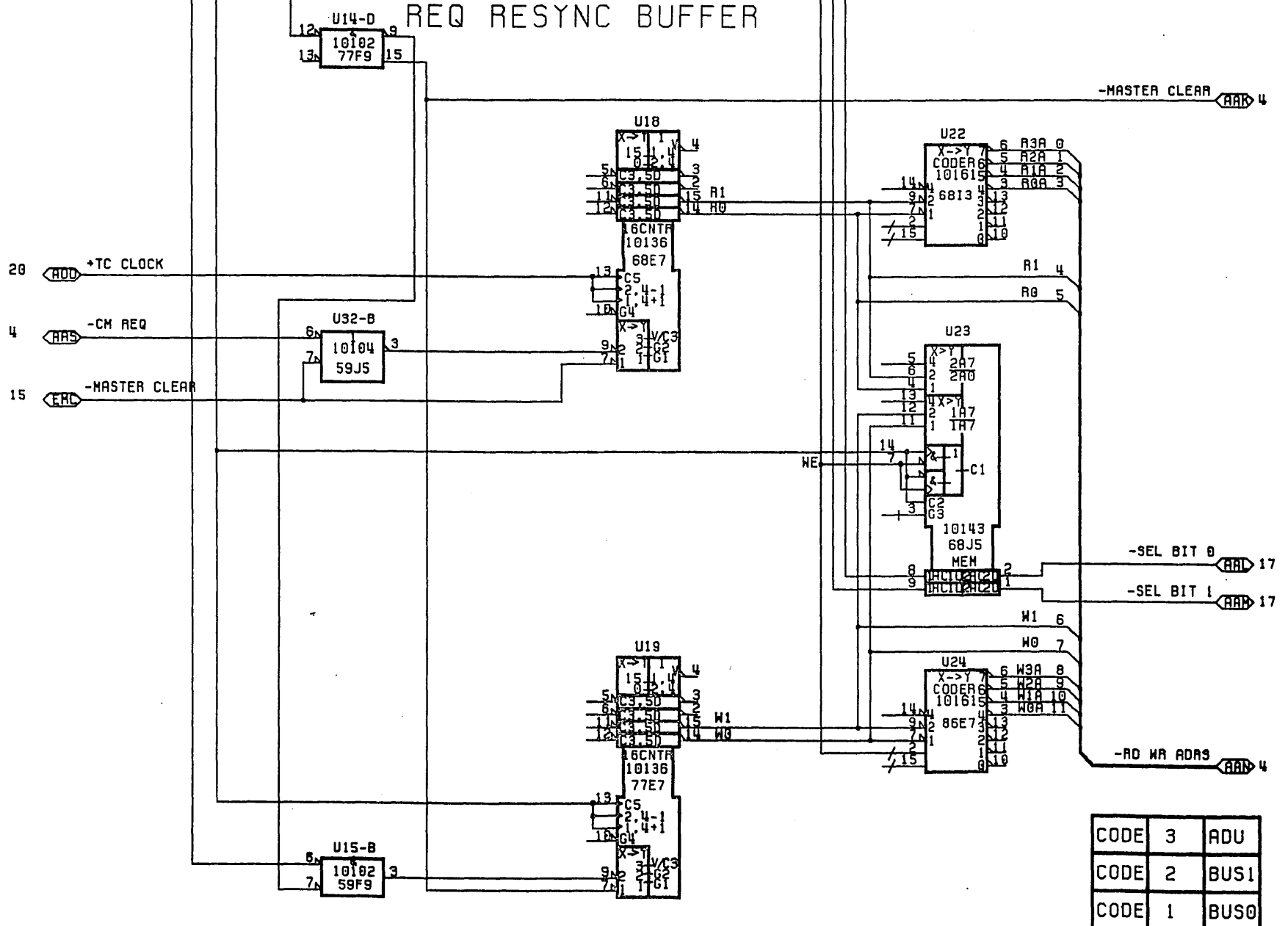
PRIORITY CONTROL

FFB=

A= ADU PRIORITY
B= BUS-0 PRIORITY
C= BUS-1 PRIORITY



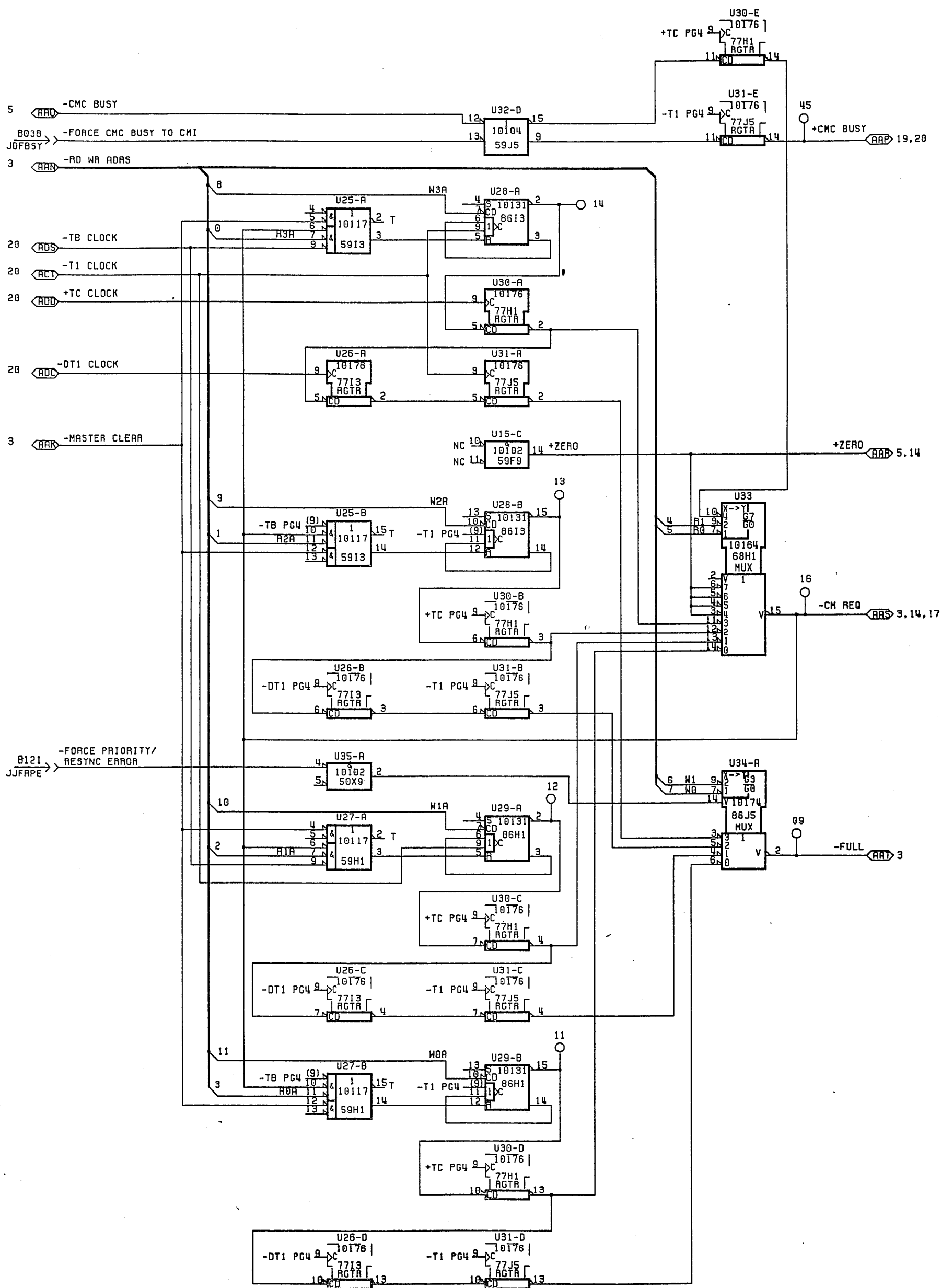
REQ RESYNC BUFFER



CODE	3	ADU
CODE	2	BUS1
CODE	1	BUS0

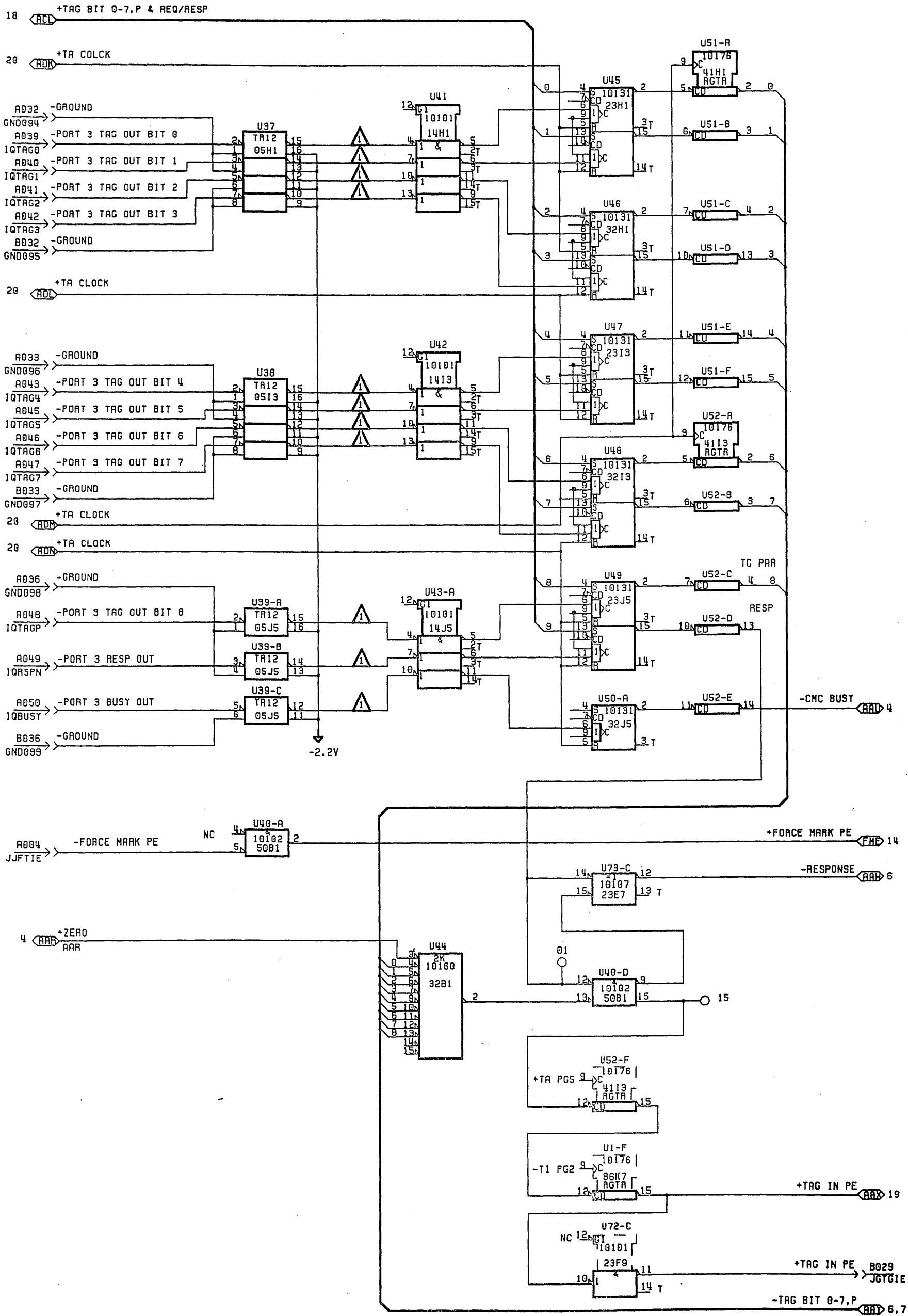
 <p>CONTROL DATA</p>	<p>CHI CONTROL BOARD PRIORITY CONTROL AND REQUEST RESYN BUFFER TYPE 1JGH</p>		<p>B</p>	<p>DWG NO. 53575506</p>	<p>DATE 01/30/88</p>	<p>REV B</p>
	<p>SHEET NO. 3</p>		<p>60462210</p>		<p>PAGE 16-83</p>	
	<p>4-179</p>					

REQ RESYNC RGTR



CONTROL DATA	CMI CONTROL BOARD REQUEST RESYNCH F/P'S		DWG NO.	DATE	REV
	TYPE 1JGH		B 53575586	11/01/85	A
	SHEET NO. 4		60462210	PAGE	JG-04

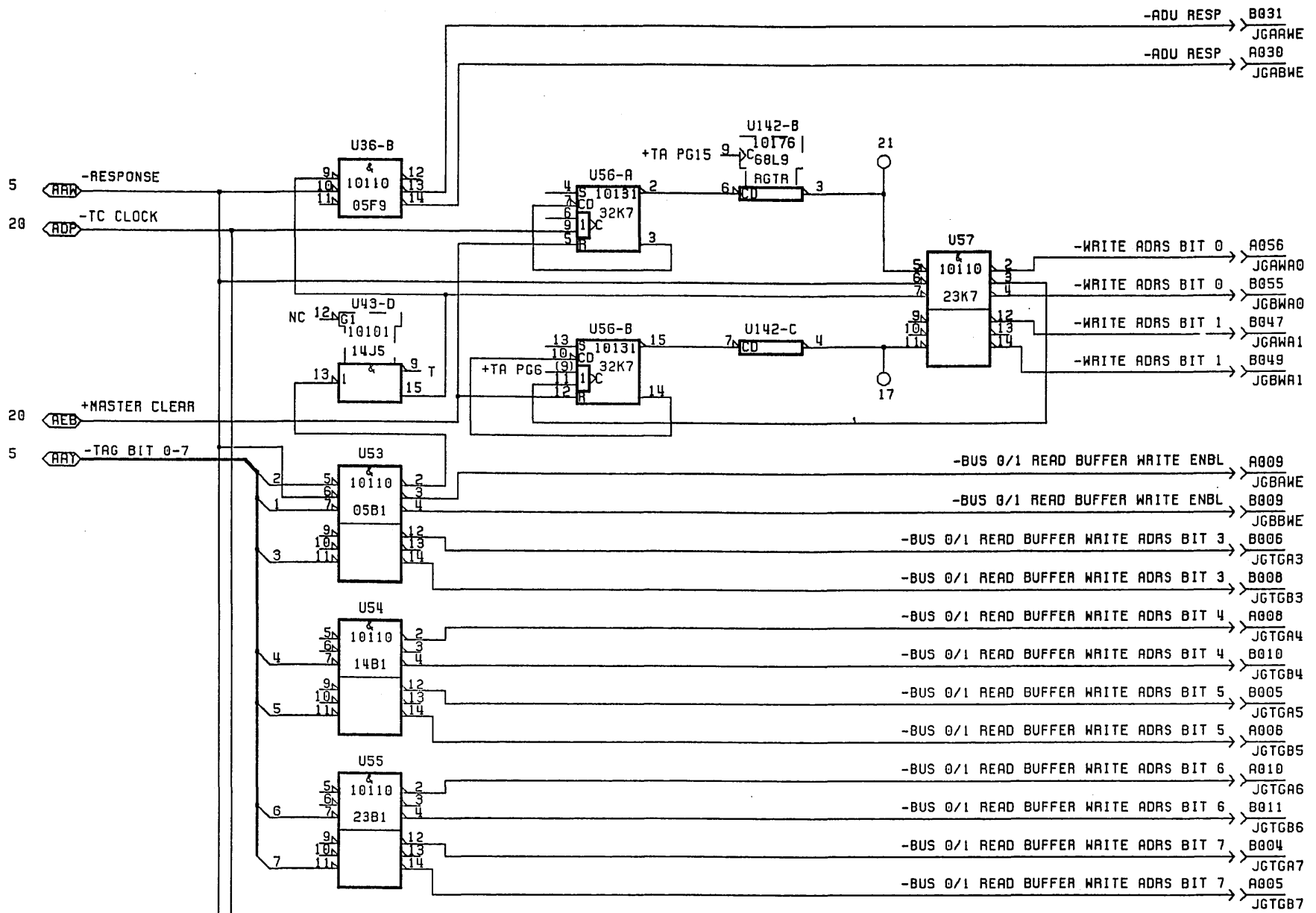
TAG BITS IN RGTR



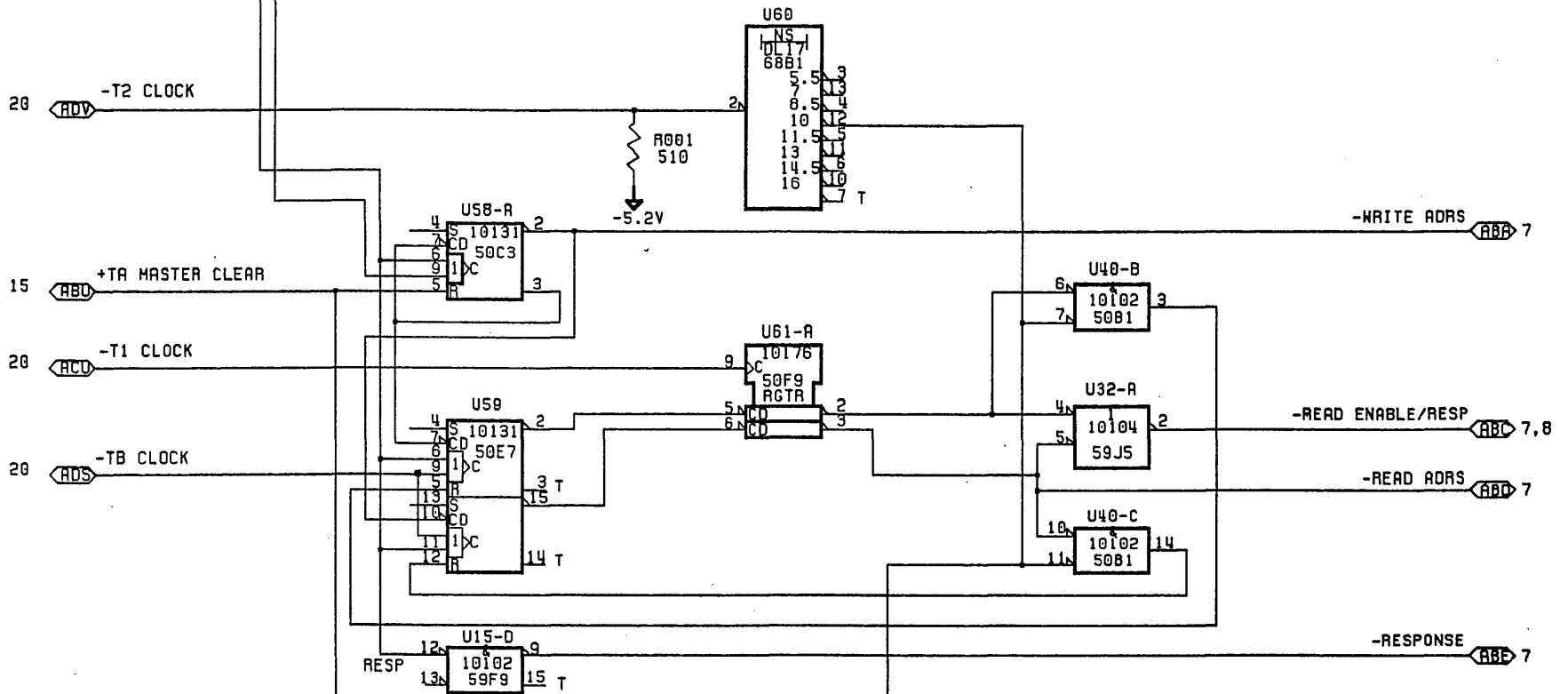
NOT TERMINATED

	CMI CONTROL BOARD TAG BITS IN		B	DWG NO. 53575506	DATE 11/01/85	REV A
	TYPE 1JGH		SHEET NO. 5	60462210	PAGE	JG-05

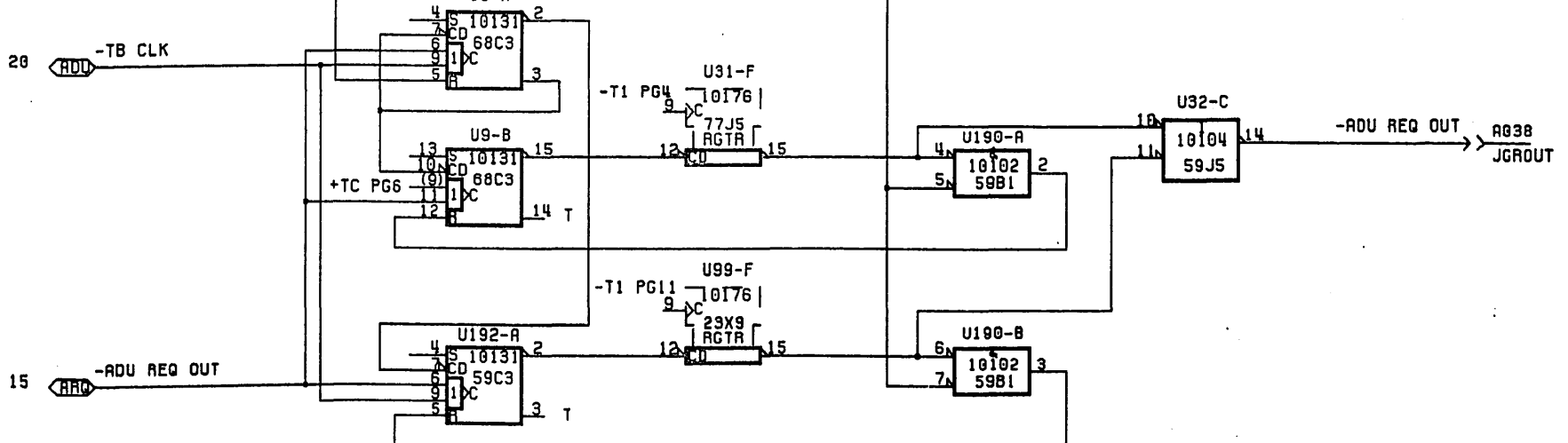
TAG BITS IN F/O



RESP RESYNC



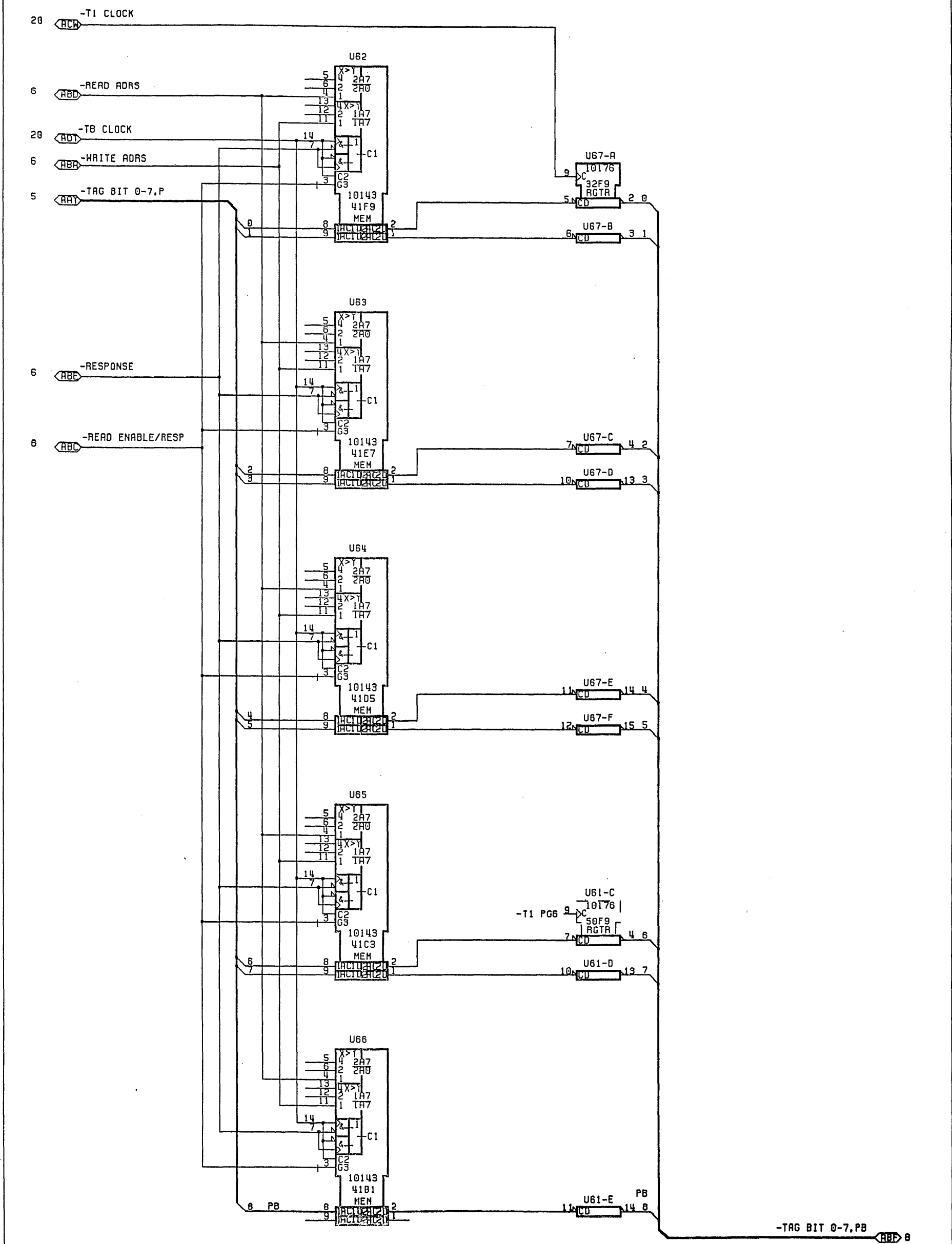
ADU REQ OUT RESYNC



CHI CONTROL BOARD
TAG BITS IN, RESPONSE RESYNCH
AND ADU REQ OUT RESYNCH
TYPE 1JGH

DWG NO.	DATE	REV
8	53575508	11/01/85
SHEET NO. 6	60462210	PAGE
		JG-06

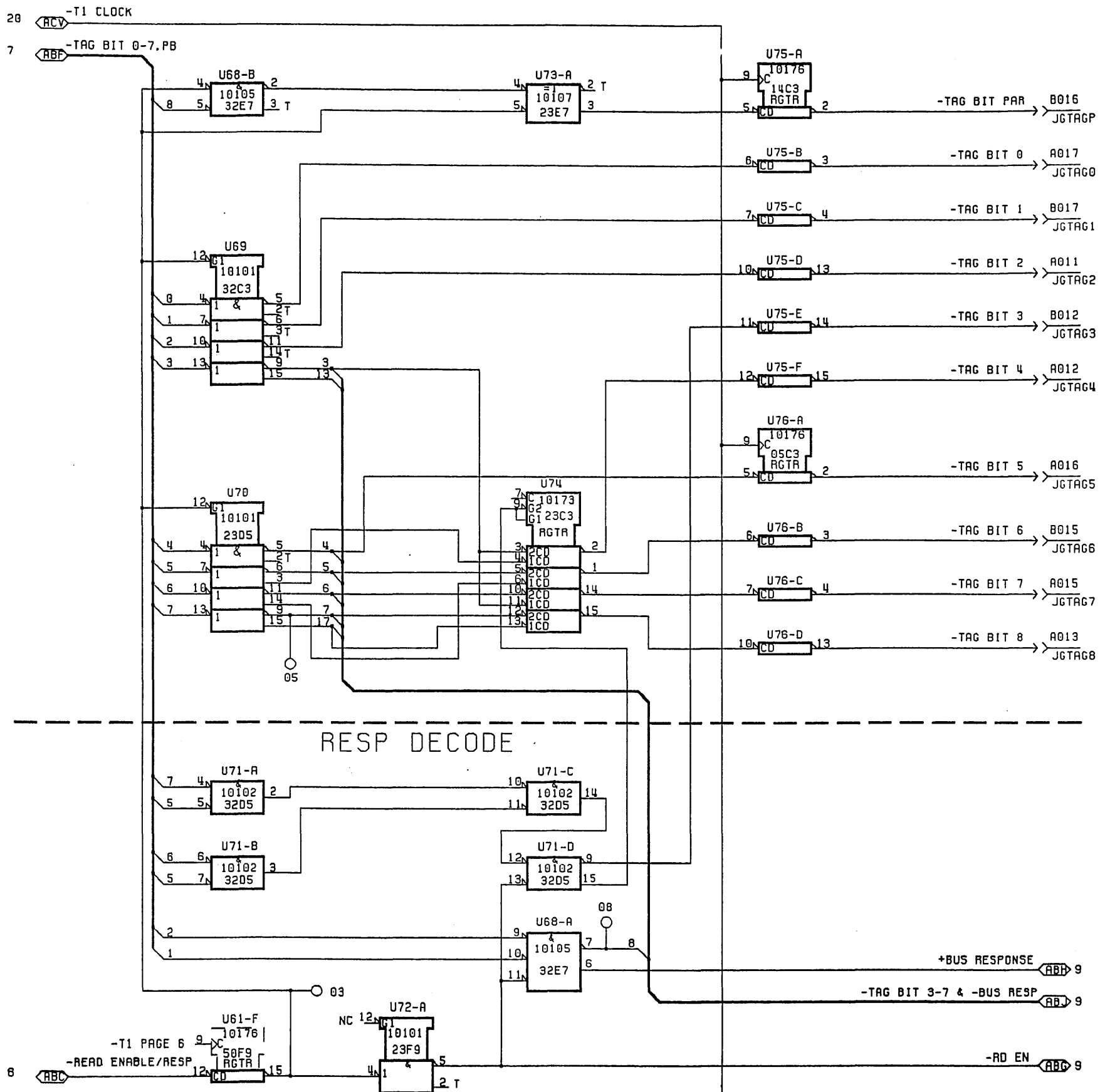
TAG BITS IN BUFFER



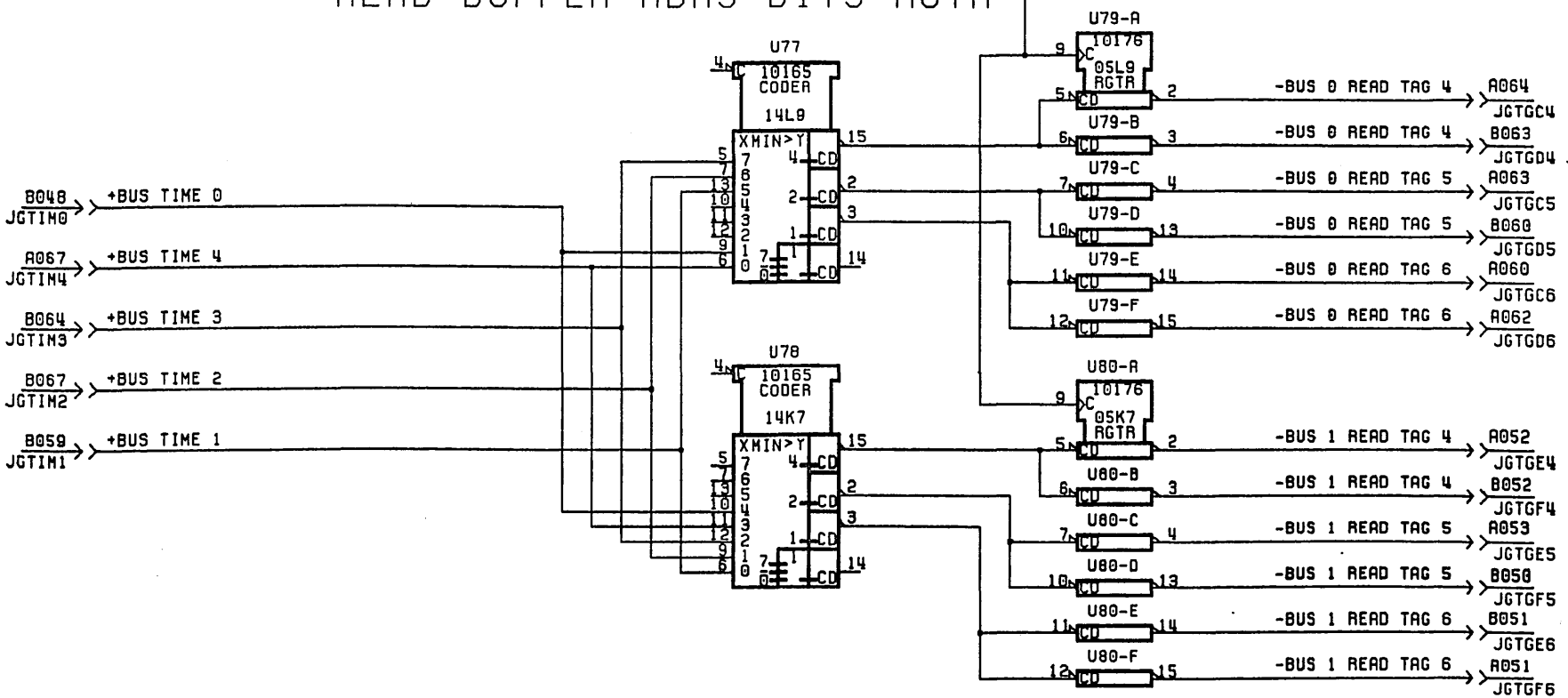
CHI CONTROL BOARD
TAG BITS IN BUFFER
TYPE 1JGH


DWG NO.	DATE	REV
B	11/01/85	A
SHEET NO.	PAGE	
7	60462210	J6-07

TAG IN 8-9 BIT CONVERSION

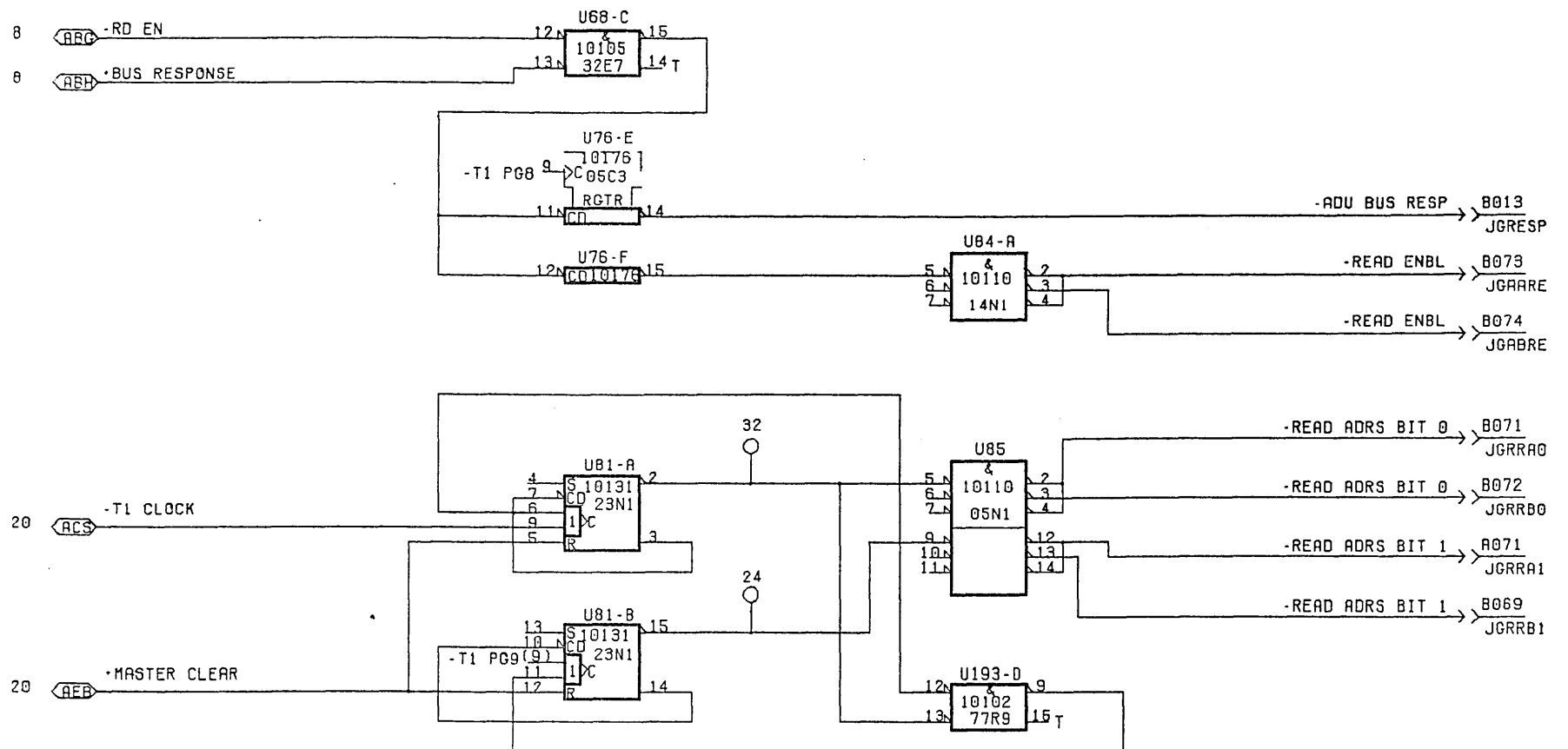


READ BUFFER ADRS BITS RGTR

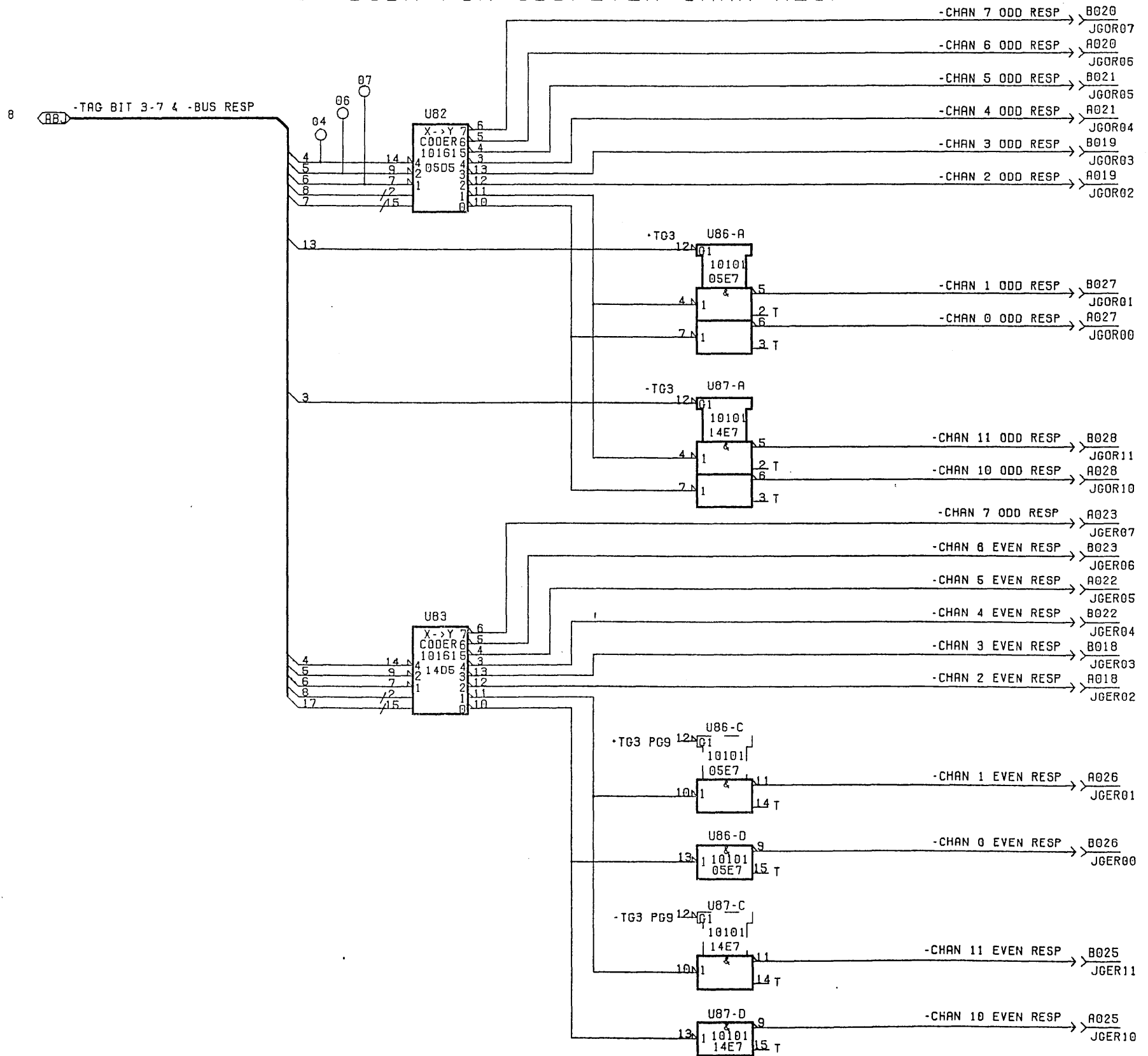



 CONTROL DATA	CMI CONTROL BOARD	B	DWG NO.	DATE	REV
	TAG BIT IN 8-9 BIT CONVERSION, RD BUFFER ADRS BITS & RESP DECODE		53575506	11/01/85	A
	TYPE 1JGH				
SHEET NO. 8		60462210		PAGE 16-08	

ADU READ ADRS CNTR

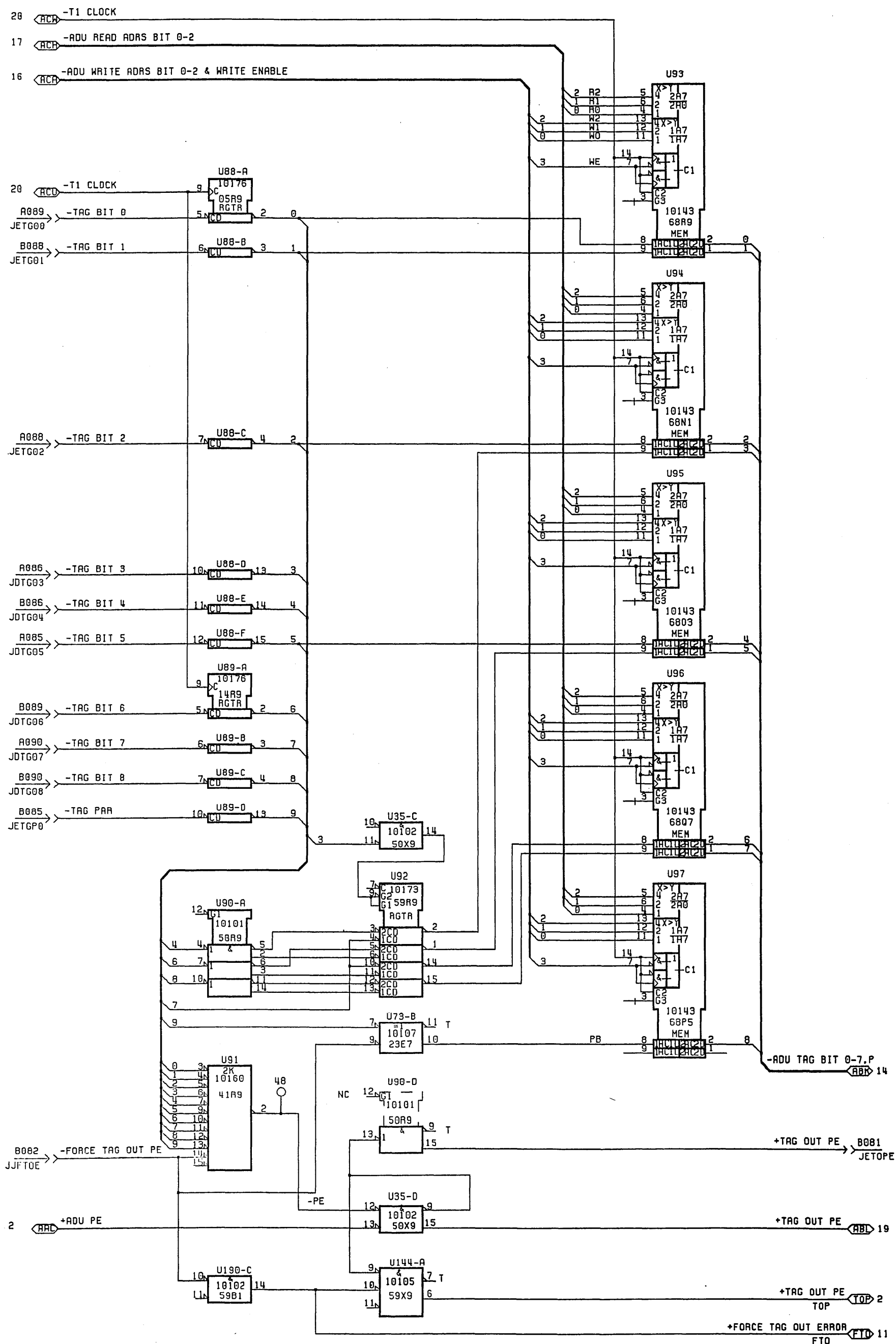



TAG BIT DCDR FOR ODD/EVEN CHAN RESP



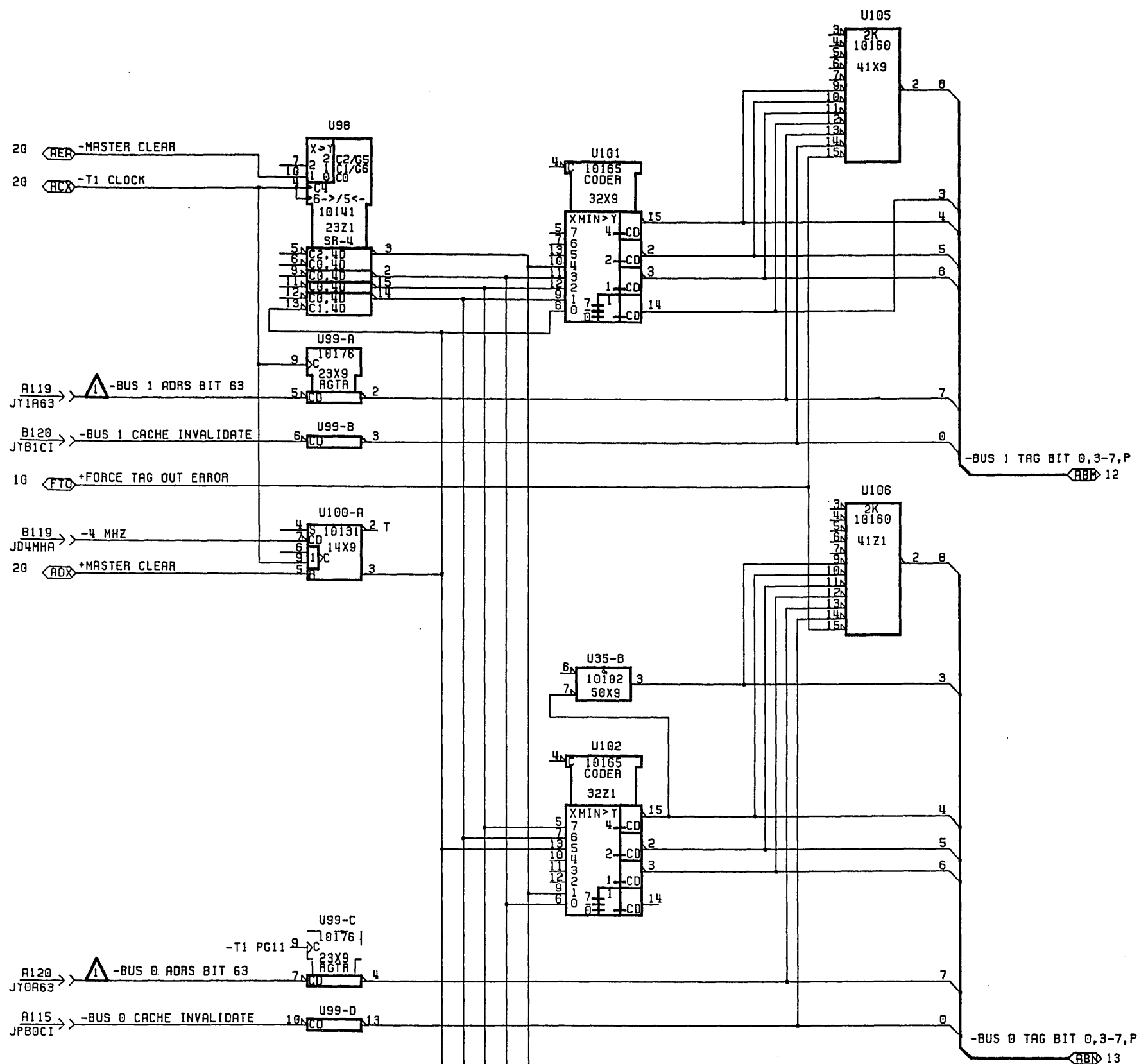
 CONTROL DATA	CHI CONTROL BOARD ADD READ ADDR COUNTER AND TAG BIT DECODE FOR O/E CH RESP TYPE 1JGH	B	DWG NO. 53575506	DATE 08/04/87	REV E
	SHEET NO. 9	60462210	PAGE 10-09		

ADU TAG BITS OUT RGTR




 CONTROL DATA	CMI CONTROL BOARD ADV TAG BITS OUT	B	DWG NO. 53575506	DATE 11/01/85	REV A
	TYPE 1JCH	SHEET NO. 10	60462210	PAGE 10	

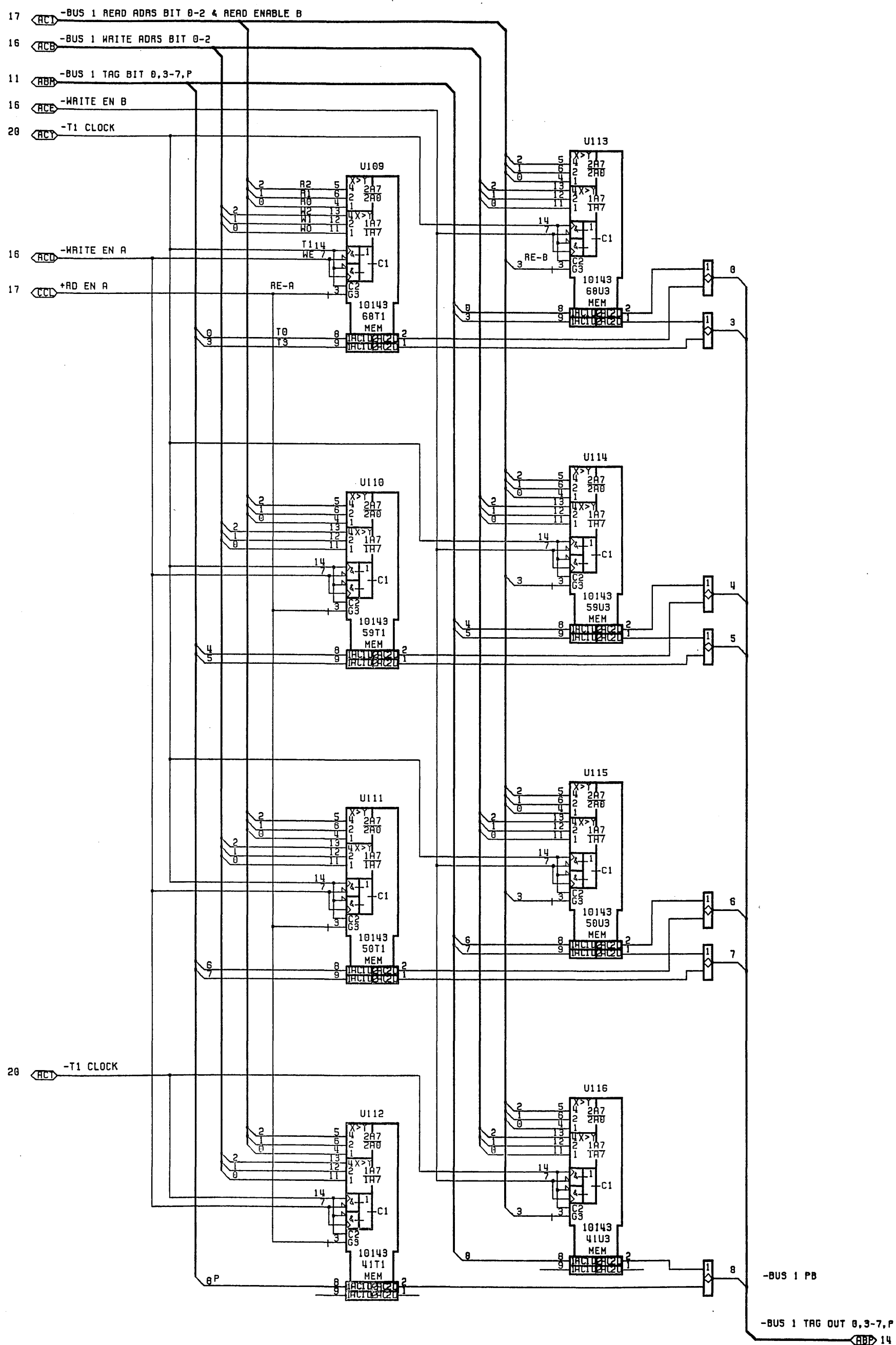
BUS 0 & 1 TAG OUT BITS GEN




1 NOT TERMINATED ON THIS BOARD

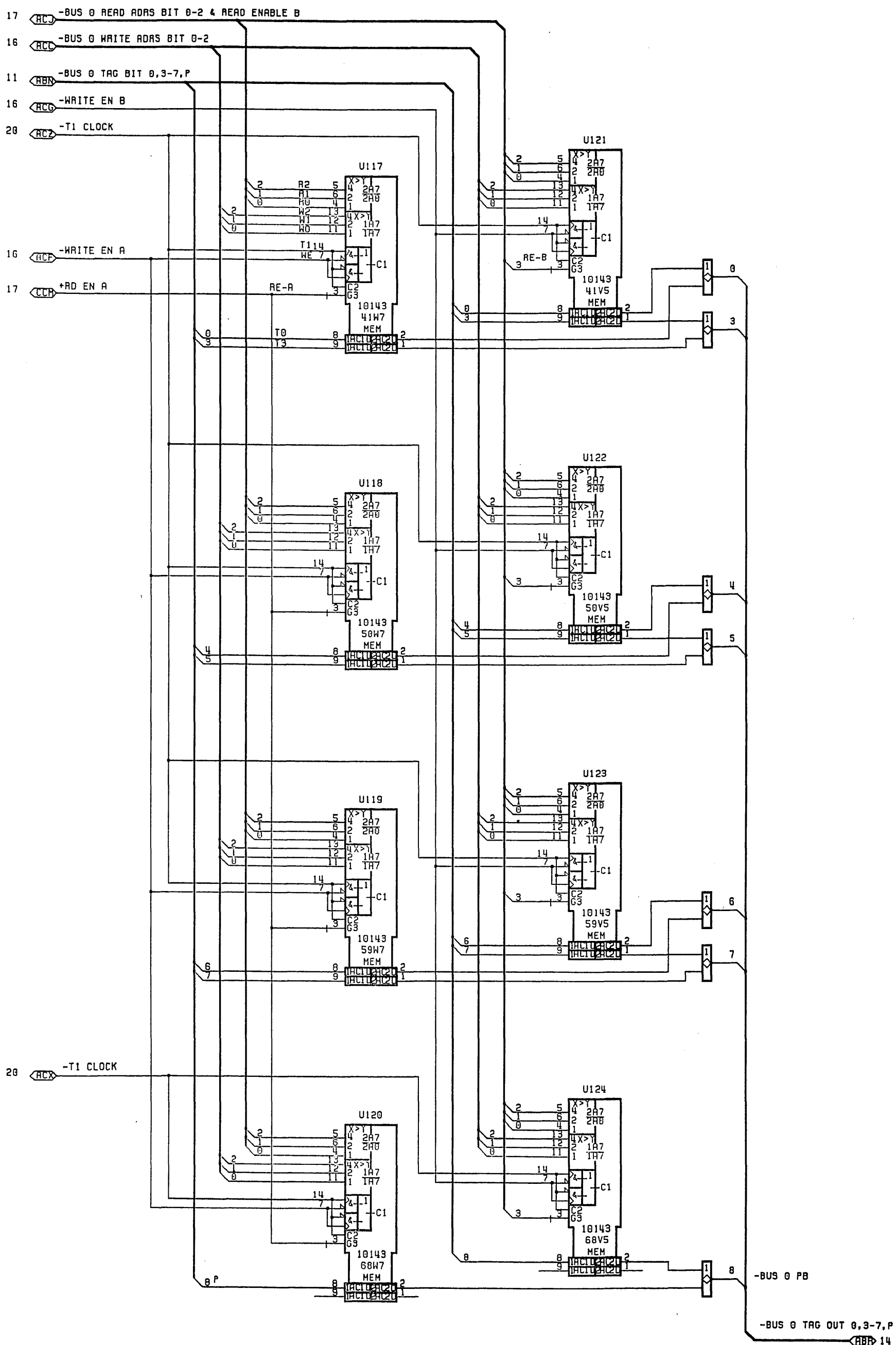
 CONTROL DATA	CMI CONTROL BOARD		B	DWG NO.	DATE	REV
	BUS 0 & 1 TAG BITS OUT AND			53575506	11/01/85	A
	CHANNEL GO FANOUT					
TYPE 1JGH		N	SHEET NO. 11		60462210	PAGE JG-11

BUS 1 TAG BITS OUT BUFFER



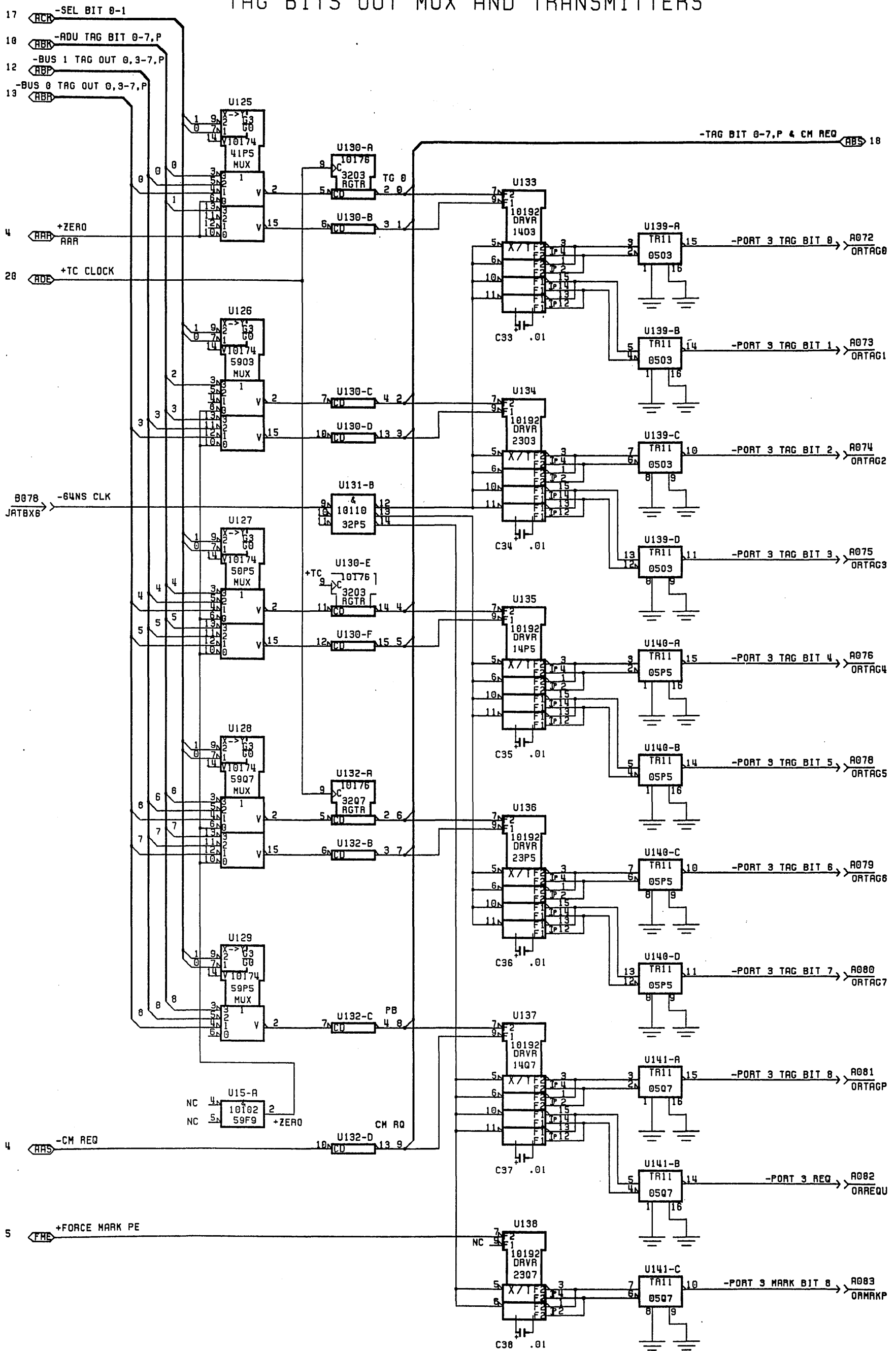
 CONTROL DATA	CHI CONTROL BOARD BUS 1 TAG BITS OUT BUFFER	B	DWG NO. 53575506	DATE 11/01/85	REV A
	TYPE 1JGH	SHEET NO. 12	60462210	PAGE	JG-12

BUS 0 TAG BITS OUT BUFFER



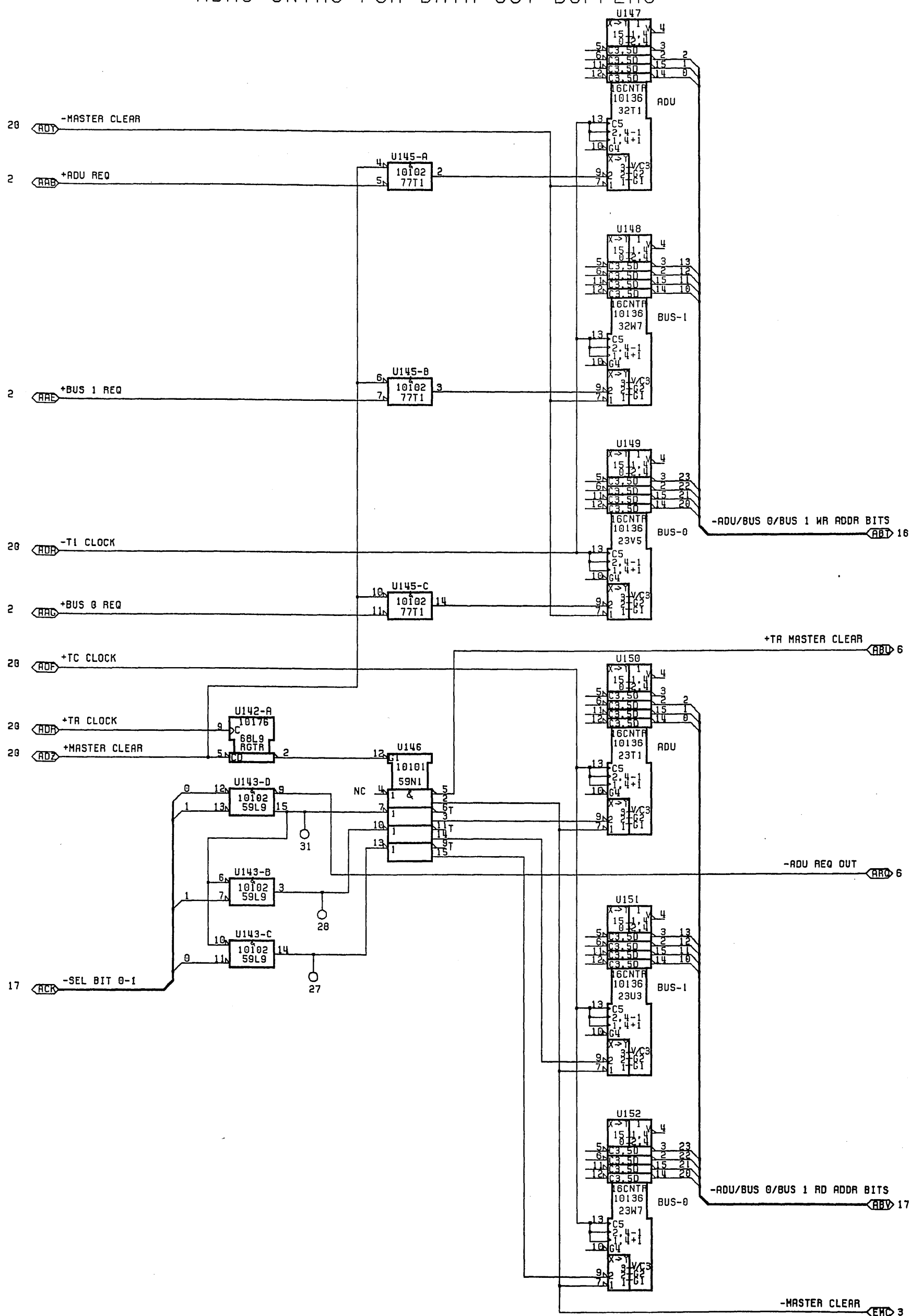
	CHI CONTROL BOARD		DWG NO.	DATE	REV
	BUS 0 TAG BITS OUT BUFFER		8	53575506	11/01/85
	TYPE 1JGH		SHEET NO. 13	60462210	PAGE 13

TAG BITS OUT MUX AND TRANSMITTERS



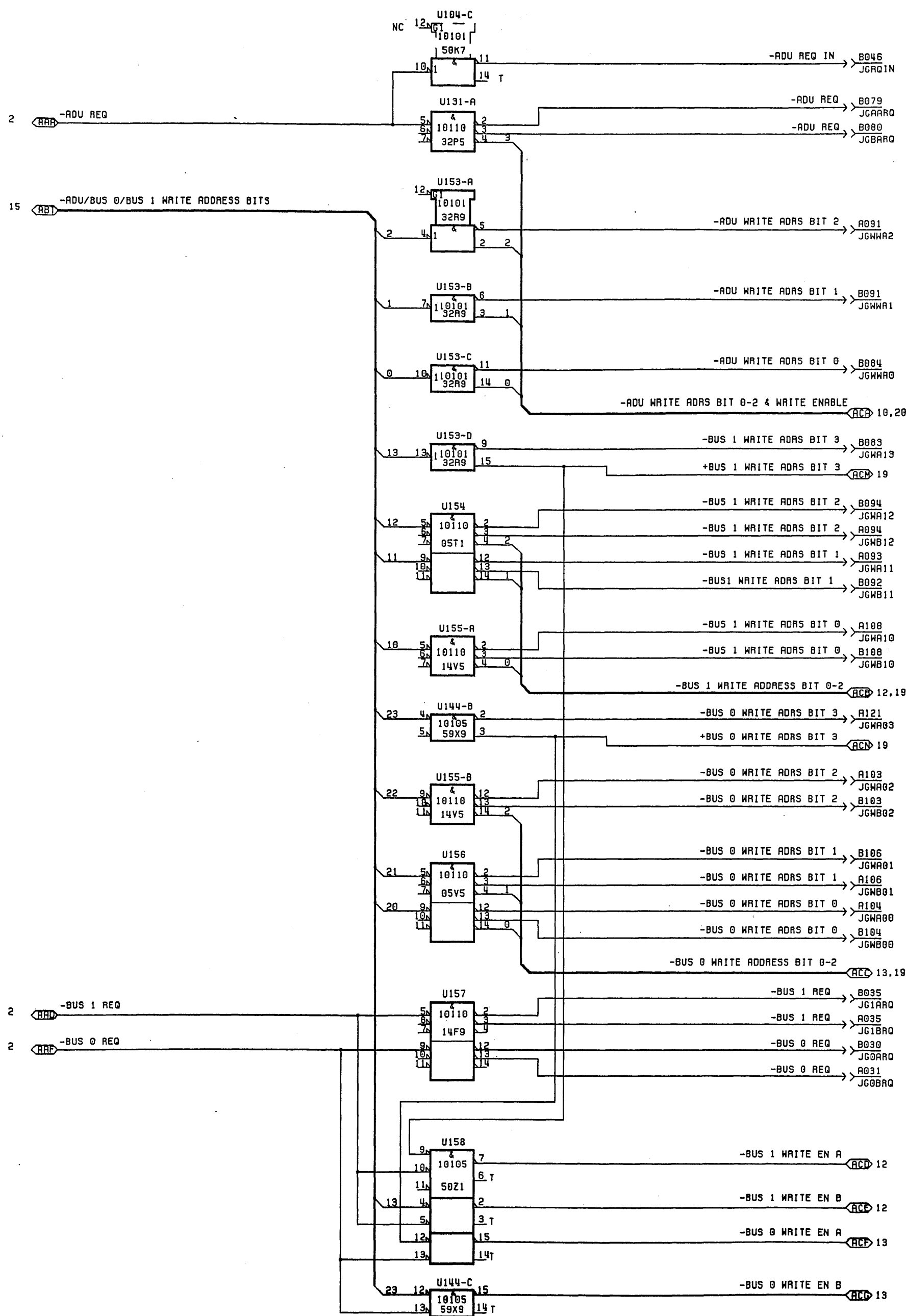
	CMI CONTROL BOARD TAG BITS OUT MUX AND TRANSMITTERS TYPE 1JGH				DWG NO. 53575508		DATE 11/01/85		REV A	
	SHEET NO. 14				60462210		PAGE		JG-14	
	N				60462210		PAGE		JG-14	

ADRS CNTRS FOR DATA OUT BUFFERS



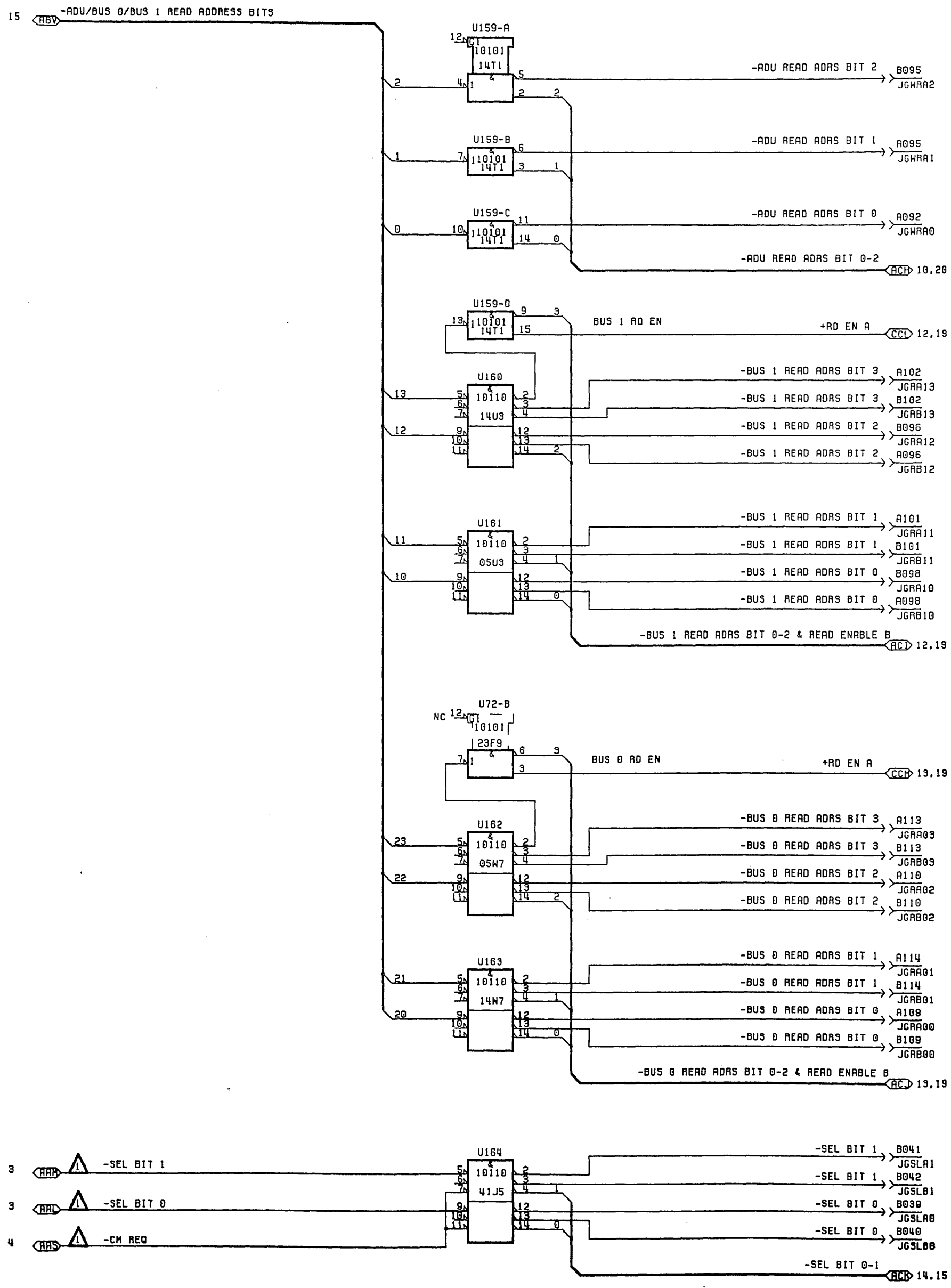
 CONTROL DATA	CMI CONTROL BOARD ADRS COUNTERS FOR DATA OUT BUFFER				B	DWG NO. 53575506	DATE 11/01/85	REV A
	TYPE 1JGH				N	SHEET NO. 15	60462210	PAGE JG-15

WRITE ADRS & WRITE ENBL F/O'S



CHI CONTROL BOARD WRITE ADDRESS & WRITE ENABLE FANOUTS FOR DATA OUT BUFFERS TYPE 1JGH	8	DWG NO.	DATE	REV
		53575508	11/01/85	A
		SHEET NO. 16	60462210	PAGE 16

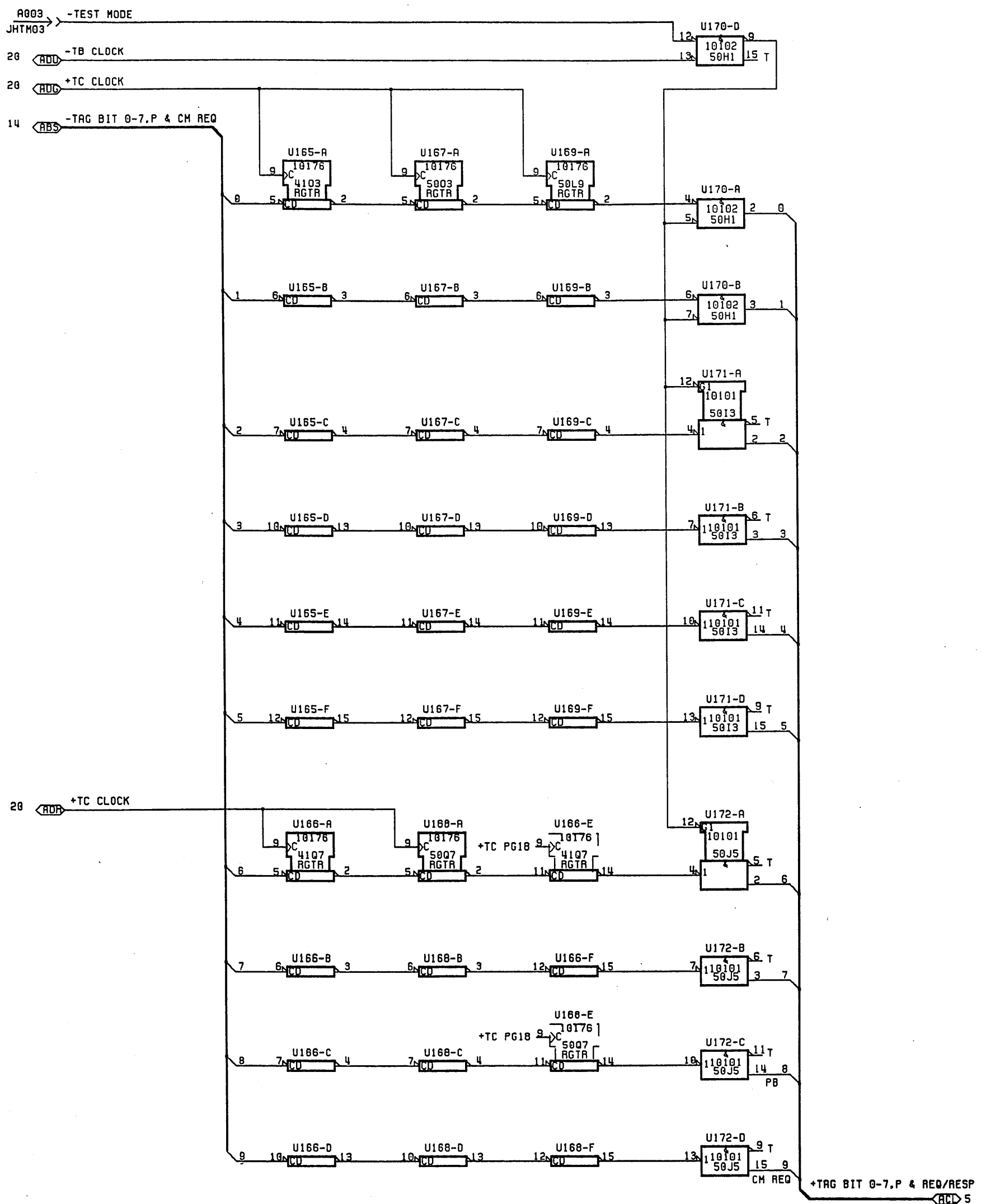
READ ADRS & READ ENBL F/O



1 SHORT

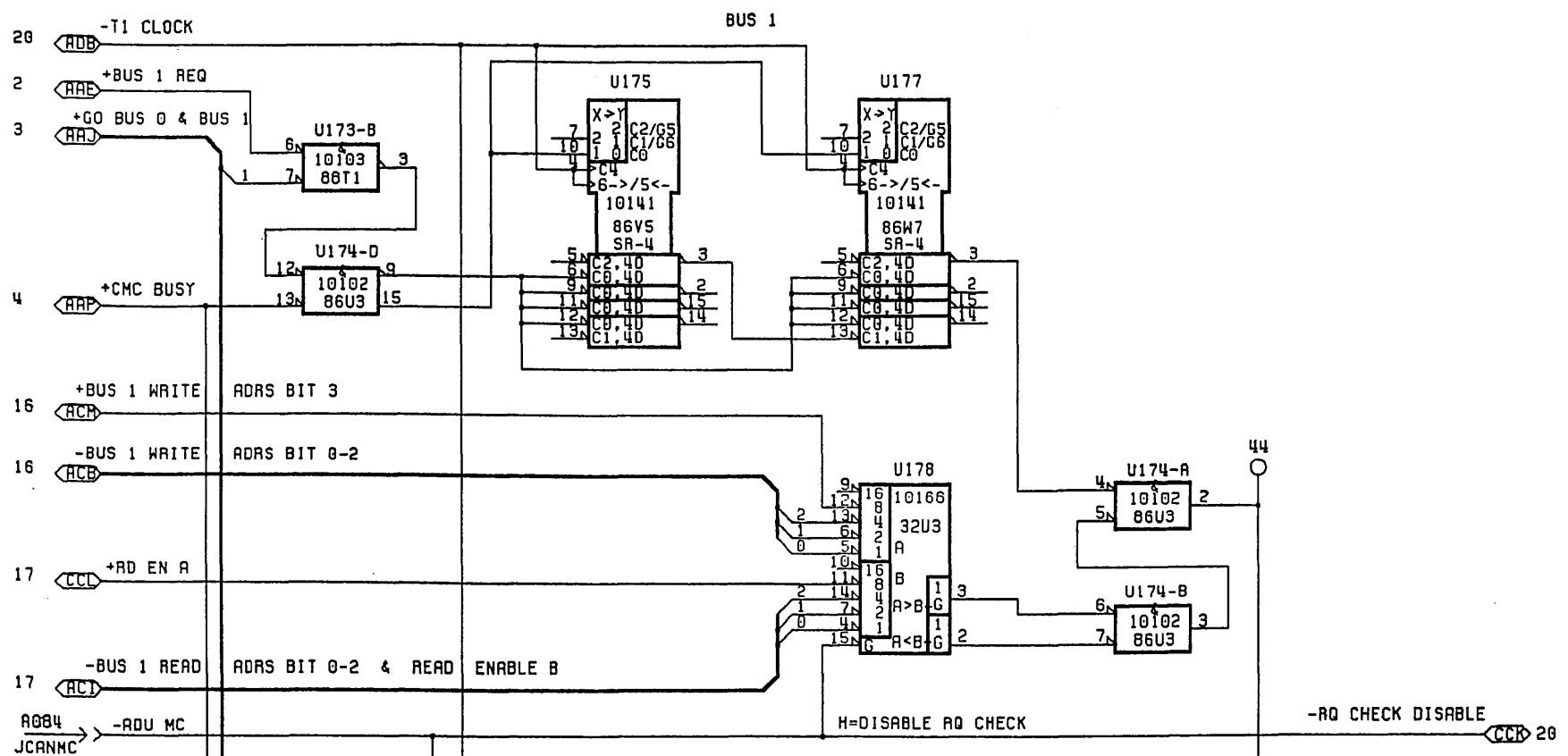
CONTROL DATA	CHI CONTROL BOARD READ ADRS & READ ENABLE FANOUT FOR DATA OUT BUFFERS TYPE 1JGH	B	DWG NO. 53575508	DATE 11/01/85	REV A
			SHEET NO. 17	60462210	PAGE 17

TAG BITS 0-7, PAR AND CM REQ FOR SELF-TEST MODE

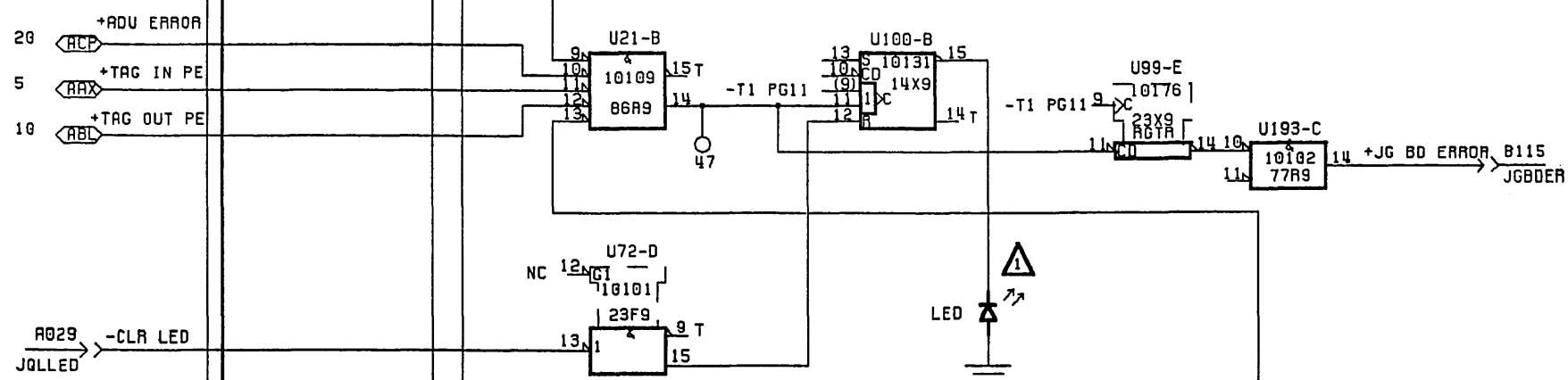


	CHI CONTROL BOARD		DWG NO.	DATE	REV
	TAG BIT 0-7, P AND CM REQ		53575508	11/01/85	A
TYPE 1JCH		SHEET NO. 18	60462210	PAGE	JG-18

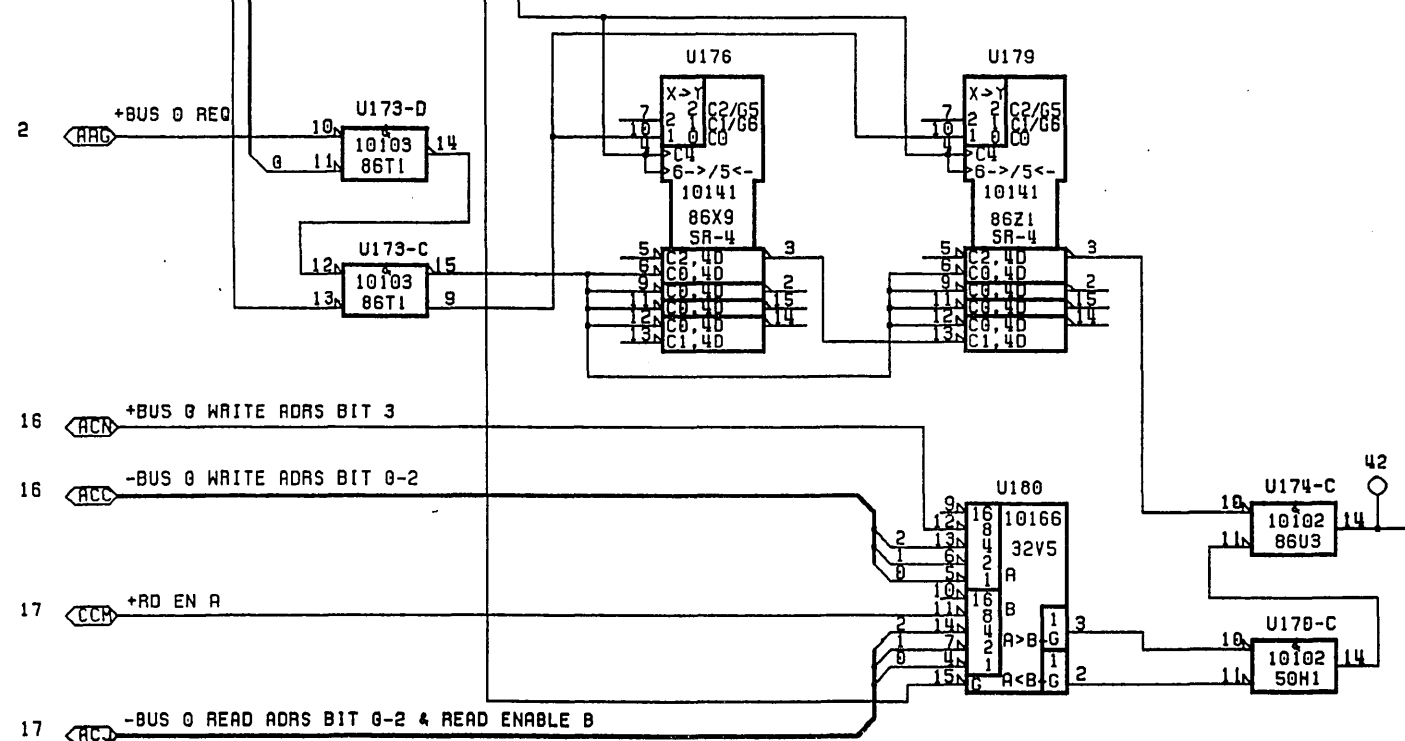
BUS 1 ERROR CHECKER



ERROR MUX



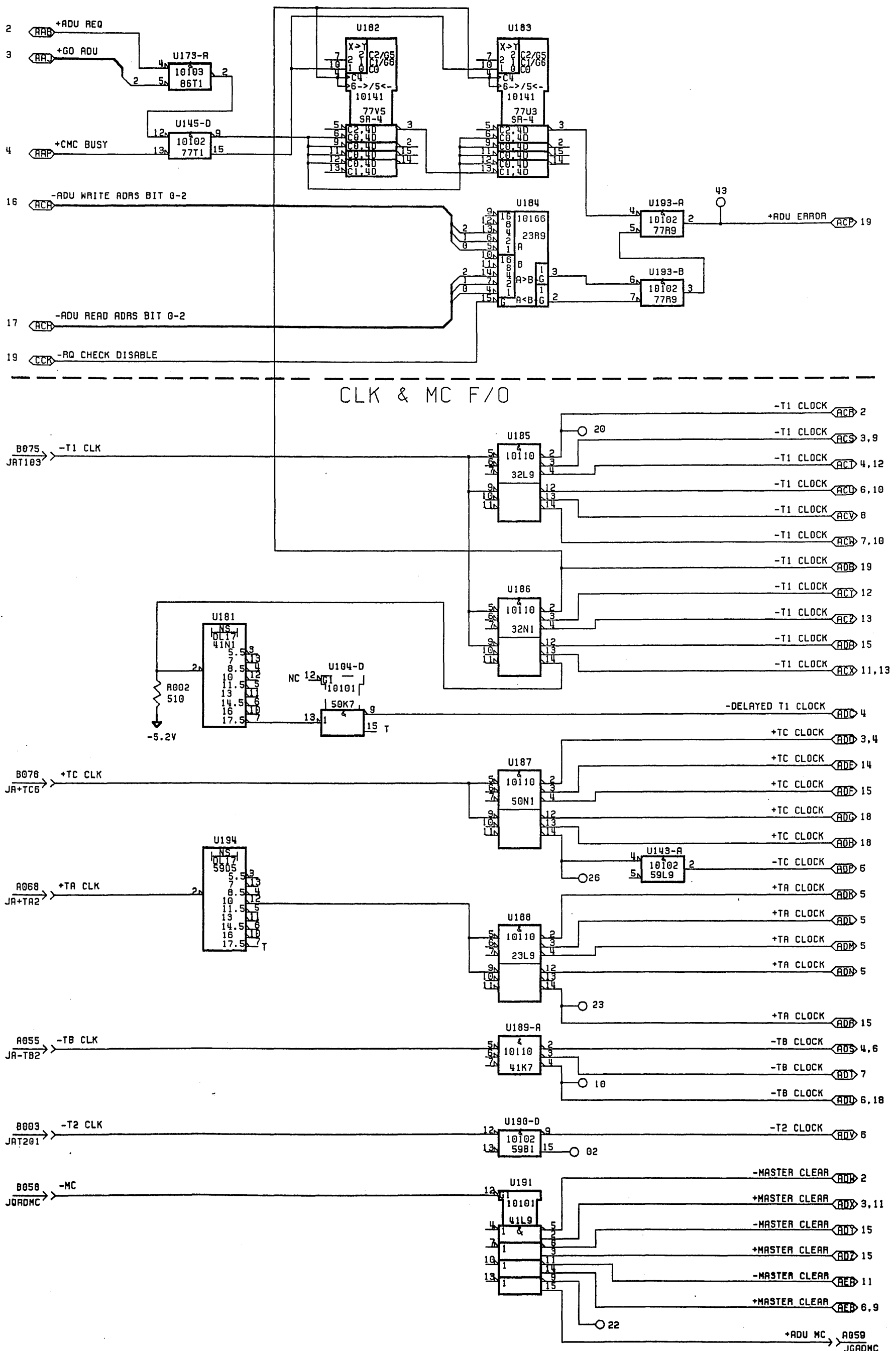
BUS 0 ERROR CHECKER



△ TERMINATE

	CHI CONTROL BOARD		DWG NO.	DATE	REV
	BUS 0 & 1 ERROR CHECKER		53575506	11/01/85	A
TYPE 1JGH		SHEET NO.	19	60462210	PAGE
		JG-19			

ADU ERROR CHECKER



CHI CONTROL BOARD
ADU ERROR CHECKER,
CLOCK & MASTER CLEAR FANOUT
TYPE 1JGH

B

ING NO.

DATE _____

REV


SHEET NO. 20

60462210

PAGE 16-20

TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	05	-RESPONSE	27	15	+BUS 0 RQ OUT
02	20	-T2 CLOCK	28	15	+BUS 1 RQ OUT
03	08	-RESPONSE (RESYNC)	29	03	-PRIORITY F/F A
04	09	-TAG IN BIT 4	30	03	-PRIORITY F/F B
05	08	-TAG IN BIT 7	31	15	+ADU RQ OUT
06	09	-TAG IN BIT 5	32	09	-ADU IN RD ADRS B0
07	09	-TAG IN BIT 6	33	03	-BUS 0 GO
08	08	-BUS RESPONSE	34	02	-BUS 0 CM REQUEST
09	04	-RESYNC BUFFER FULL	35	02	-BUS 0 CM RQ CNT=0
10	20	-TB CLOCK	36	02	-BUS 1 CM RQ CNT=0
11	04	-RESYNC 0 F/F	37	02	-ADU CM REQUEST
12	04	-RESYNC 1 F/F	38	03	-BUS 1 GO
13	04	-RESYNC 2 F/F	39		
14	04	-RESYNC 3 F/F	40		
15	05	+TAG IN P.E.	41	02	-BUS 1 CM REQUEST
16	04	-CM REQUEST (RESYNC)	42	19	+BUS 0 RQ ERROR
17	06	-ADU IN WRT ADRS B1	43	20	+ADU RQ ERROR
18	03	-ADU GO	44	19	+BUS 1 RQ ERROR
19	02	-ADU CM RQ COUNT=0	45	04	+CMC BUSY
20	20	-T1 CLOCK	46	11	-CHANNEL 4 GO
21	06	-ADU IN WRT ADRS B0	47	19	-BOARD ERROR
22	20	-MASTER CLEAR	48	10	+TAG OUT P.E.
23	20	+TA CLOCK	49	11	-CHANNEL 0 GO
24	09	-ADU IN RD ADRS B1	50	11	-CHANNEL 1 GO
25	11	-CHANNEL 3 GO	51	11	-CHANNEL 2 GO
26	20	+TC CLOCK			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 [NOT USED]
TERM	NONE
UNUSED	A037, B037, A099, A100, B100, A105, A111, B111, A112, B112, A127, B127, A128, B128

	CHI CONTROL BOARD		DWG NO.	DATE	REV
	TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JGH		B 53575506	11/01/85	A
		SHEET NO. 21	60462210	PAGE	JG-21

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

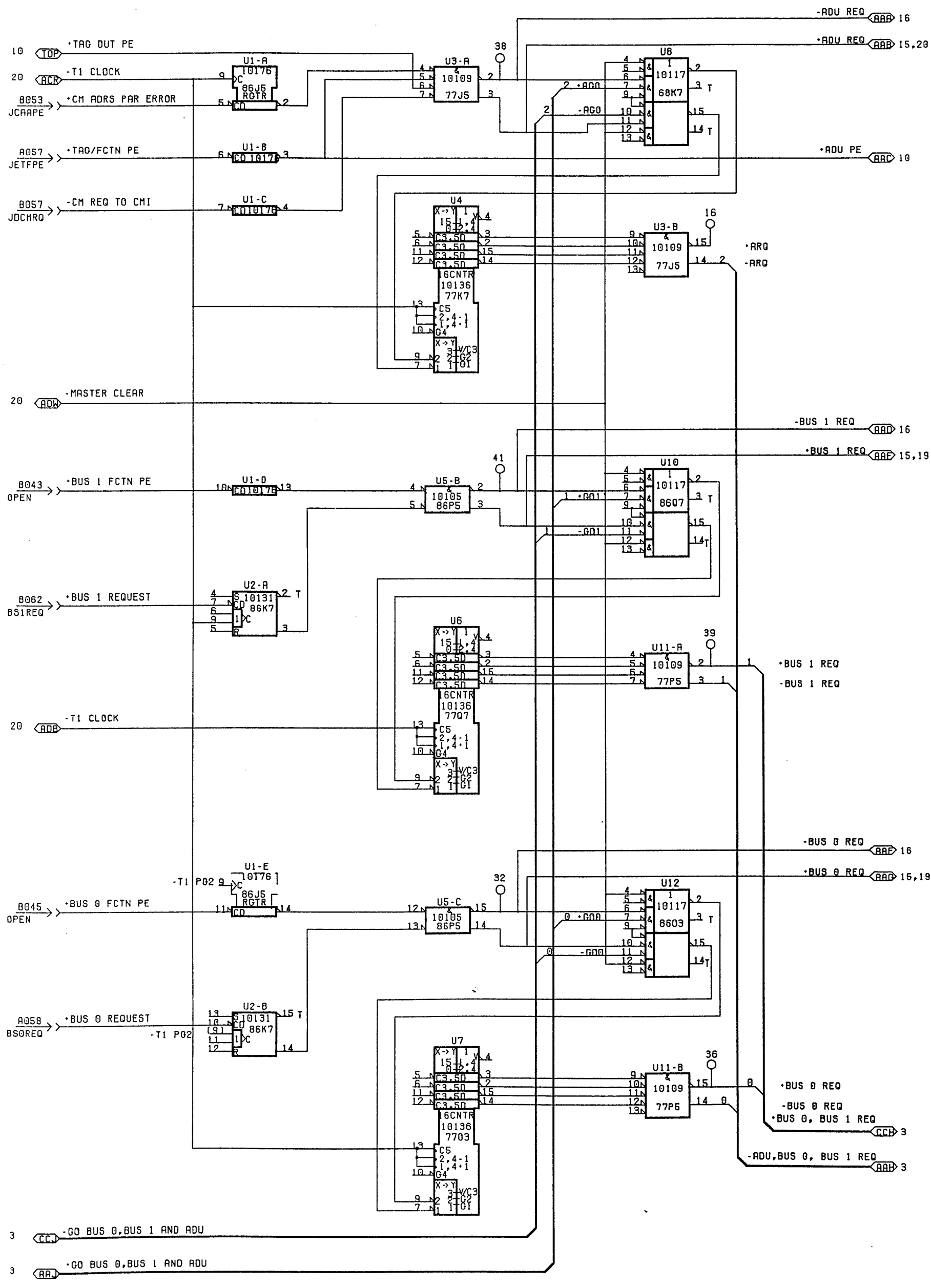
CMI CONTROL BOARD


DWN	L H JOHNSON	12/13/85
CHKD	J P STROMBECK	01/08/86
ENG	J P STROMBECK	01/08/86
PUBS	R K BONDE	01/08/86
APP	J P STROMBECK	01/08/86

LOC: A08

4-199●

REQ CONTROL

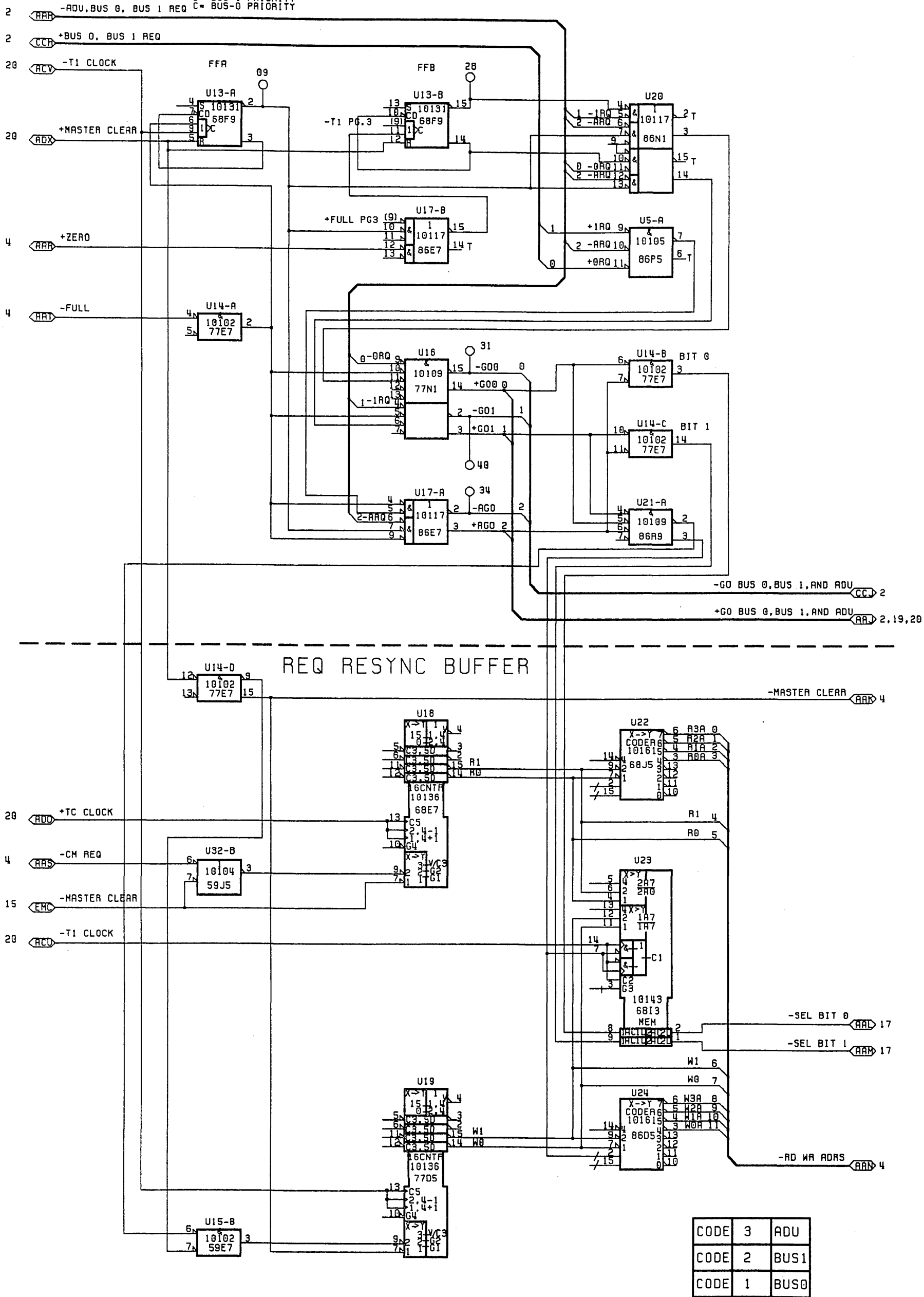


 CONTROL DATA	CMI CONTROL BOARD REQUEST CONTROL	B	DWG NO. 22105673	DATE 06/16/88	REV C
	TYPE 1JGH		SHEET NO. 2	60462210	PAGE JG-02
		N			

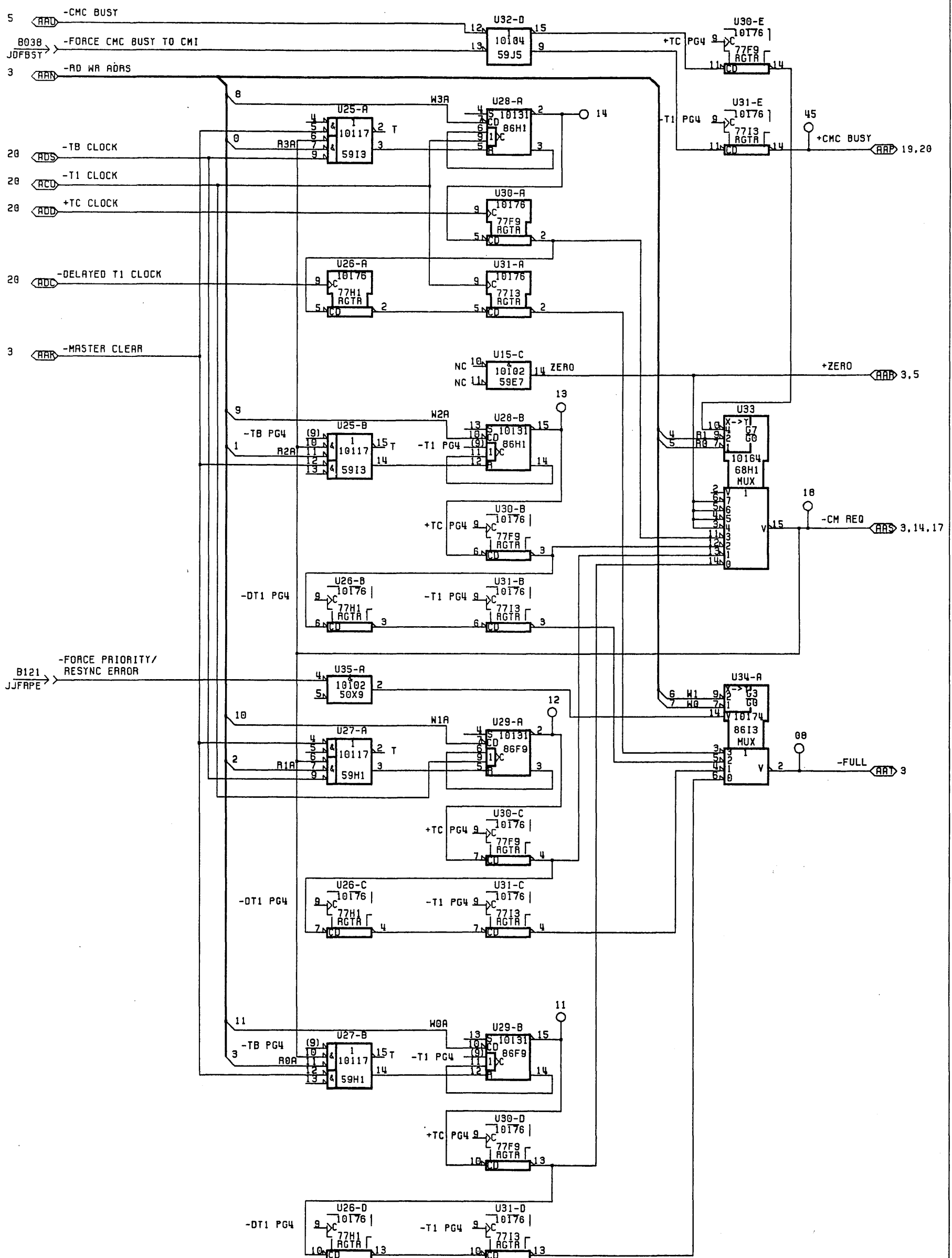
FFA= C A B A C A B
 FFB=


A= ADU PRIORITY
 B= BUS-1 PRIORITY
 C= BUS-0 PRIORITY

PRIORITY CONTROL

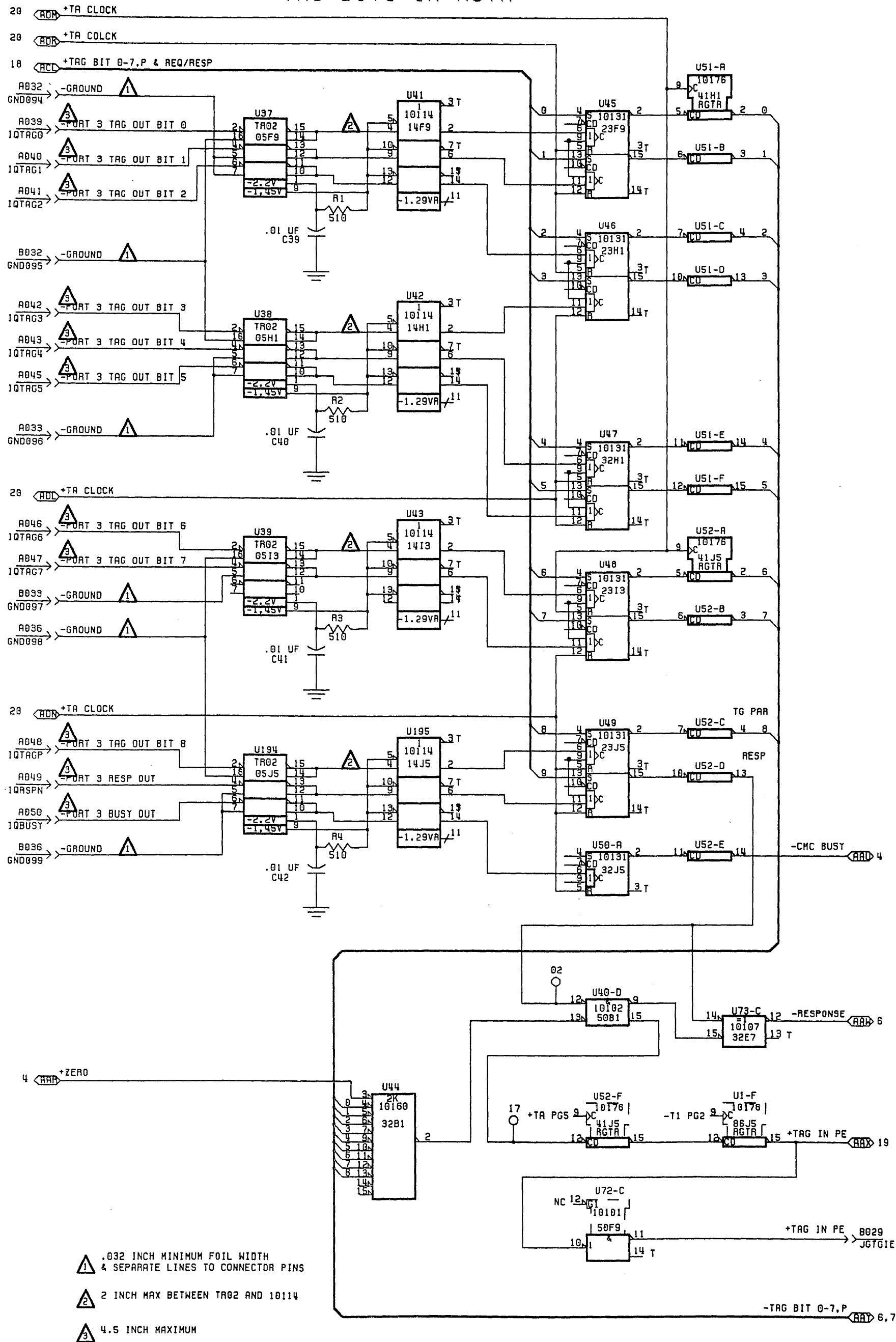


REQ RESYNC F/F'S



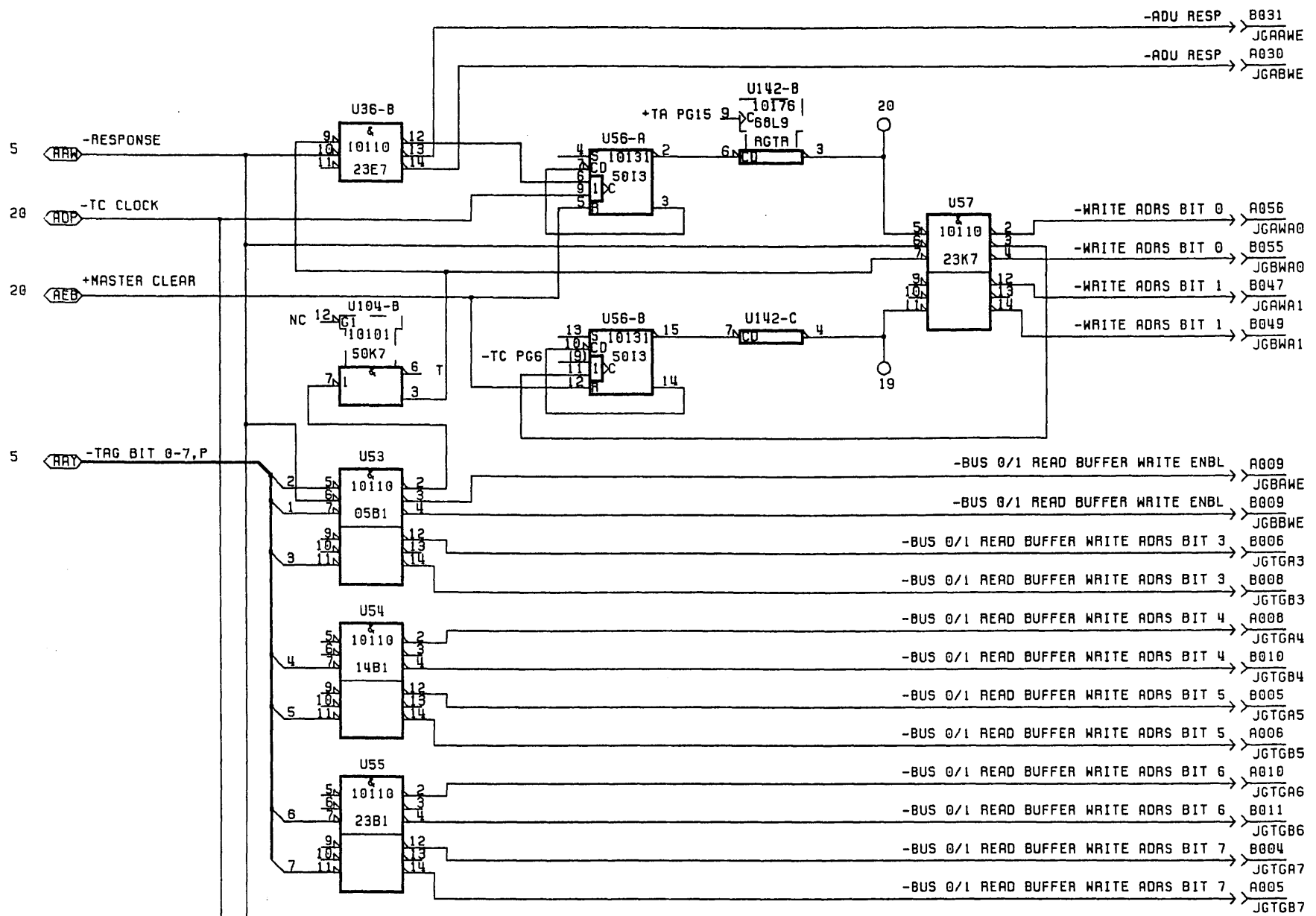
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			22105673	12/13/85	A
N		SHEET NO. 4	60462210	PAGE	JG-04

TAG BITS IN RGTR

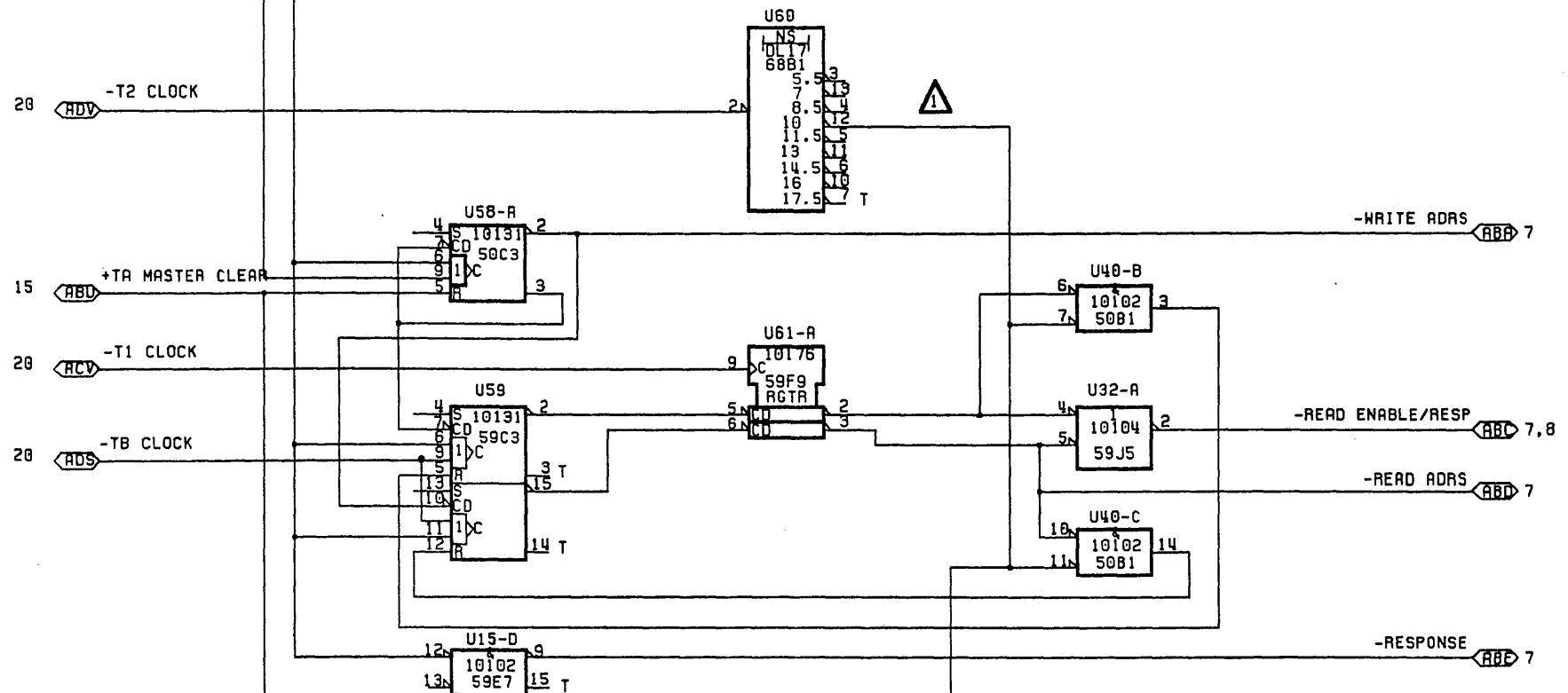


CHI CONTROL BOARD TAG BITS IN TYPE 1JGH	B	DWG NO.	DATE	REV
		22185673	07/18/86	B
		SHEET NO. 5	60462210	PAGE 16-05

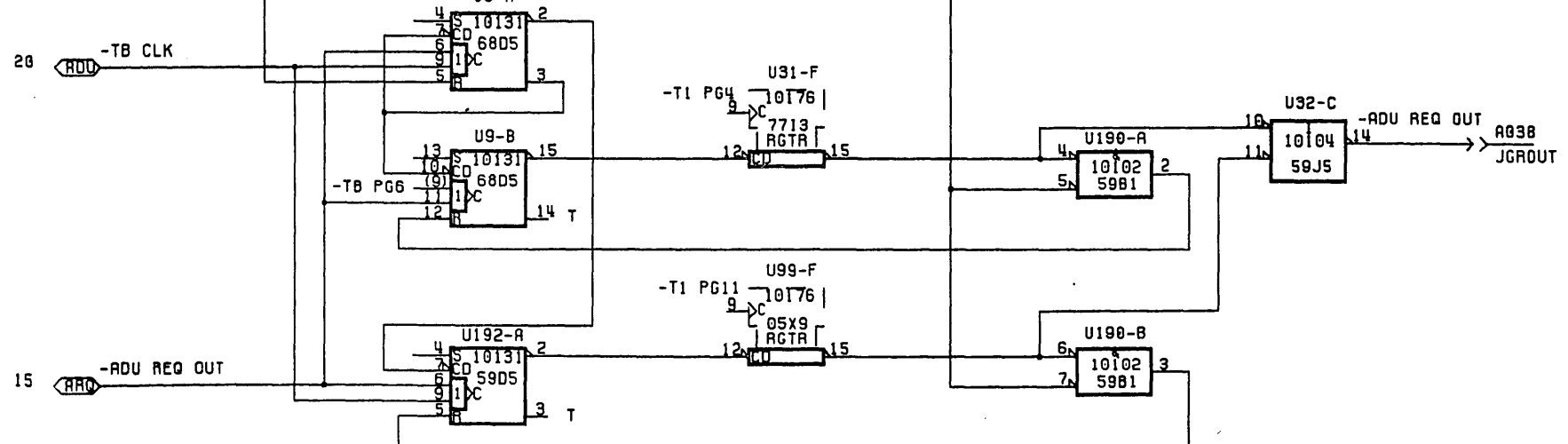
TAG BITS IN F/O




RESP RESYNC



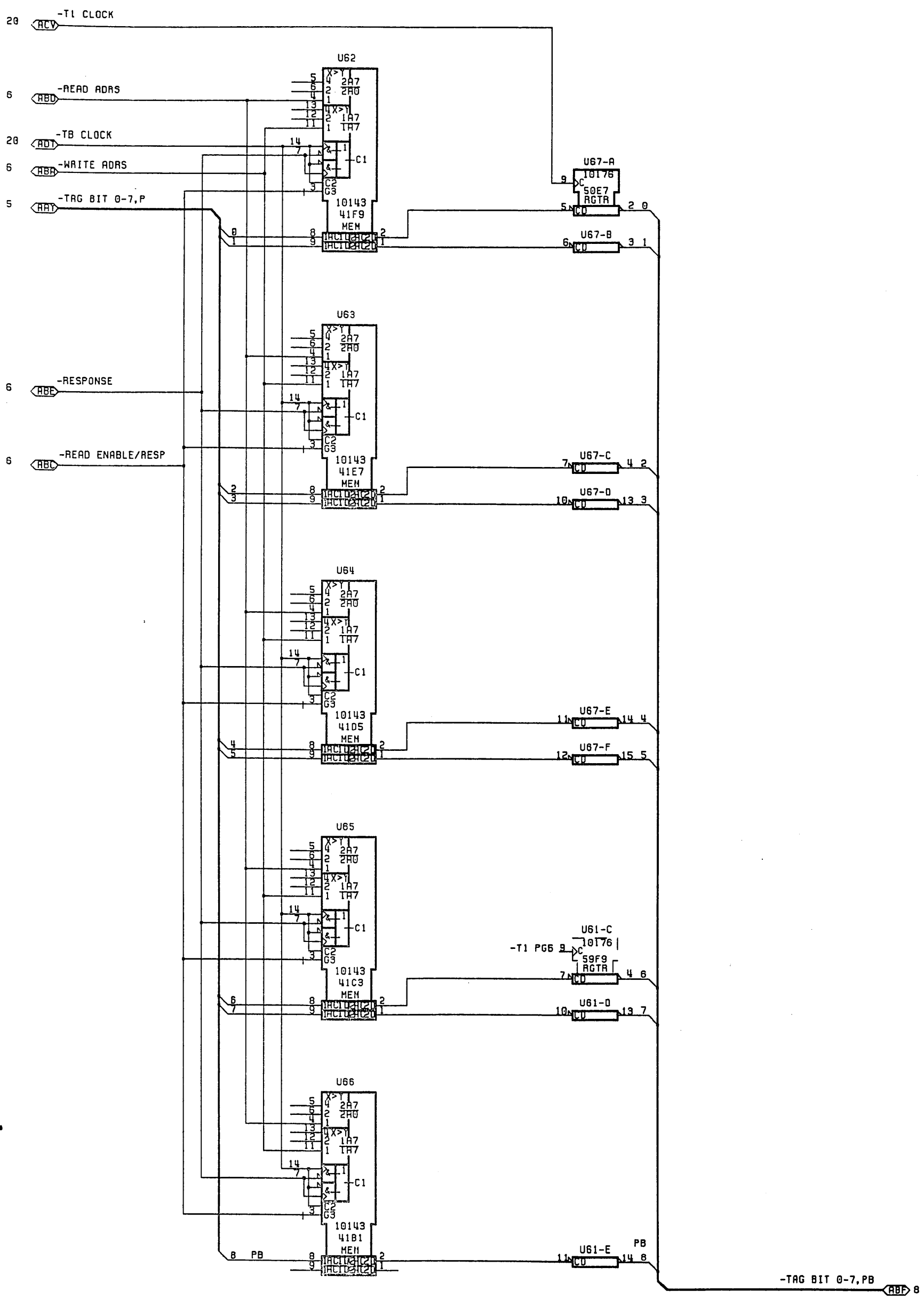
ADU REQ OUT RESYNC




6 INCH MAXIMUM

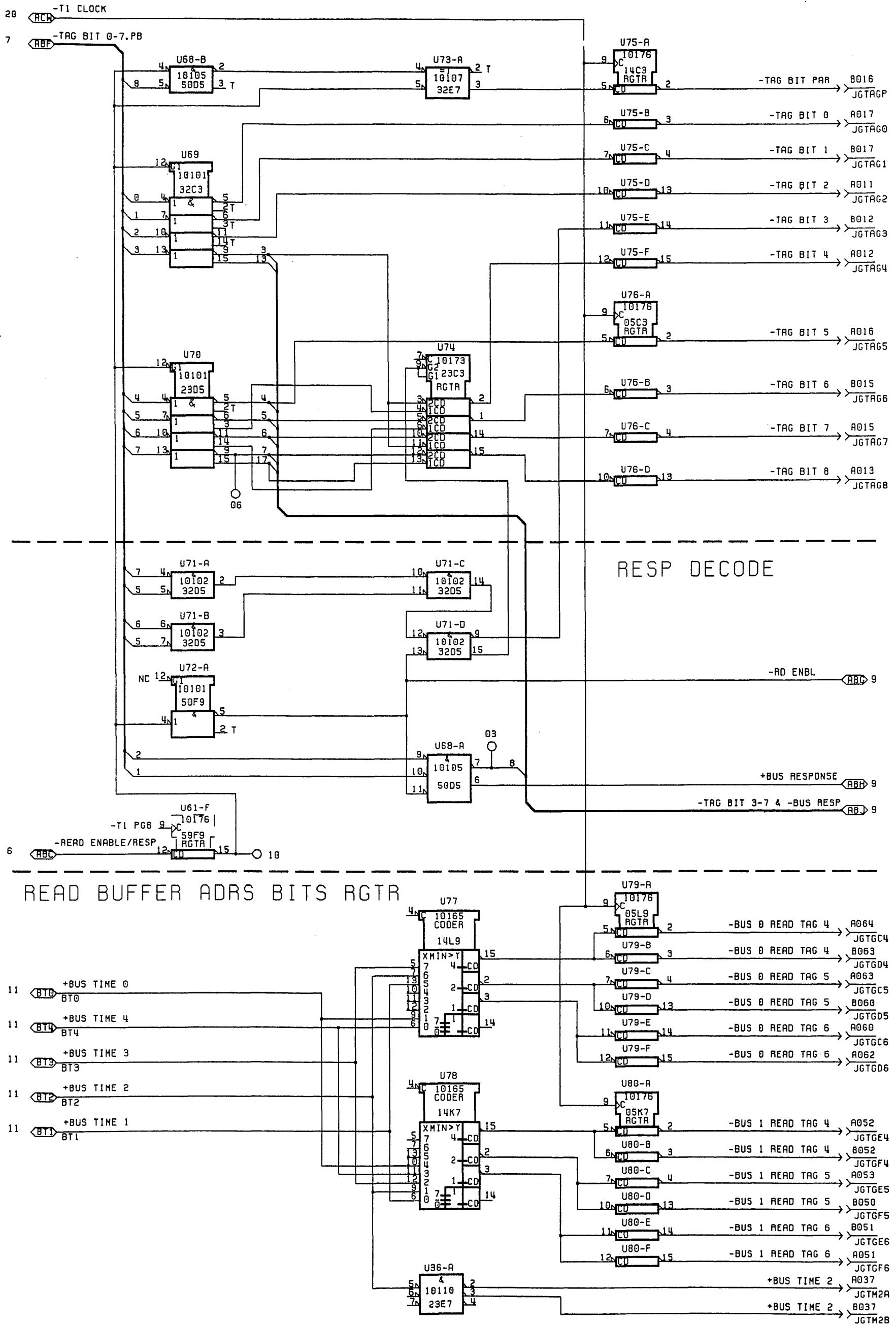
 CONTROL DATA	CHI CONTROL BOARD		B	DWG NO.	DATE	REV		
	TAG BITS IN, RESPONSE RESYNCH			22105673	12/13/85	A		
	AND ADU REQ OUT RESYNCH							
	TYPE 1JGH		N	SHEET NO.	6	60462210	PAGE	JG-06


TAG BITS IN BUFFER



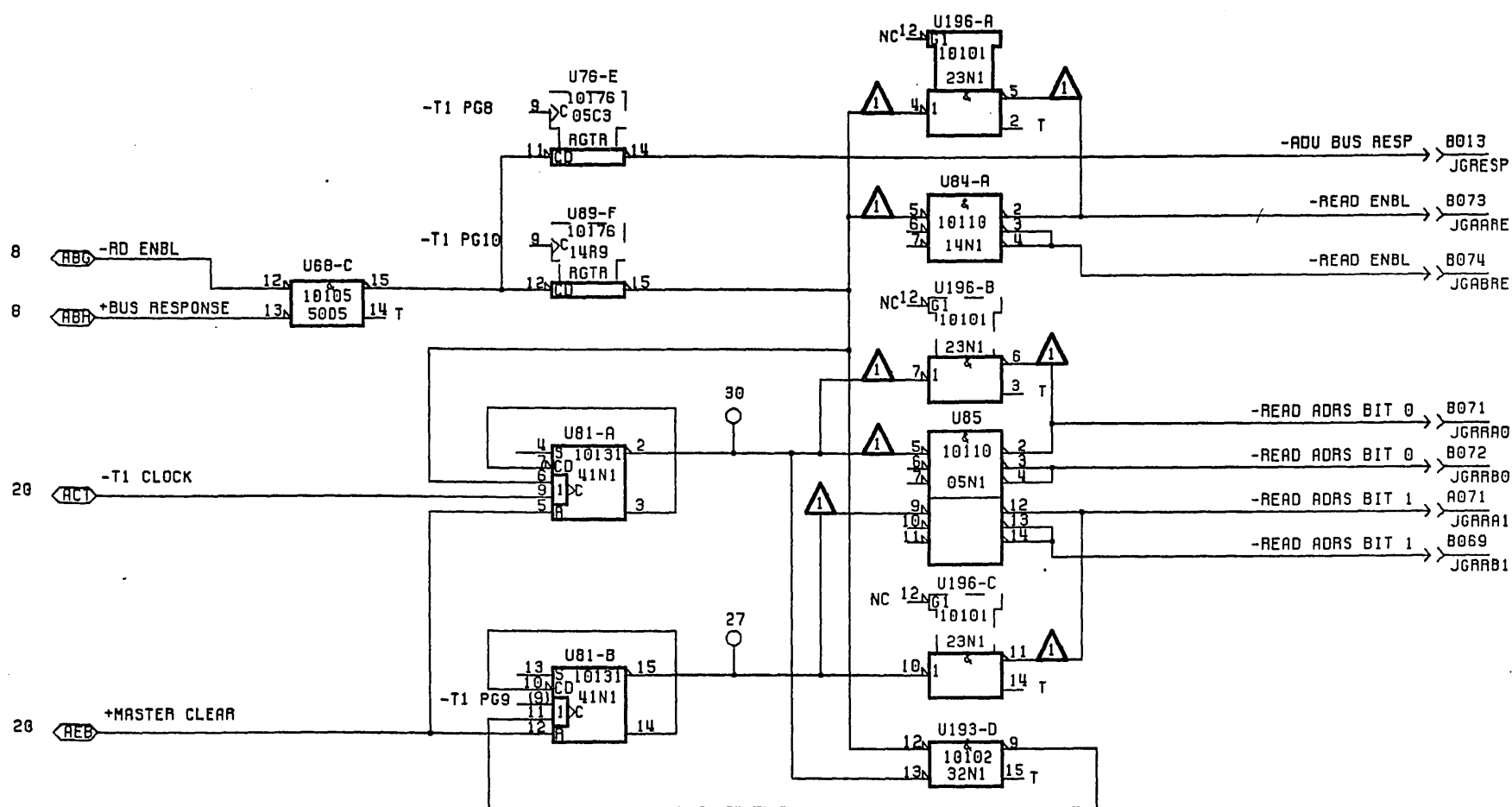
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				22105673	12/13/85	A
	TYPE 1JGH					
			N	SHEET NO. 7	60462210	PAGE JG-07

TAG IN 8-9 BIT CONVERSION

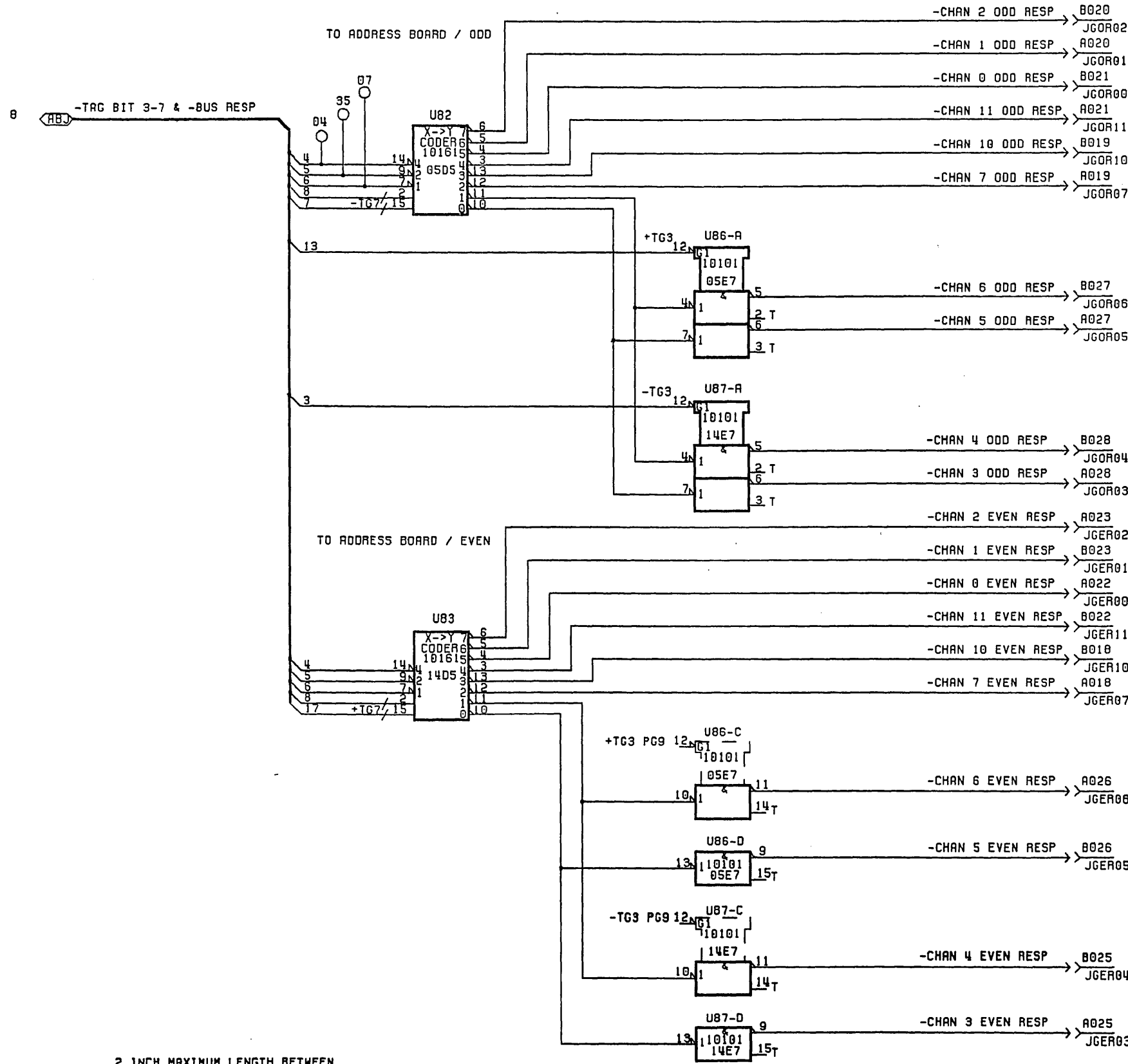


 CONTROL DATA	CMI CONTROL BOARD TAG BIT IN 8-9 BIT CONVERSION, RD BUFFER ADAS BITS & RESP DECODE	B	DWG NO. 22105673	DATE 07/18/86	REV B
	TYPE 1JGH	N	SHEET NO. 8	60462210	PAGE 16-08

ADU READ ADRS CNTR



TAG BIT DCDR FOR ODD/EVEN CHAN RESP

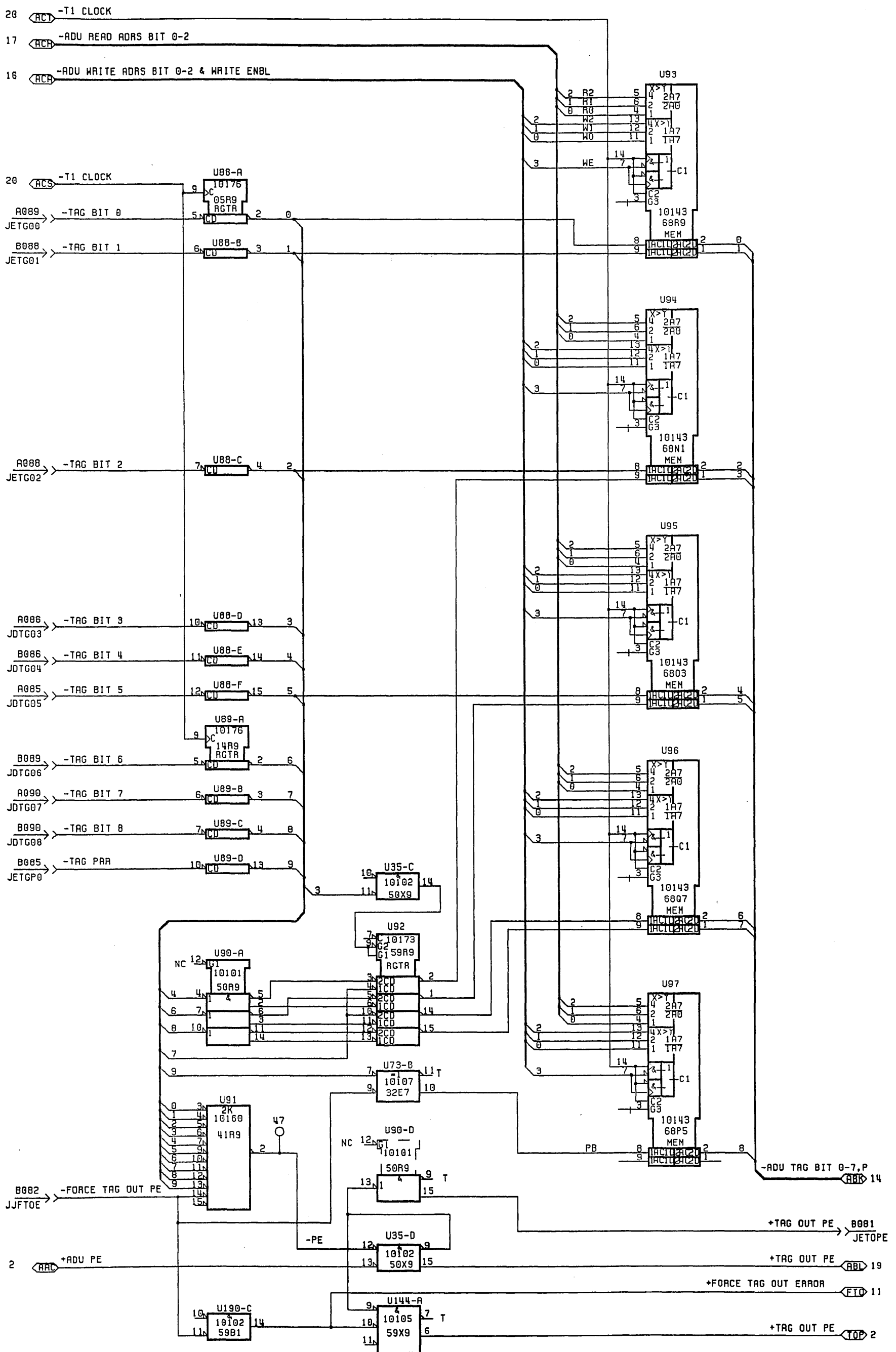



2 INCH MAXIMUM LENGTH BETWEEN THE TWO INPUT PINS & THE TWO OUTPUT PINS.

	CHI CONTROL BOARD ADU READ ADRS COUNTER AND TAG BIT DECODE FOR O/E CH RESP TYPE 1JGH	B	DWG NO. 22105673	DATE 12/13/85	REV A

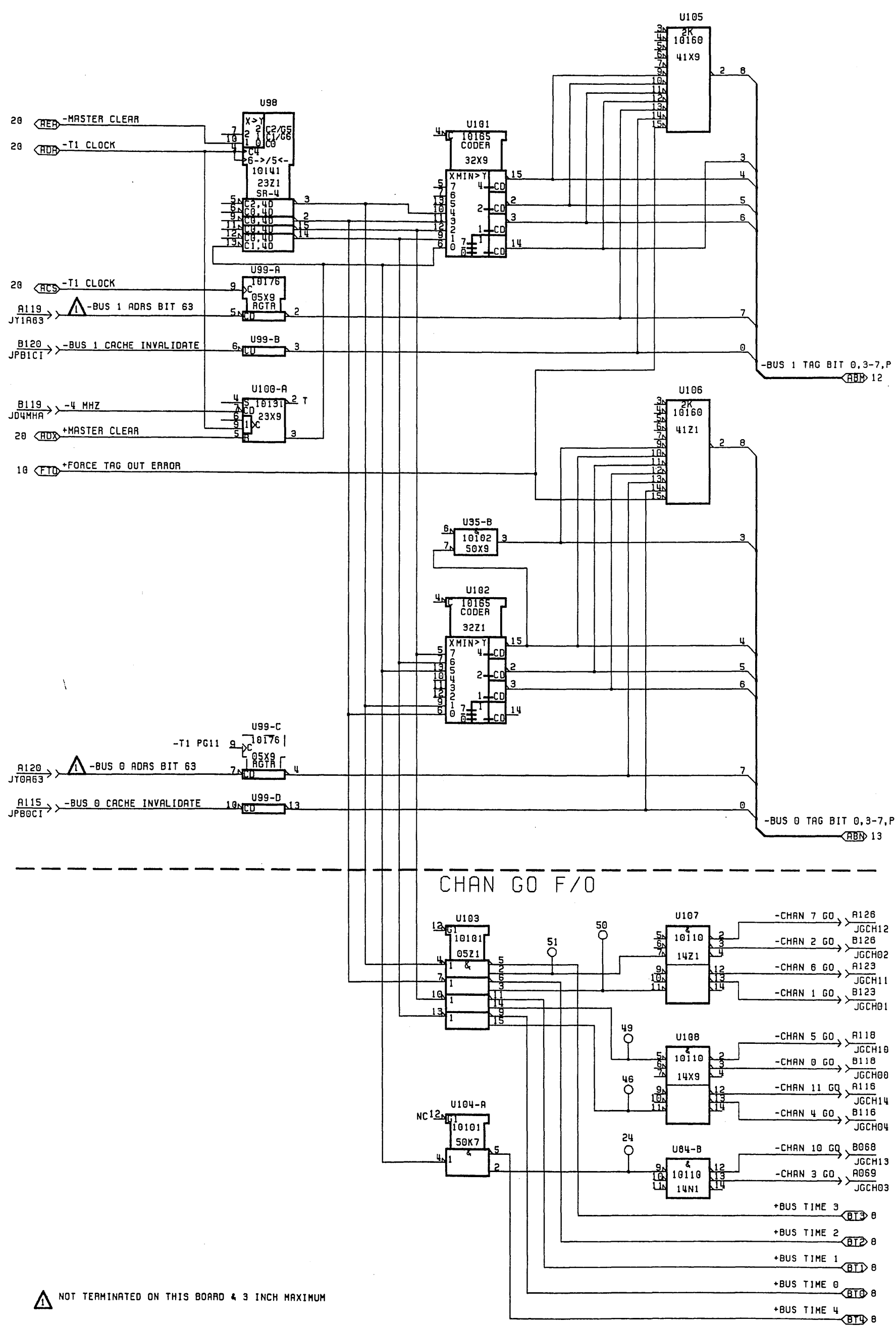
SHEET NO. 9 60462210 PAGE JG-09

ADU TAG BITS OUT RGTR



 CONTROL DATA	CMI CONTROL BOARD ADU TAG BITS OUT	B	DWG NO. 22105673	DATE 12/13/85	REV A
	TYPE 1JCH	SHEET NO. 10	60462210	PAGE	JG-10

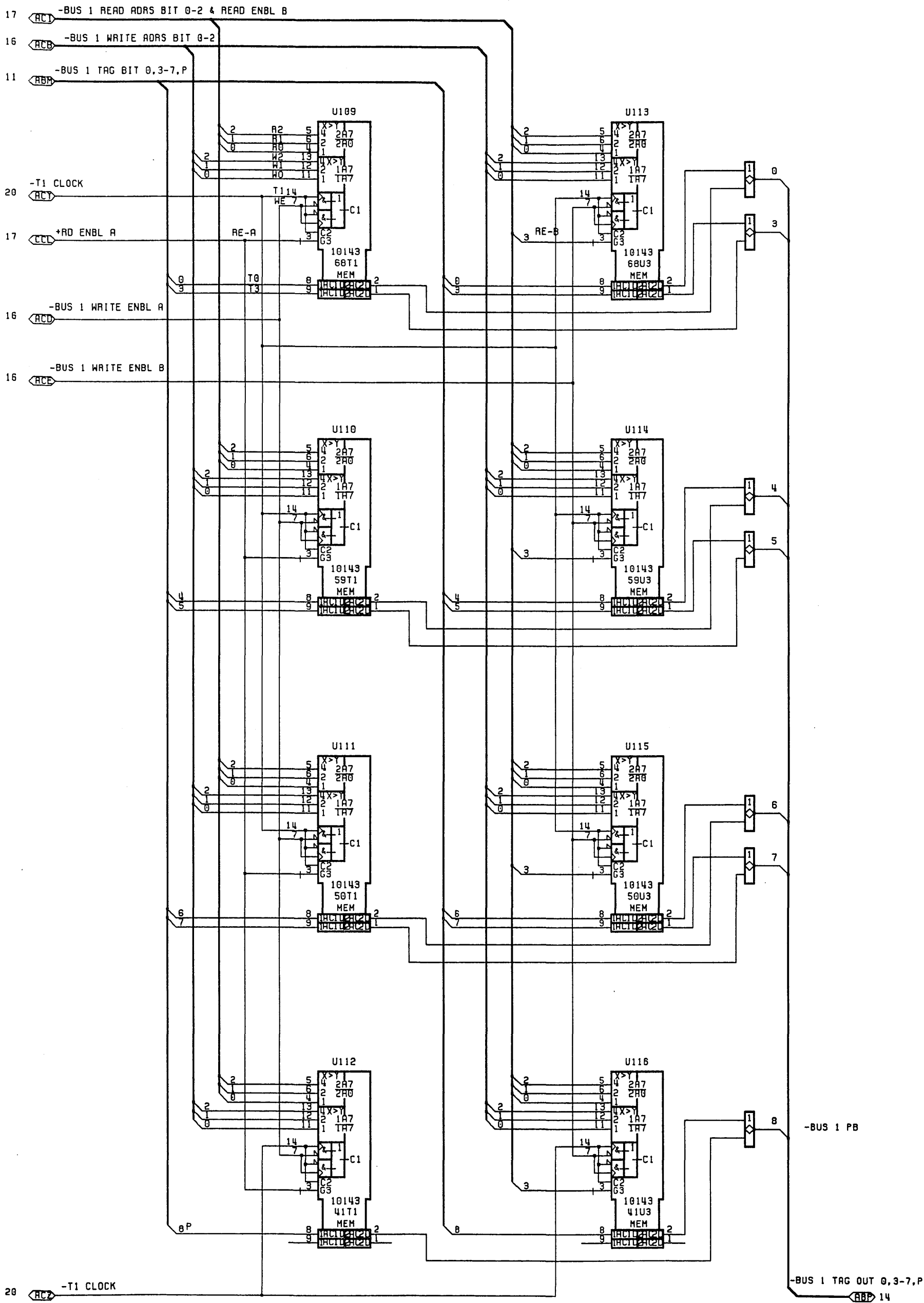
BUS 0 & 1 TAG OUT BITS GEN



⚠ NOT TERMINATED ON THIS BOARD & 3 INCH MAXIMUM

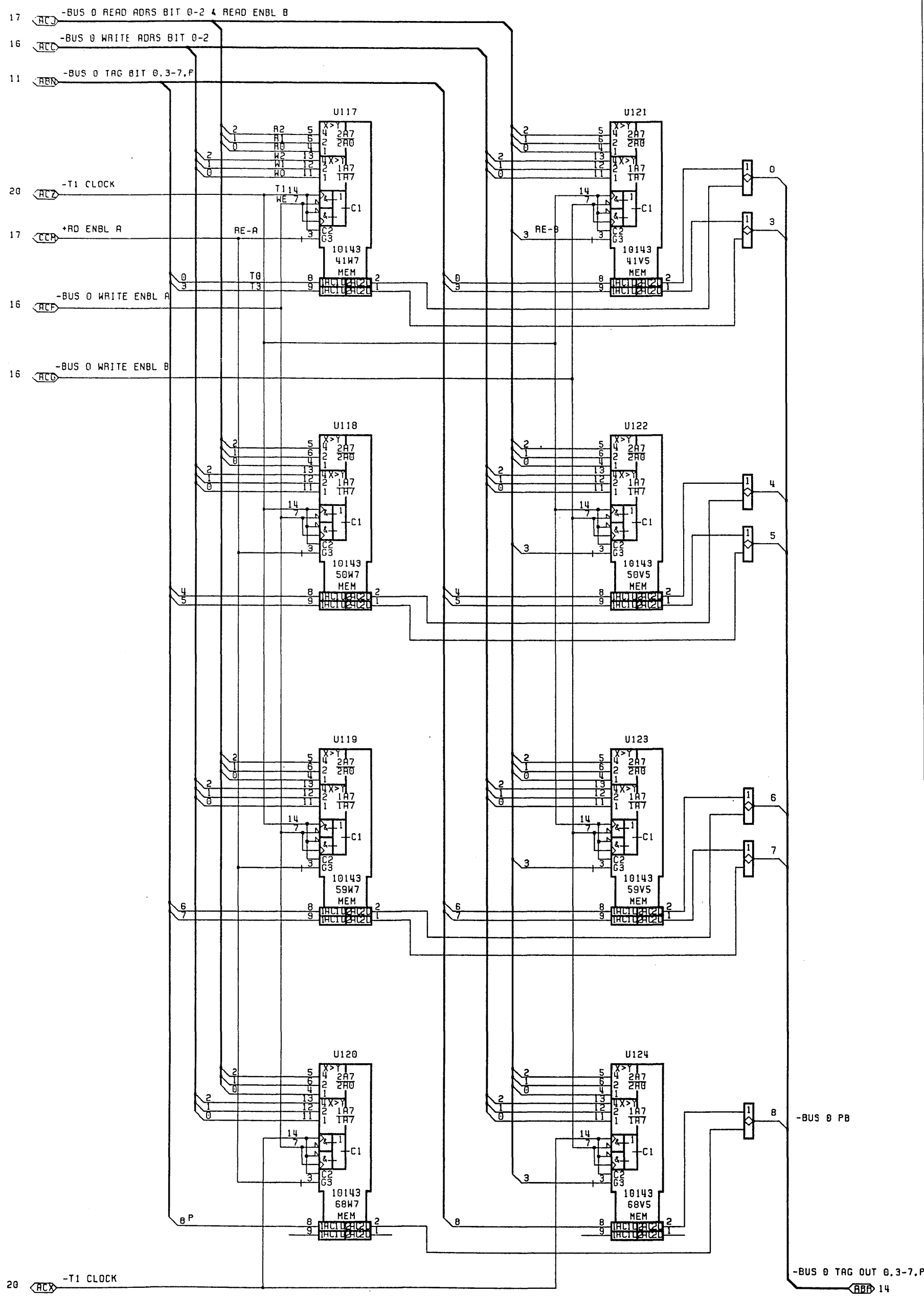
GD CONTROL DATA	CMI CONTROL BOARD BUS 0 & 1 TAG BITS OUT AND CHANNEL GO FANOUT TYPE 1JCH		B	DWG NO.	DATE	REV
				22105673	07/18/86	B
				SHEET NO. 11	60462210	PAGE JG-11

BUS 1 TAG BITS OUT BUFFER



CMI CONTROL BOARD BUS 1 TAG BITS OUT BUFFER TYPE 1JGH	B	DWG NO.	DATE	REV
		22105673	12/13/85	A
		SHEET NO. 12	60462210	PAGE 10-12

BUS 0 TAG BITS OUT BUFFER



CMI CONTROL BOARD BUS 0 TAG BITS OUT BUFFER TYPE 1JGH	B	DWG NO.	DATE	REV
		22105673	12/13/85	A
		SHEET NO. 13	60462210	PAGE JG-13

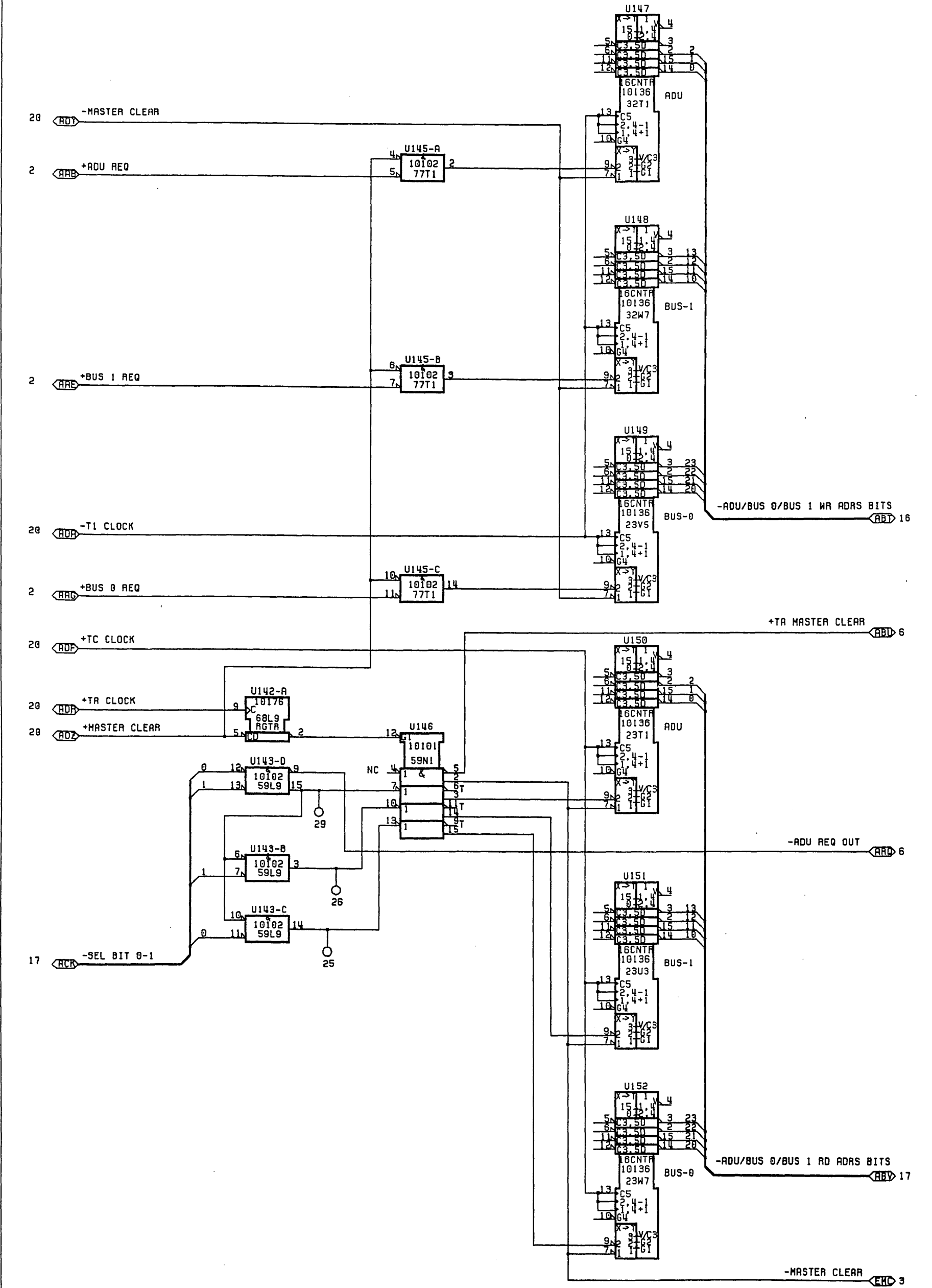
```


17  ACK -SEL BIT 0-1
10  ABK -ADU TAG BIT 0-7,P
12  ABP -BUS 1 TAG OUT 0,3-7,P
13  ABR -BUS 0 TAG OUT 0,3-7,P

```

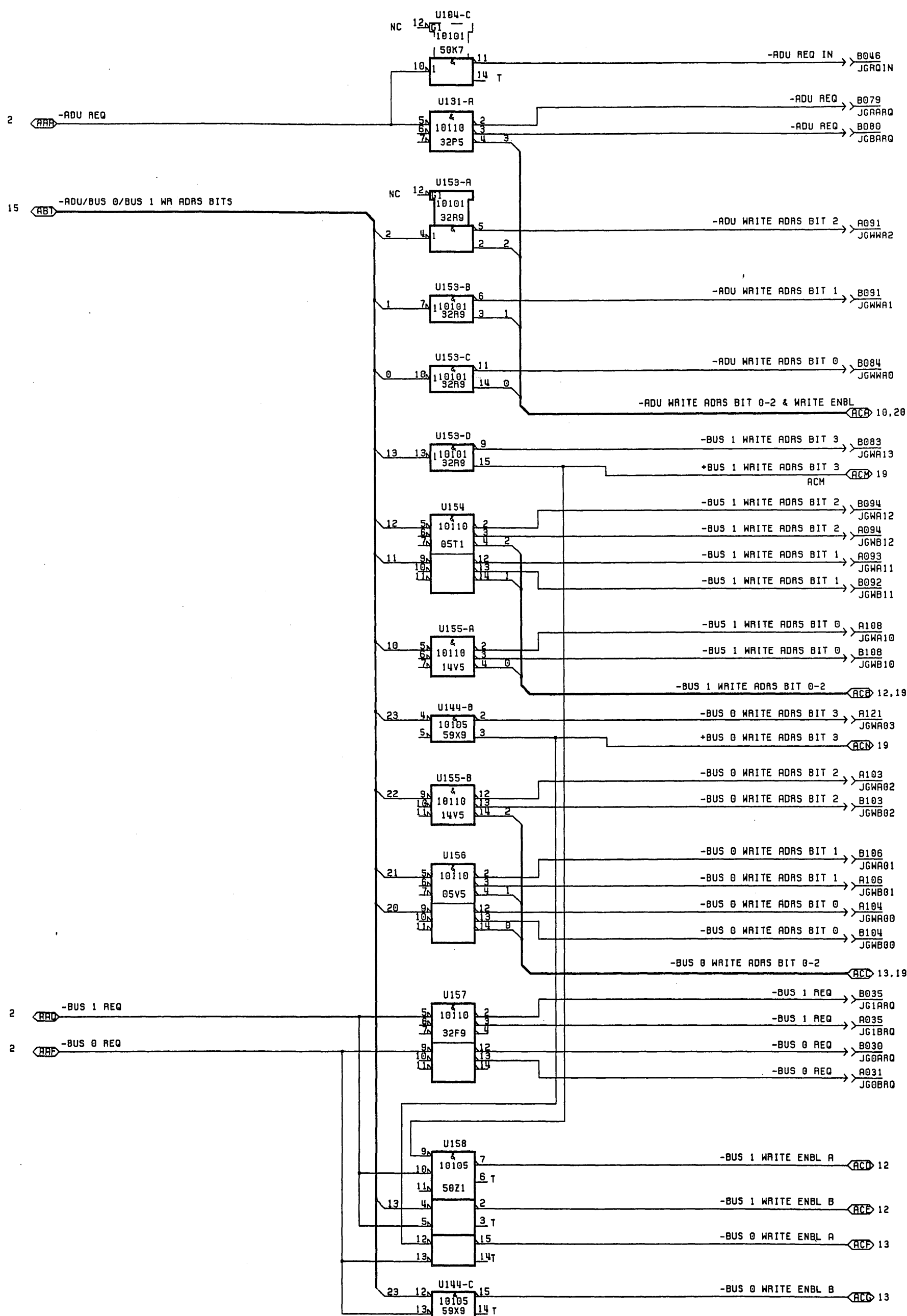



ADRS CNTRS FOR DATA OUT BUFFERS



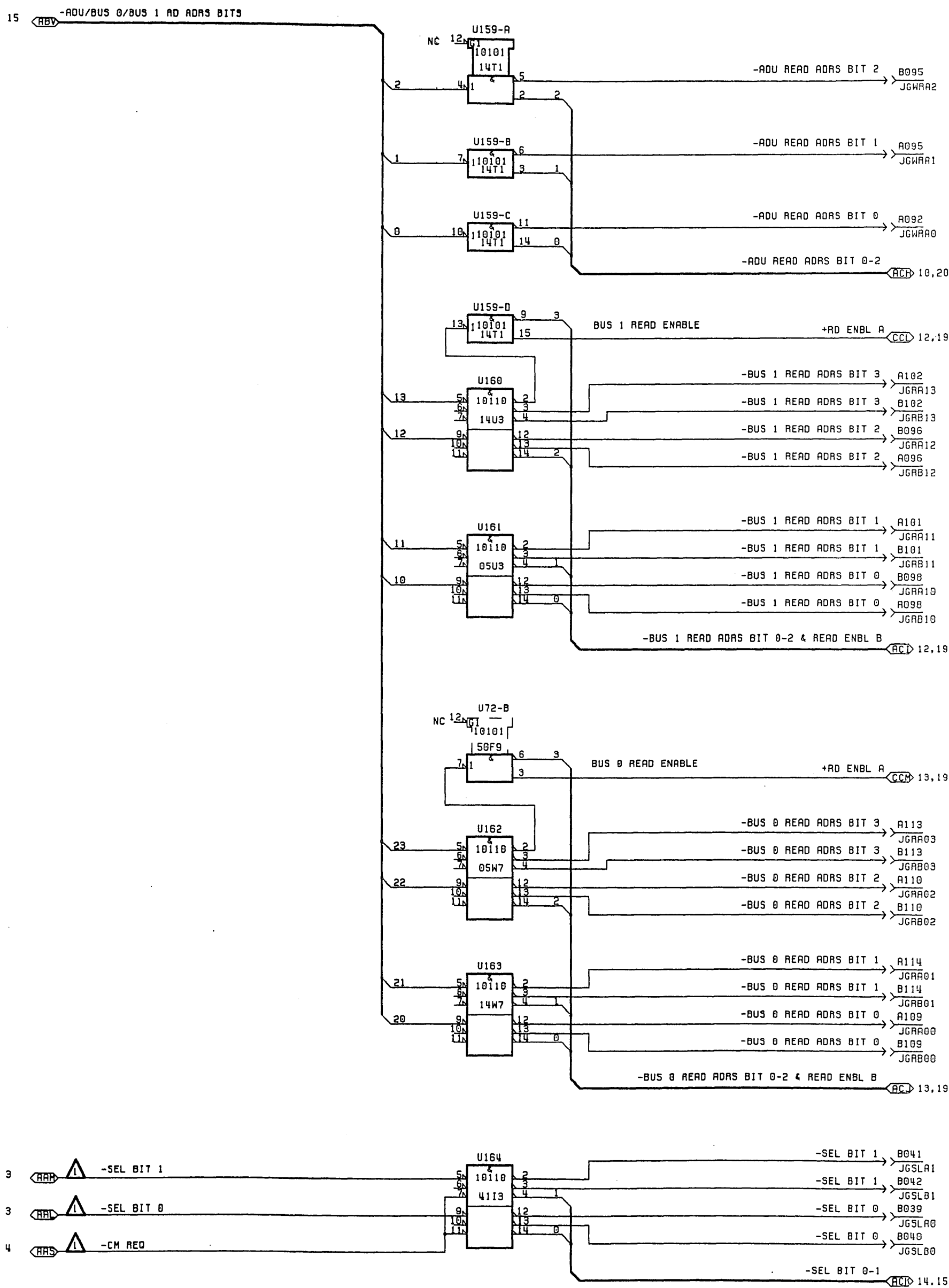
 CONTROL DATA	CMI CONTROL BOARD		B	DWG NO.	DATE	REV
	ADRS COUNTERS FOR DATA OUT BUFFER			22105673	12/13/85	A
	TYPE 1JGH			SHEET NO. 15	60462210	PAGE JG-15

WRITE ADRS & WRITE ENBL F/O'S




 CONTROL DATA	CMI CONTROL BOARD WRITE ADDRESS & WRITE ENABLE FANOUTS FOR DATA OUT BUFFERS TYPE 1JGH			B	DWG NO. 22105673		DATE 12/13/85		REV A		
				N	SHEET NO. 16		60462210		PAGE JC-16		

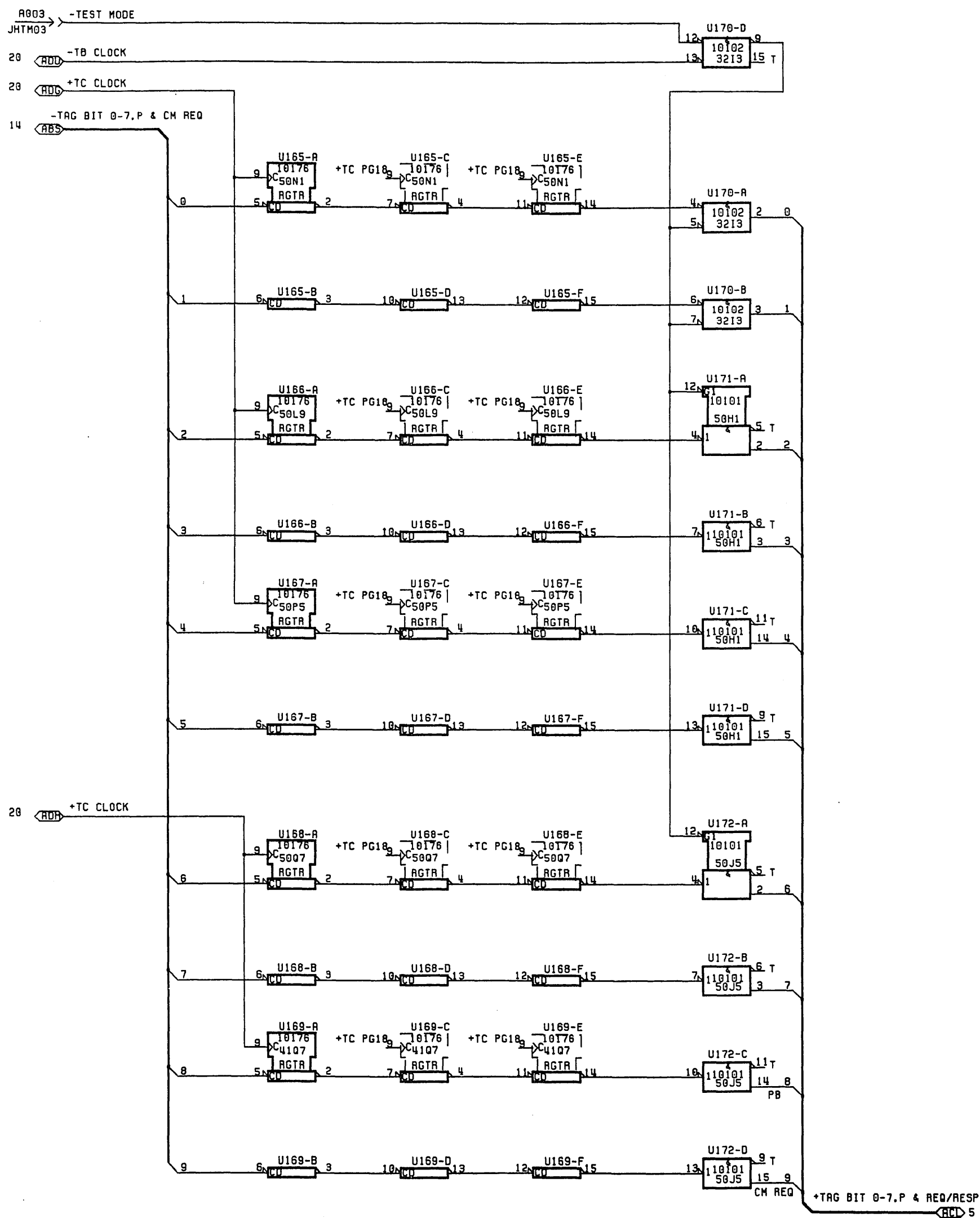
READ ADRS & READ ENBL F/O




4.5 INCH MAXIMUM LENGTH

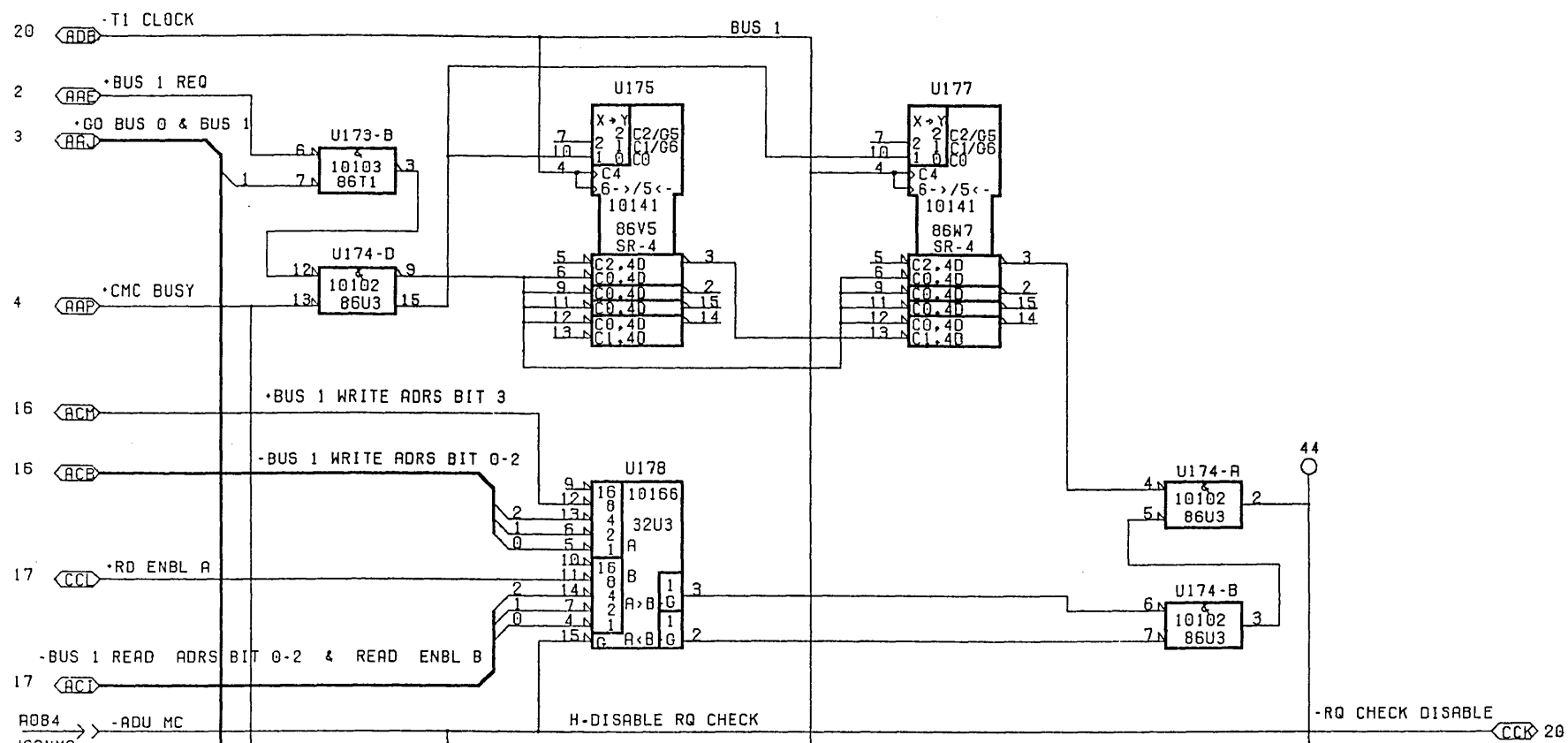
 CONTROL DATA	CMI CONTROL BOARD	B	DWG NO.	DATE	REV
	READ ADRS & READ ENABLE FANOUT		22105673	07/18/86	B
	FOR DATA OUT BUFFERS				
TYPE 1JGH	N	SHEET NO.	17	60462210	PAGE JG-17

TAG BITS 0-7, PAR AND CM REQ FOR SELF-TEST MODE

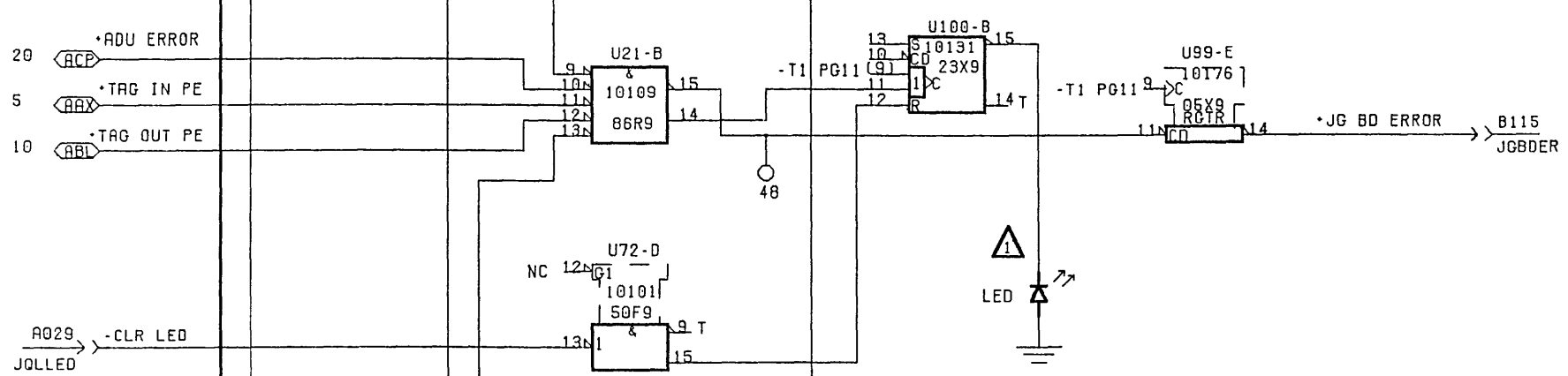


 CONTROL DATA	CMI CONTROL BOARD TAG BIT 0-7, P AND CM REQ FOR SELF TEST MODE TYPE 1JCH	B	DWG NO.	DATE	REV
			22105673	12/13/85	A
			SHEET NO. 10		

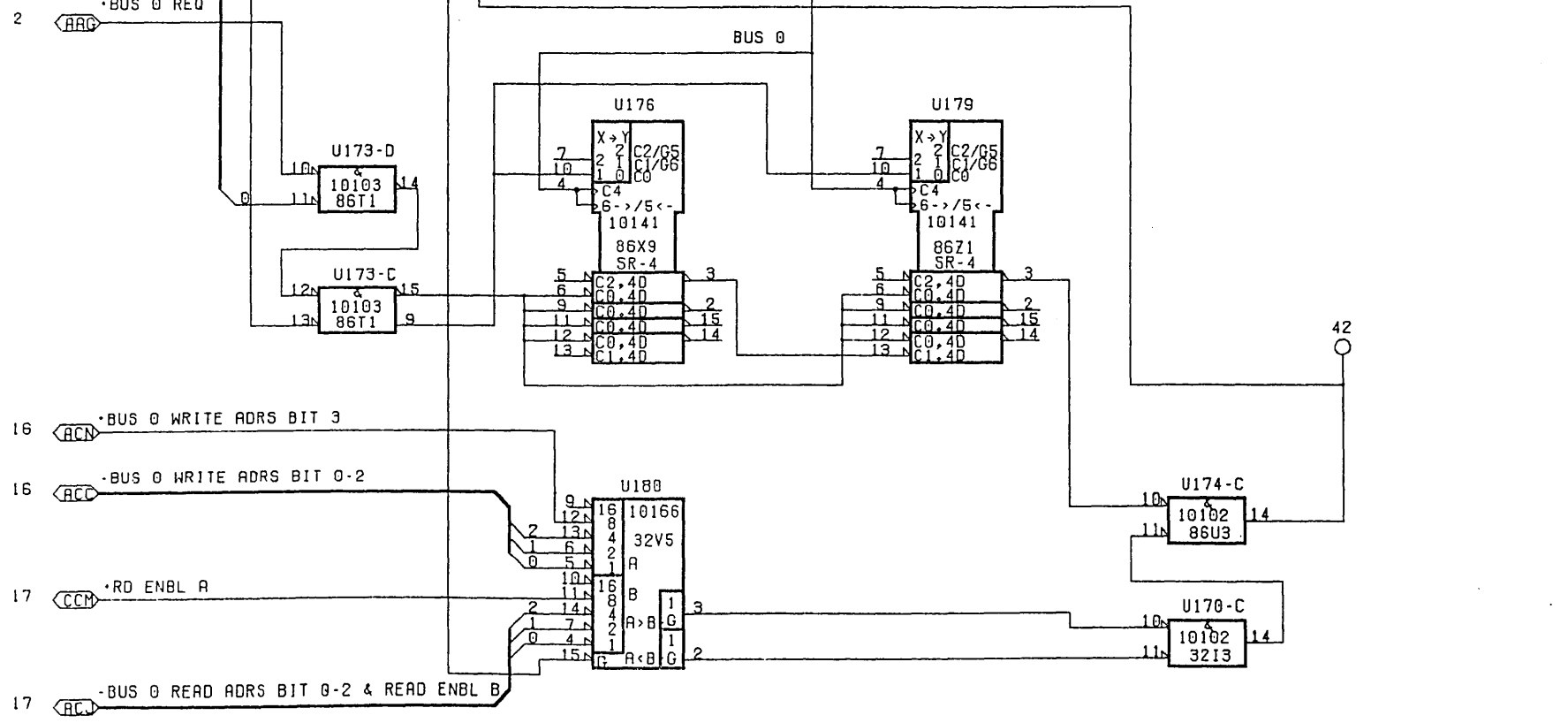
BUS 1 ERROR CHECKER




ERROR MUX



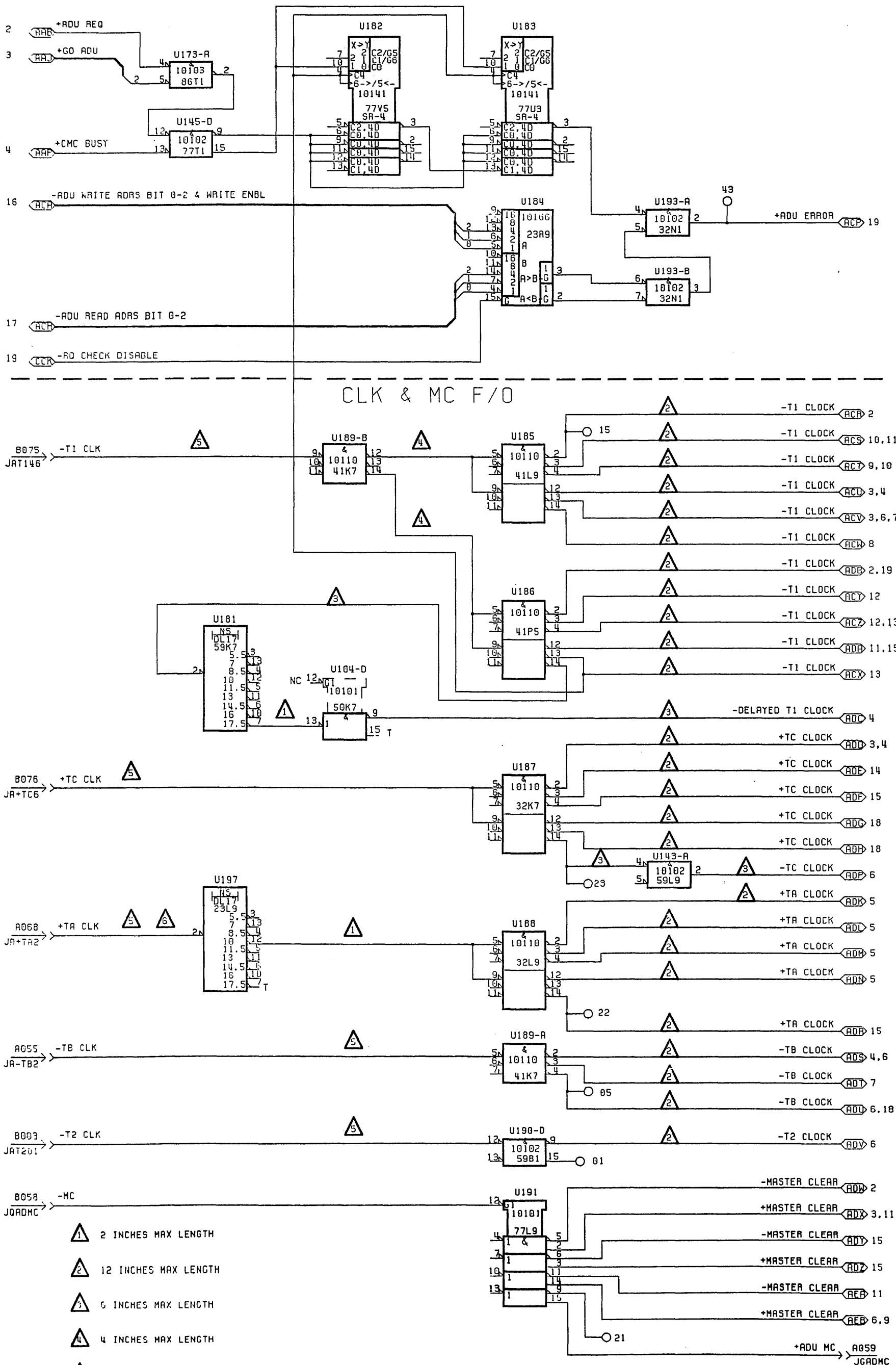
BUS 0 ERROR CHECKER




1 TERMINATE

 CONTROL DATA	CMI CONTROL BOARD BUS 0 & 1 ERROR CHECKER AND ERROR MUX TYPE 1JGH	N	B	DWG NO. 22105673	DATE 06/16/88	REV C
			SHEET NO. 19		60462210	PAGE JG-19

ADU ERROR CHECKER



 CONTROL DATA	CM1 CONTROL BOARD ADU ERROR CHECKER, CLOCK & MASTER CLEAR FANOUT TYPE 1JGH	B	DWG NO. 22105673	DATE 12/13/85	REV A
	N		SHEET NO. 20	60462210	PAGE 10-20

TESTPOINTS					
TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	20	+T2 CLOCK	27	09	-ADU IN RD ADRS B1
02	05	-RESPONSE	28	03	-PRIORIYT F/F B
03	08	-BUS RESPONSE	29	15	+ADU RQ OUT
04	09	-TAG IN BIT 4	30	09	-ADU IN RD ADRS B0
05	20	-TB CLOCK	31	03	-BUS 0 GO
06	08	-TAG IN BIT 7	32	02	-BUS 0 CM REQUEST
07	09	-TAG IN BIT 6	33		
08	04	-RESYNC BUFFER FULL	34	03	-ADU GO
09	03	-PRIORITY F/F A	35	09	-TAG IN BIT 5
10	08	-RESPONSE (RESYNC)	36	02	-BUS 0 CM RQ CNT=0
11	04	-RESYNC 0 F/F	37		
12	04	-RESYNC 1 F/F	38	02	-ADU CM REQUEST
13	04	-RESYNC 2 F/F	39	02	-BUS 1 CM RQ CNT=0
14	04	-RESYNC 3 F/F	40	03	-BUS 1 GO
15	20	-T1 CLOCK	41	02	-BUS 1 CM REQUEST
16	02	-ADU CM RQ COUNT=0	42	19	+BUS 0 RQ ERROR
17	05	+TAG IN P.E.	43	20	+ADU RQ ERROR
18	04	-CM REQUEST(RESYNC)	44	19	+BUS 1 RQ ERROR
19	06	-ADU IN WRT ADRS B1	45	04	+CMC BUSY
20	06	-ADU IN WRT ADRS B0	46	11	-CHANNEL 4 GO
21	20	-MASTER CLEAR	47	10	-TAG OUT P.E.
22	20	+TA CLOCK	48	19	+BOARD ERROR
23	20	+TC CLOCK	49	11	-CHANNEL 0 GO
24	11	-CHANNEL 3 GO	50	11	-CHANNEL 1 GO
25	15	+BUS 0 RQ OUT	51	11	-CHANNEL 2 GO
26	15	+BUS 1 RQ OUT			

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	A061,B061,A070,B070 [NOT USED]
TERM	NONE
UNUSED	A037,B037,B093,A099,B099,A100,B100,A105,B105,A111,B111,A112,B112,A127,B127,A128,B128

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

CMI DATA BOARD

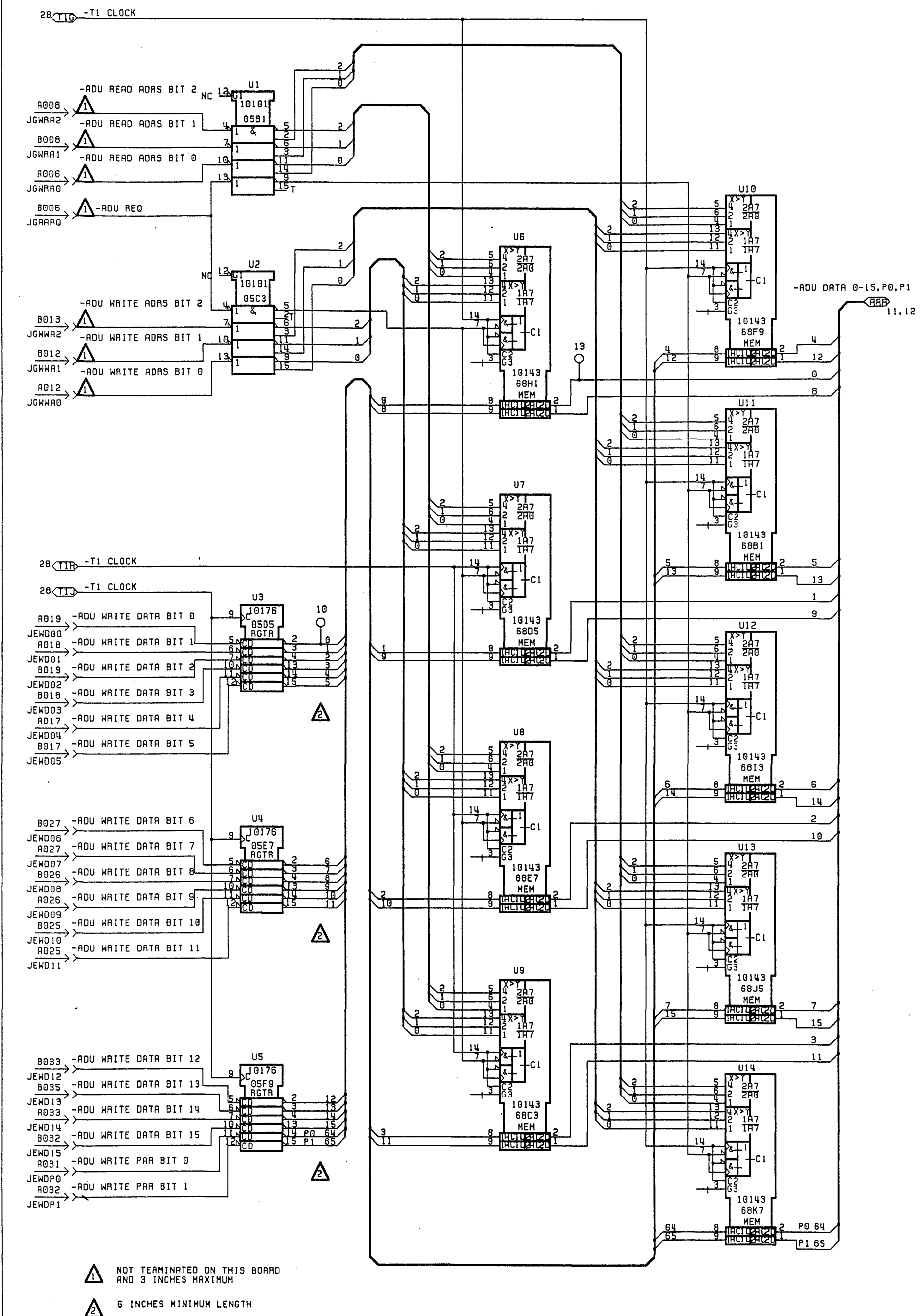
[illegible]

LOC: A02, A03, A04, A05

DWN	L H JOHNSON	11/01/85
CHKD	D R FORD	12/04/85
ENG	J P STROMBECK	12/04/85
PUBS	R K BONDE	12/04/85
APP	J P STROMBECK	12/04/85

 CONTROL DATA	REVISION HISTORY	B	DWG NO. 53575507	DATE 09/19/86	REV C
	TYPE 1JHH	SHEET NO. 1	60462210	PAGE	JH-01

WRITE BUFFER ADU DATA BITS 0-15, PAR 0,1

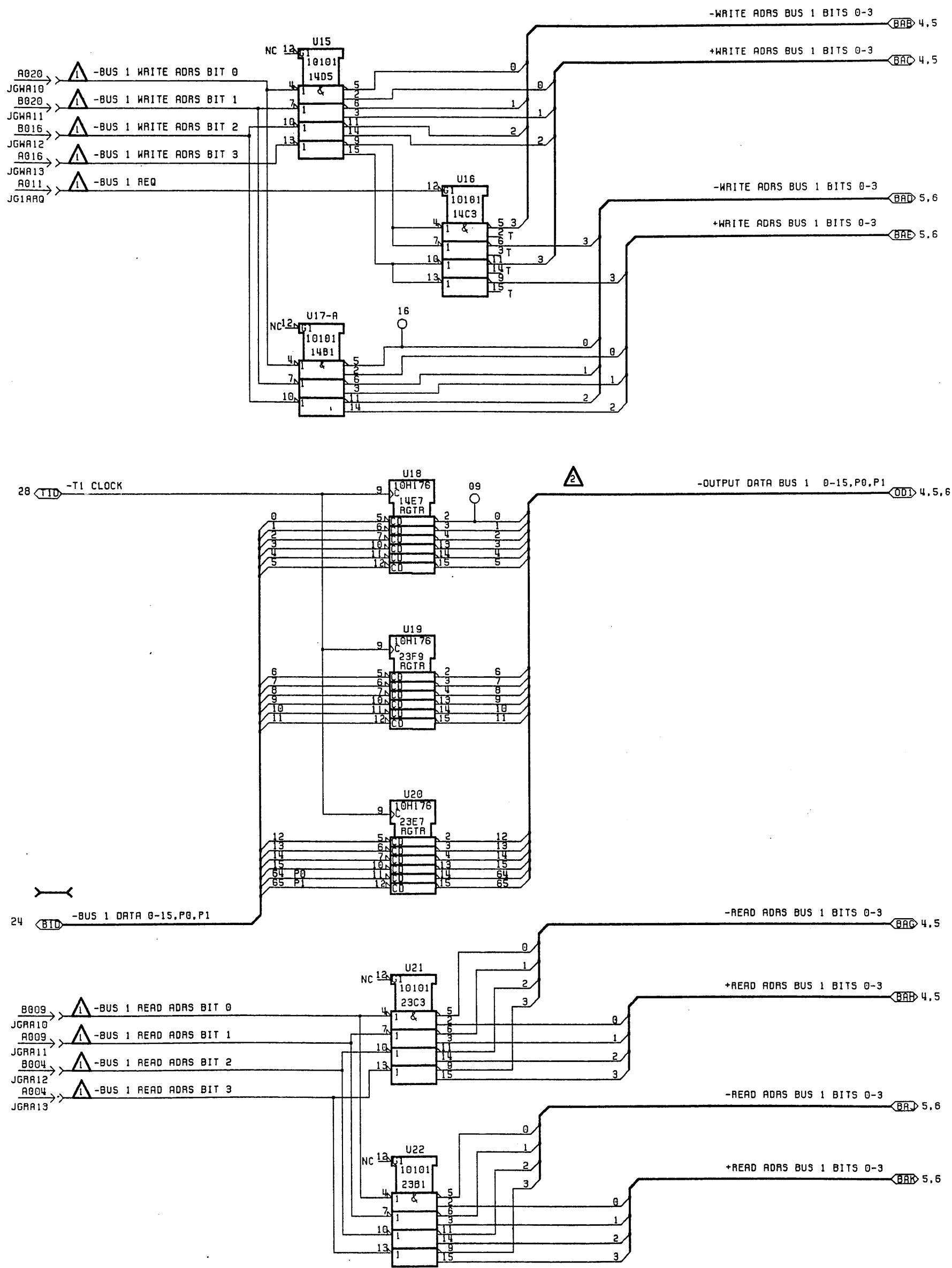


1 NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

2 6 INCHES MINIMUM LENGTH

CMI DATA BOARD WRITE BUFFER ADU DATA BITS 0-15, PAR 0,1 TYPE 1JHH	B	DWG NO.	DATE	REV
		53575507	11/01/85	A
		SHEET NO. 2	60462210	PAGE JH-02

CMI BUS 1 ADRS AND DATA OUT BUFFER

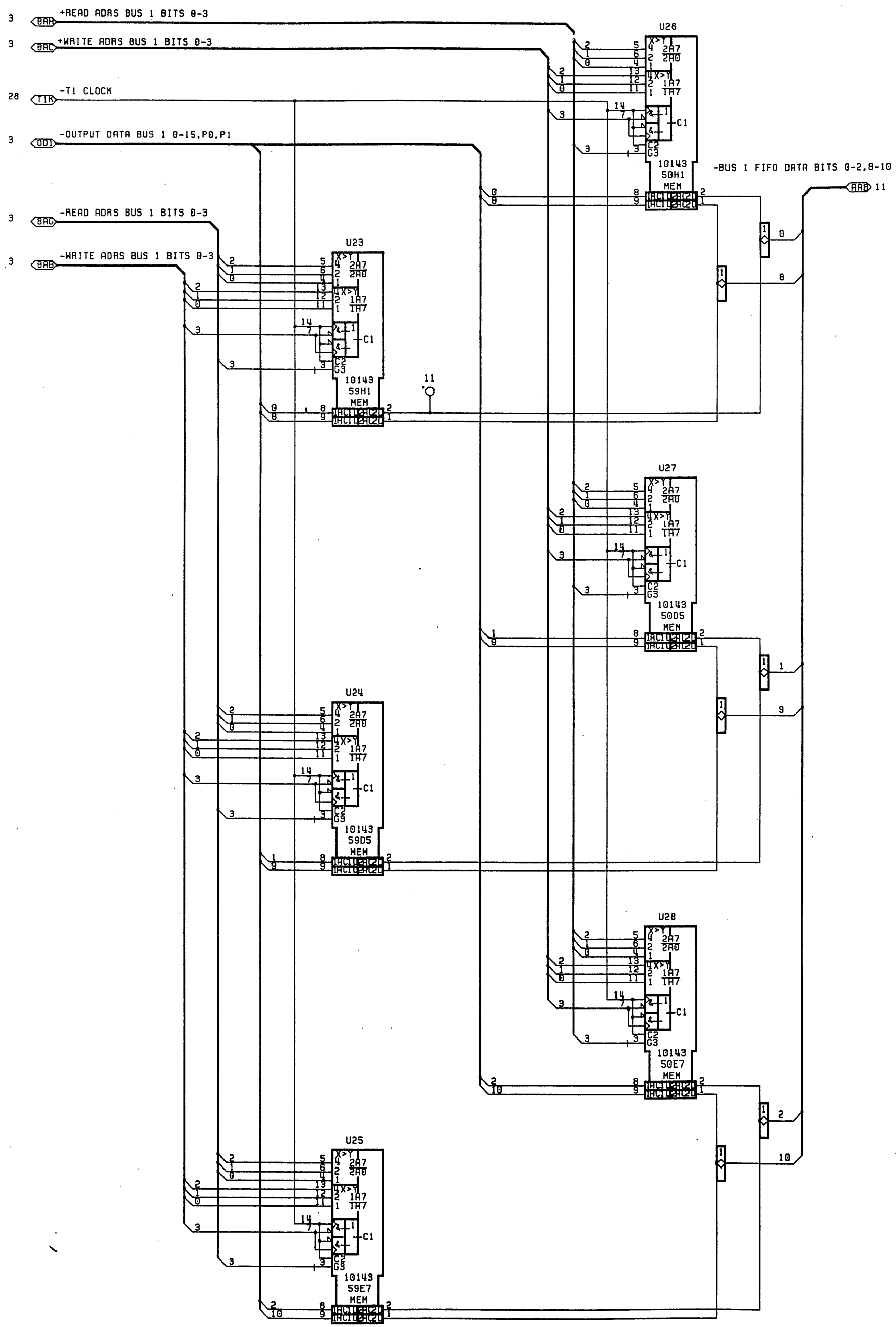


1 NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

2 6 INCHES MINIMUM LENGTH

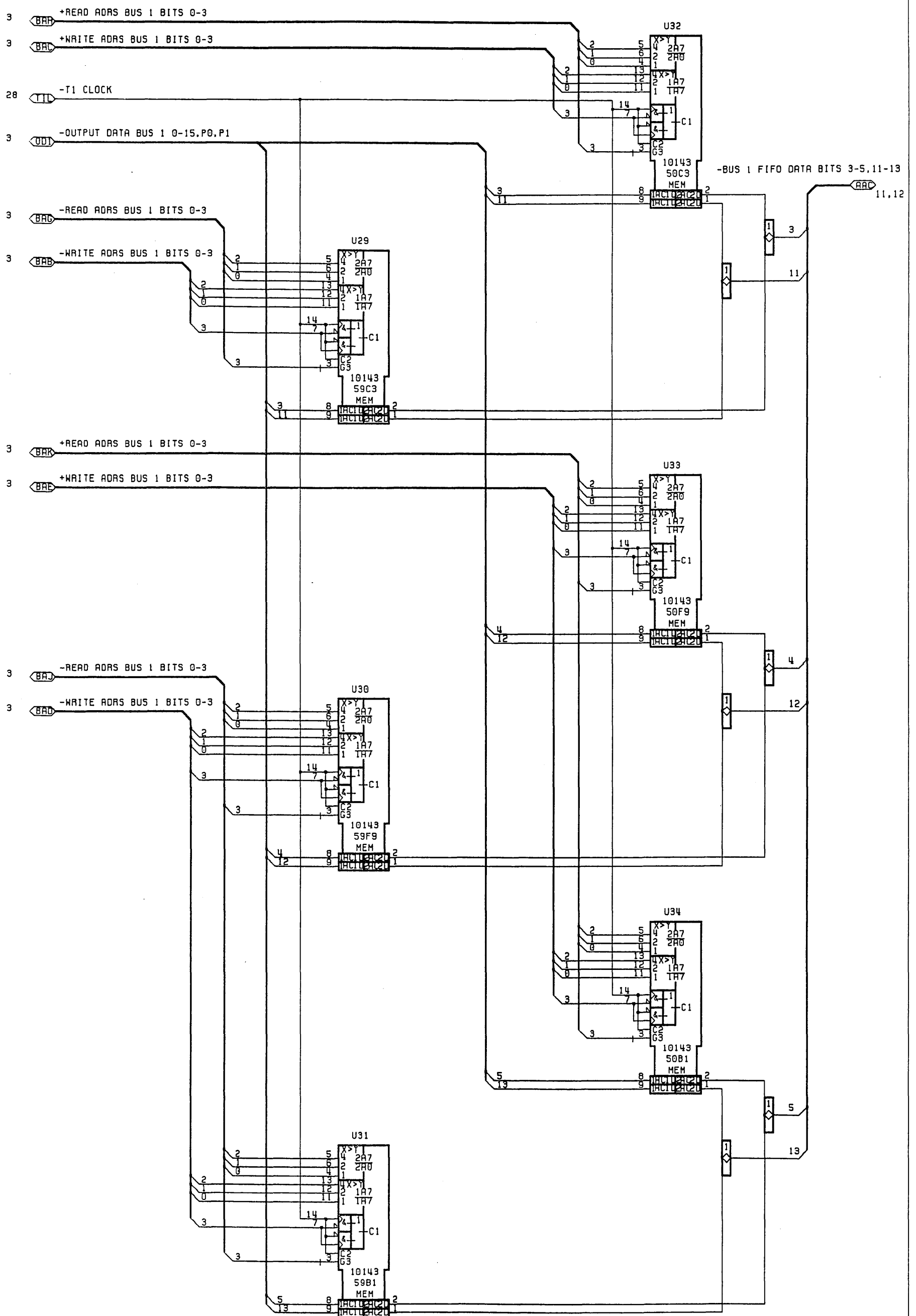
GD CONTROL DATA	CMI DATA BOARD CMI BUS 1 ADDR AND DATA OUTPUT BUFFER TYPE 1JHH	B	DWG NO. 53575507	DATE 11/01/85	REV A
			SHEET NO. 3	60462210	PAGE JH-03


CMI FIFO BUS 1 BITS 0-2, 8-10 OUT BUFFER



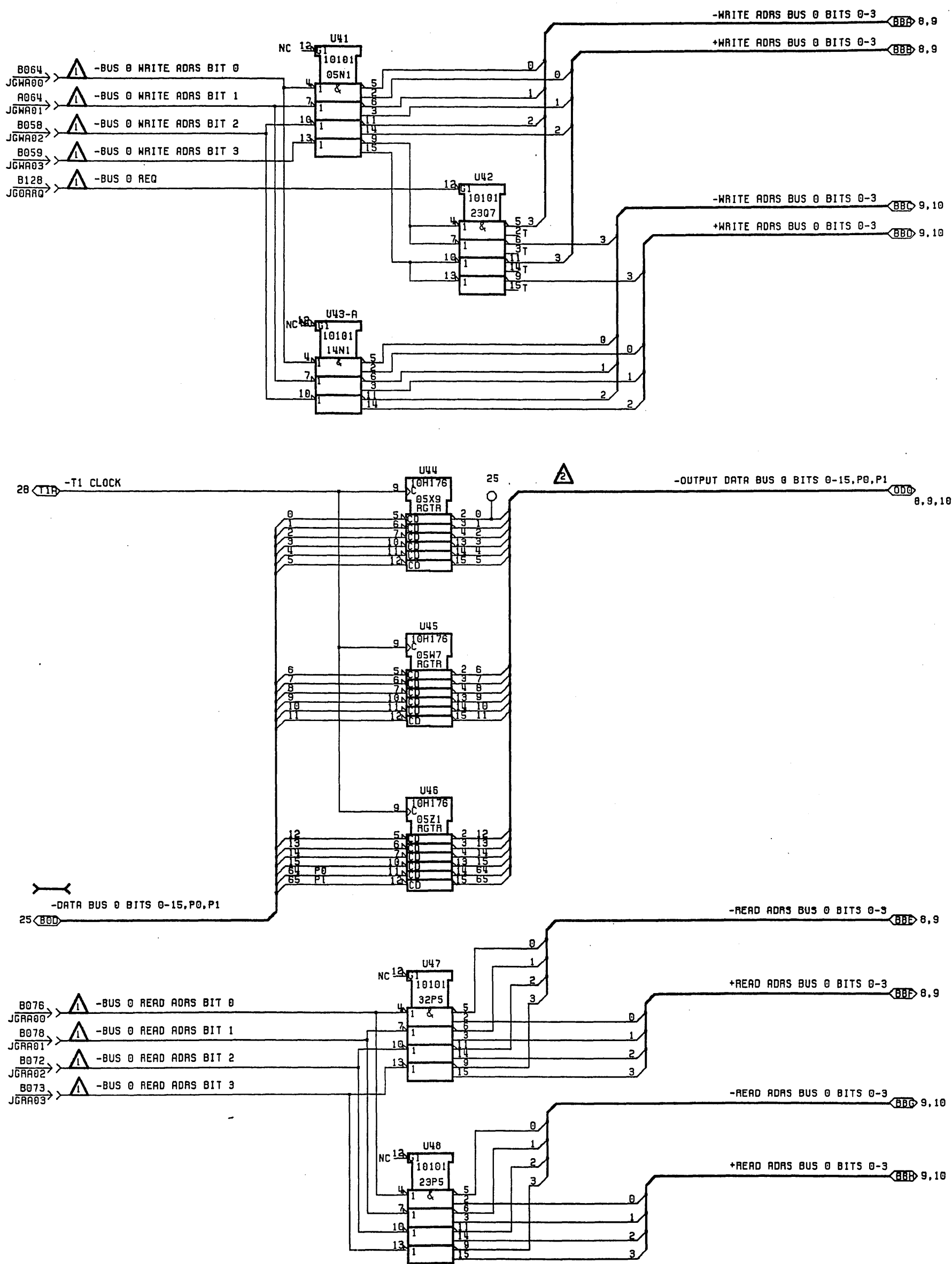
 CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 1 0-2. 8-10 OUTPUT BUFFER TYPE 1JHH		8	DWG NO. 53575507	DATE 11/01/85	REV A	
				SHEET NO. 4	60462210	PAGE	JH-04

CMI FIFO BUS 1 BITS 3-5, 11-13 OUT BUFFER



 CONTROL DATA	CMI DATA BOARD	B	DWG NO.	DATE	REV
	CMI FIFO BUS 1 BITS 3-5,		53575507	11/01/85	A
	11-13 OUTPUT BUFFER				
TYPE 1JHM	N	SHEET NO. 5	60462210	PAGE	4H-05

CMI BUS 0 ADRS AND DATA OUT BUFFER

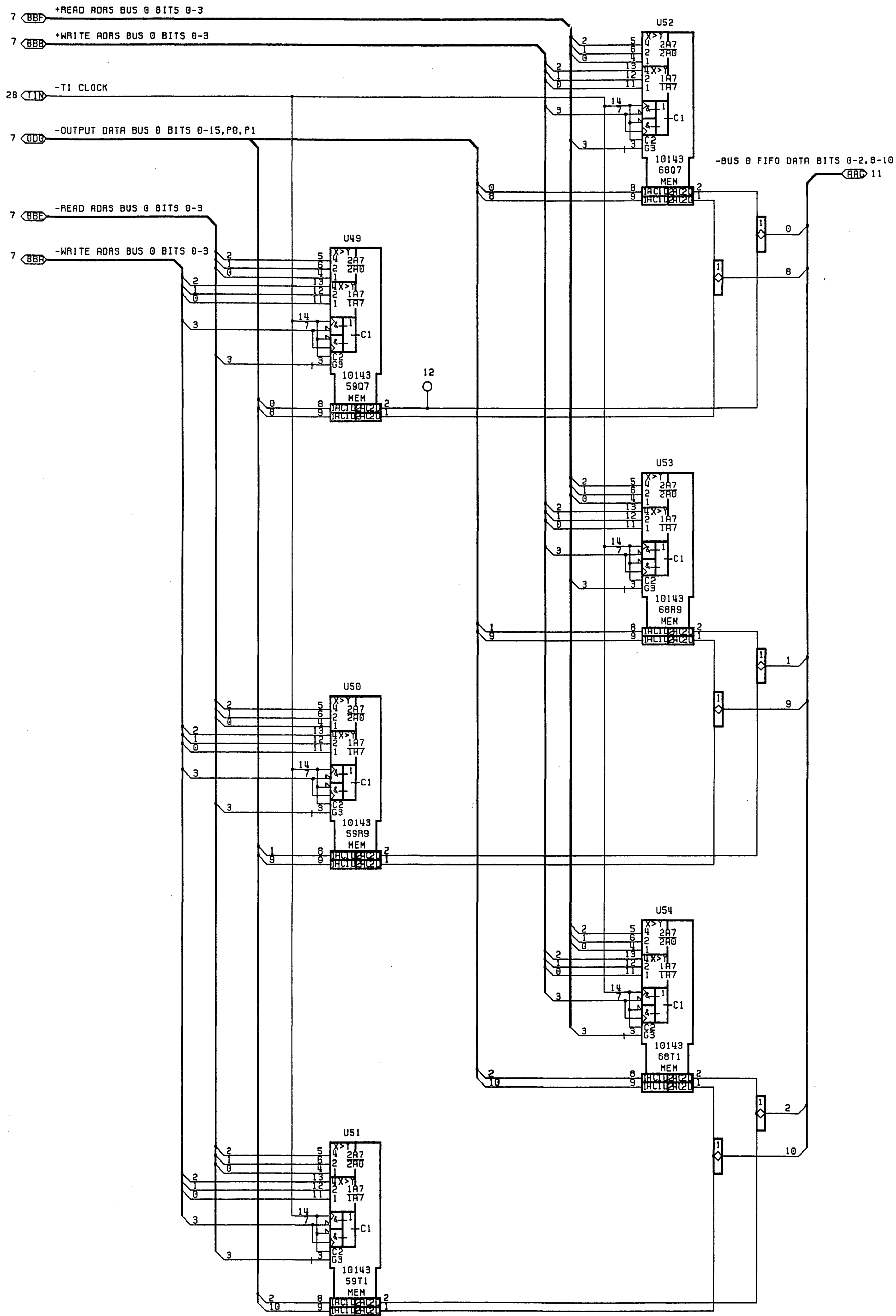



1 NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

2 6 INCHES MINIMUM LENGTH

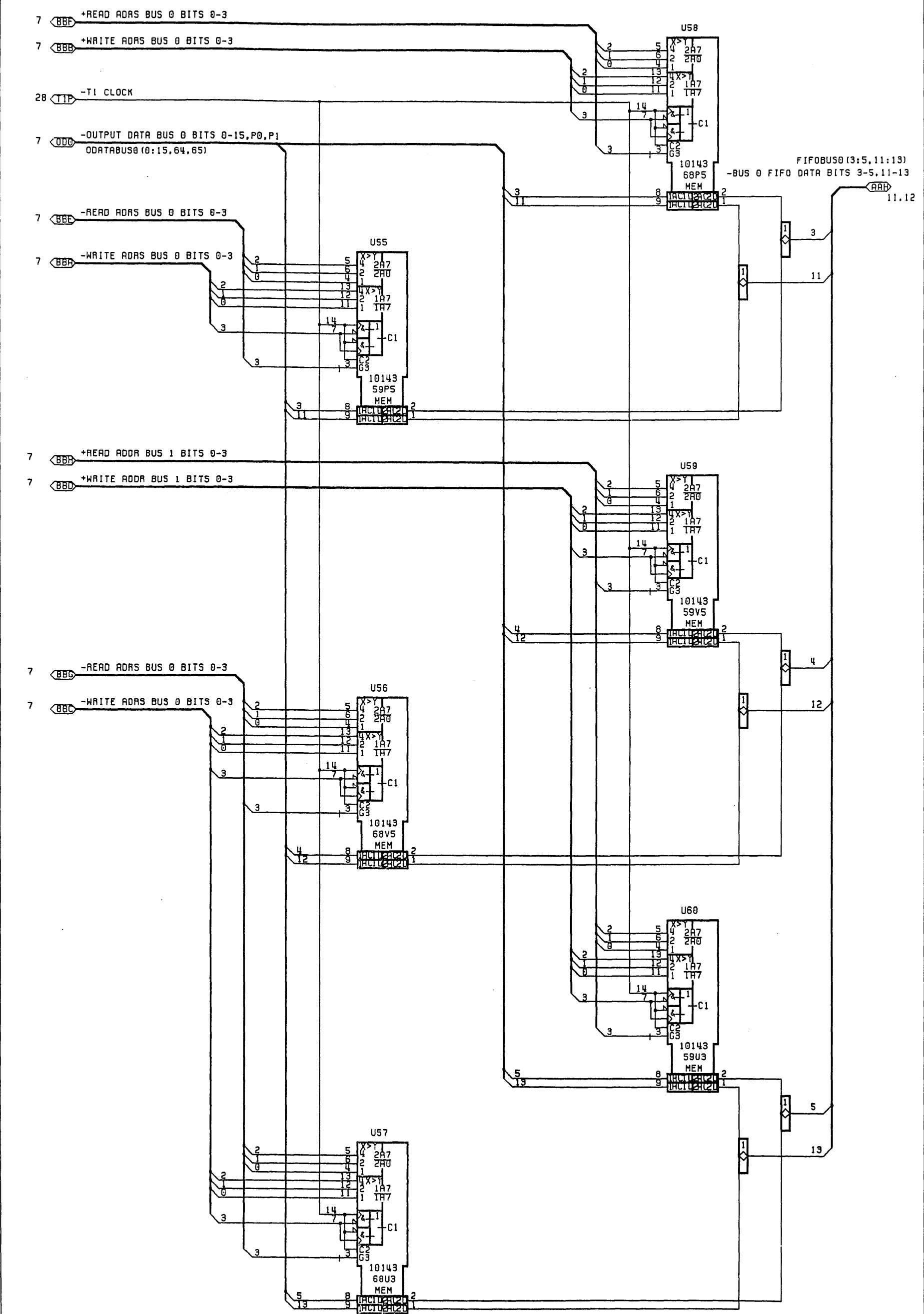
CONTROL DATA	CMI DATA BOARD CMI BUS 0 ADDRESS AND DATA OUTPUT BUFFER TYPE 1JMH		DWG NO. 8 53575507	DATE 08/18/88	REV 0
	SHEET NO. 7		60462210	PAGE	JH-07


CMI FIFO BUS 0 BITS 0-2, 8-10 OUT BUFFER



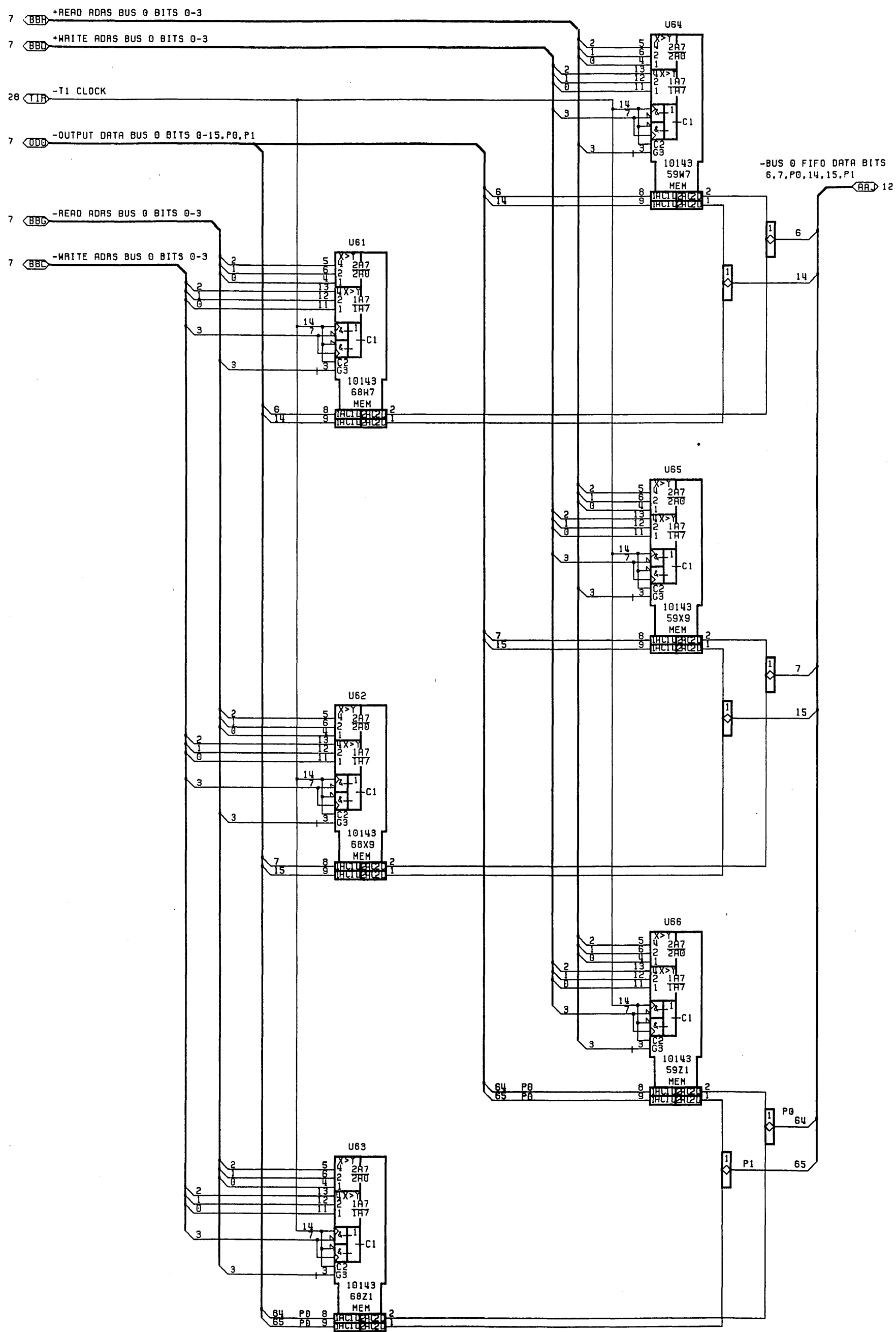
 CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 8 BITS 0-2, 8-10 OUTPUT BUFFER TYPE 1JHH	B	DWG NO.	DATE	REV
			53575507	11/01/85	A
N		SHEET NO.	8	60462210	PAGE
				JH-08	

CMI FIFO BUS 0 BITS 3-5, 11-13 OUT BUFFER



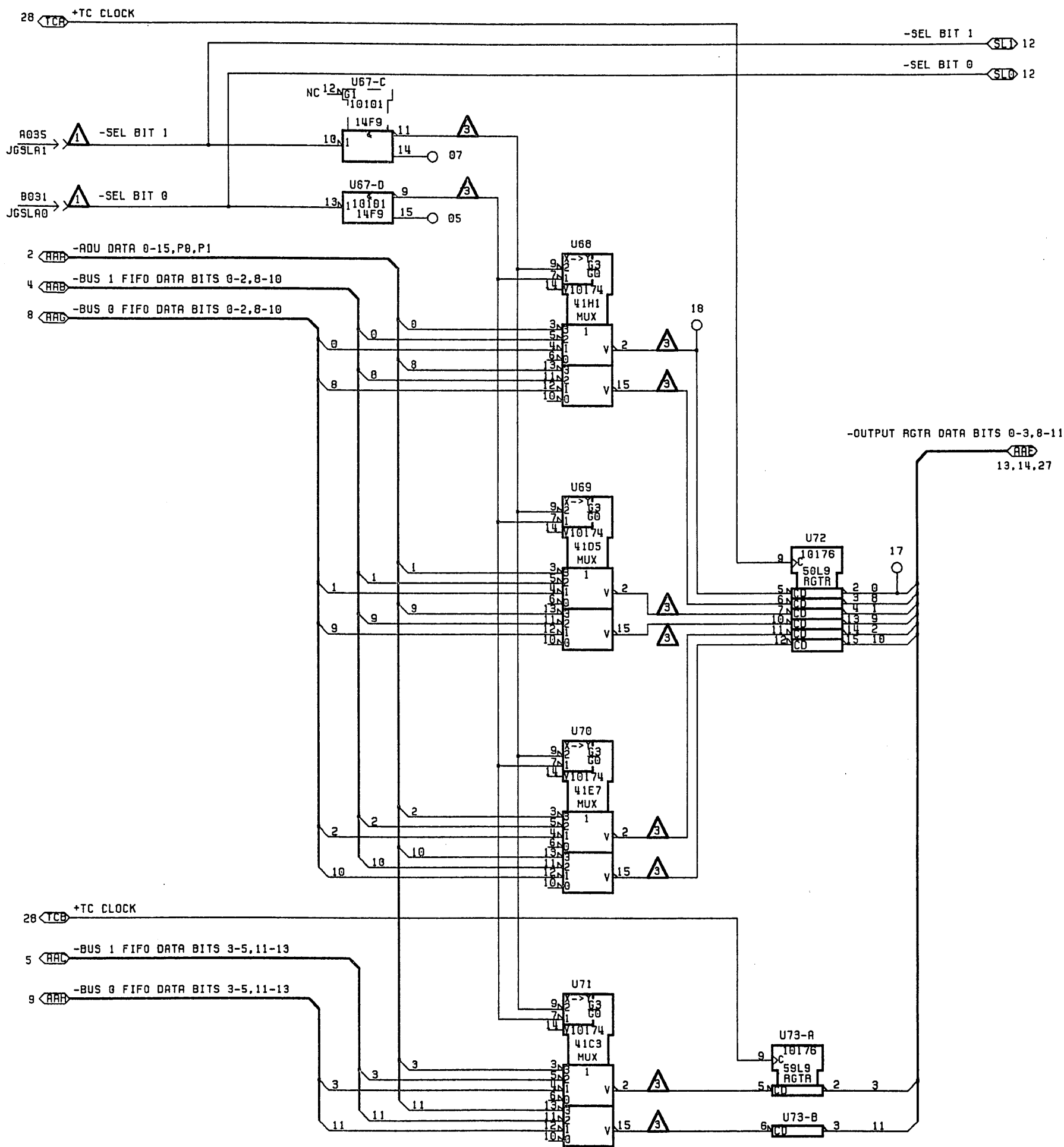
 CONTROL DATA	CMI DATA BOARD		B	DWG NO.	DATE	REV
	CMI FIFO BUS 0 BITS 3-5.			53575507	11/01/85	A
	11-13 OUTPUT BUFFER					
	TYPE 1JHM					
				SHEET NO. 9	60462210	PAGE JH-09

CMI FIFO BUS 0 BITS 6,7,PAR 0, 14,15,PAR 1 OUT BUFFER



GD CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 0 BITS 6,7,P0, 14,15,P1 OUTPUT BUFFER TYPE 1JMH		DWG NO. B 53575507	DATE 11/01/85	REV A
	SHEET NO. 10		60462210	PAGE	JH-10

CMI OUT DATA MUX AND OUT RGTR BITS 0-3, 8-11

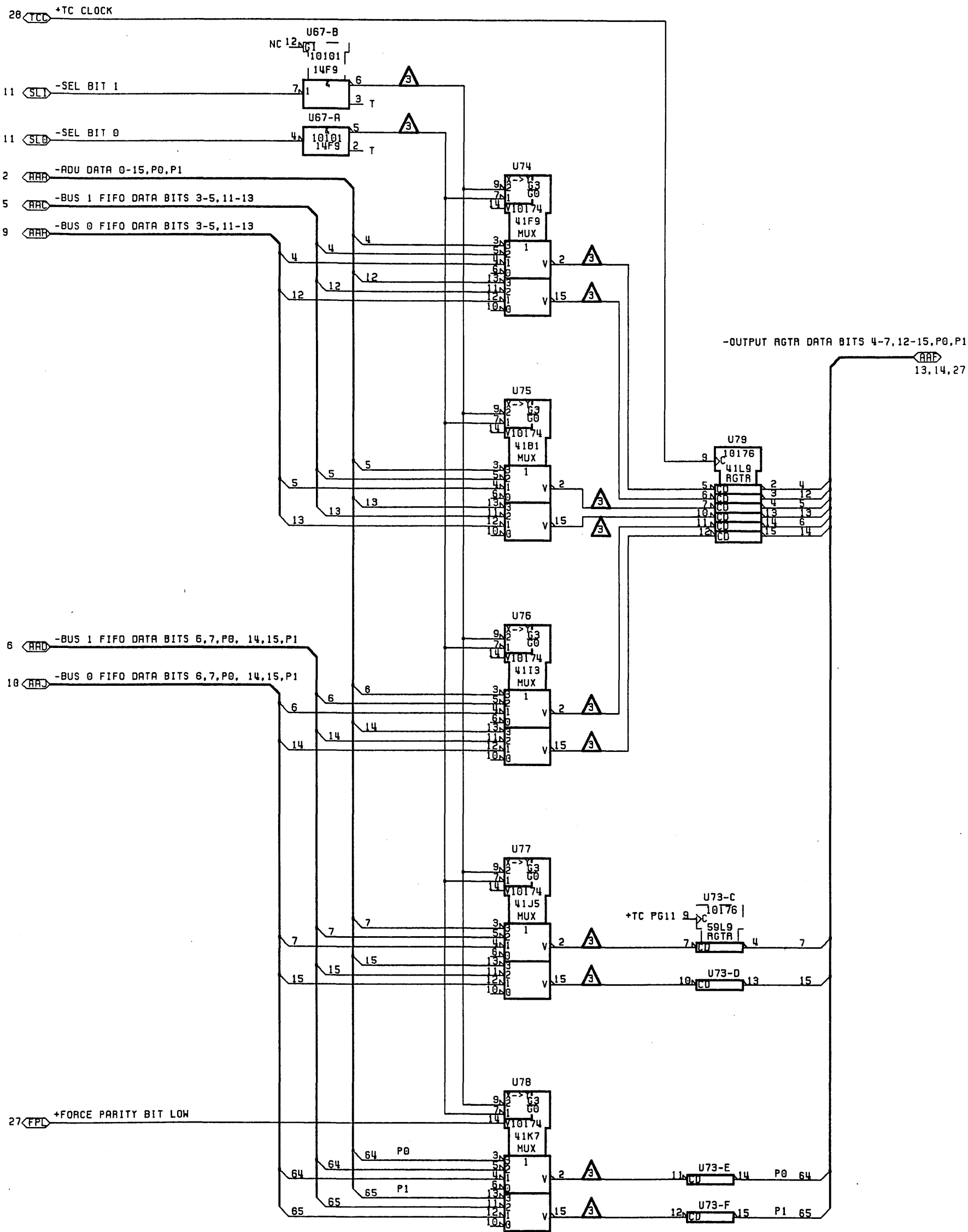


NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

6 INCHES MAXIMUM

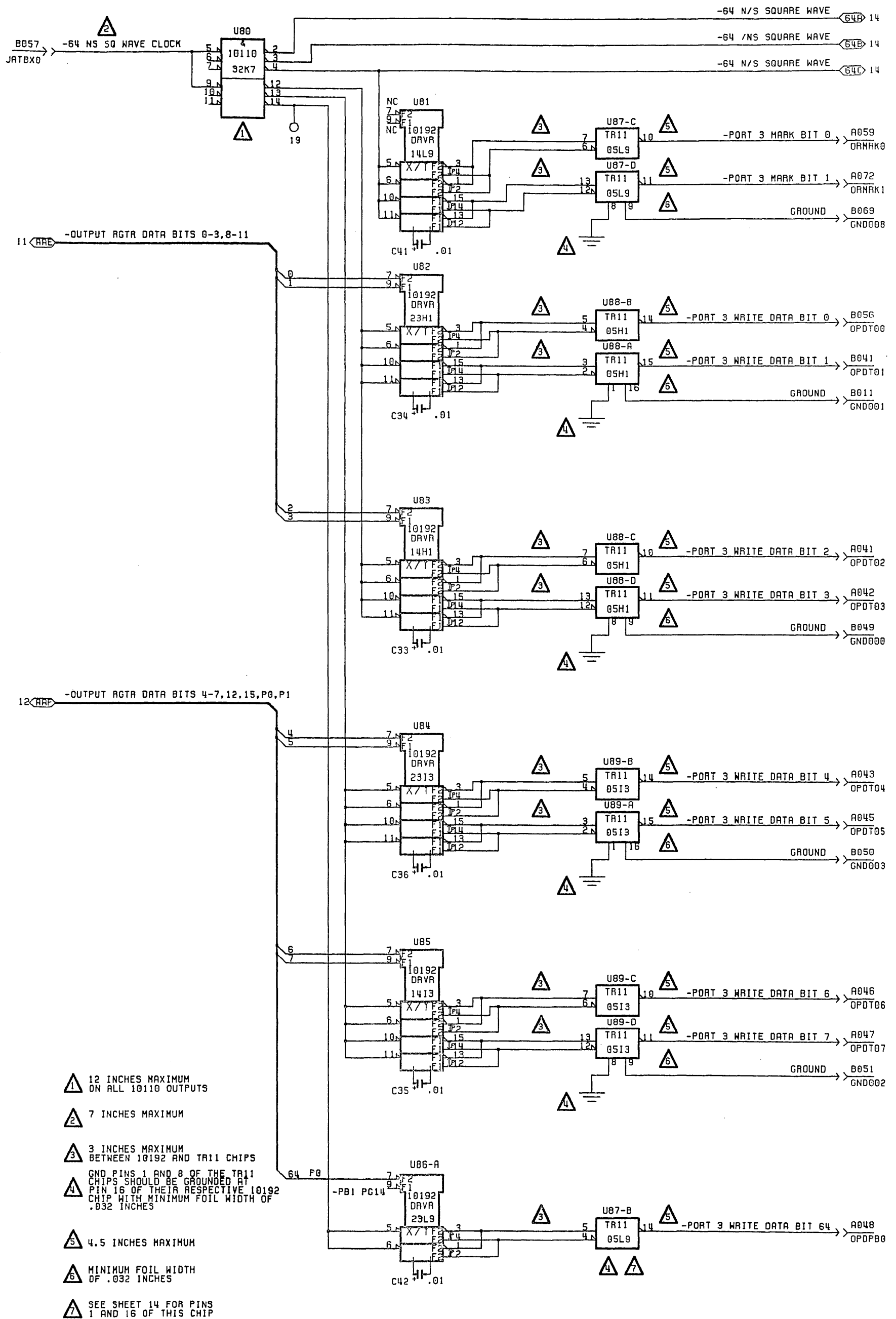
CD CONTROL DATA	CMI DATA BOARD CMI OUTPUT DATA MUX AND OUTPUT REGISTER BITS 0-3, 8-11 TYPE 1JHH		DWG NO. 8 53575507	DATE 11/01/85	REV A
	SHEET NO. 11		60462210	PAGE	JH-11

CMI OUT DATA MUX AND OUT RGTR BITS 4-7,12-15,PAR 0,1



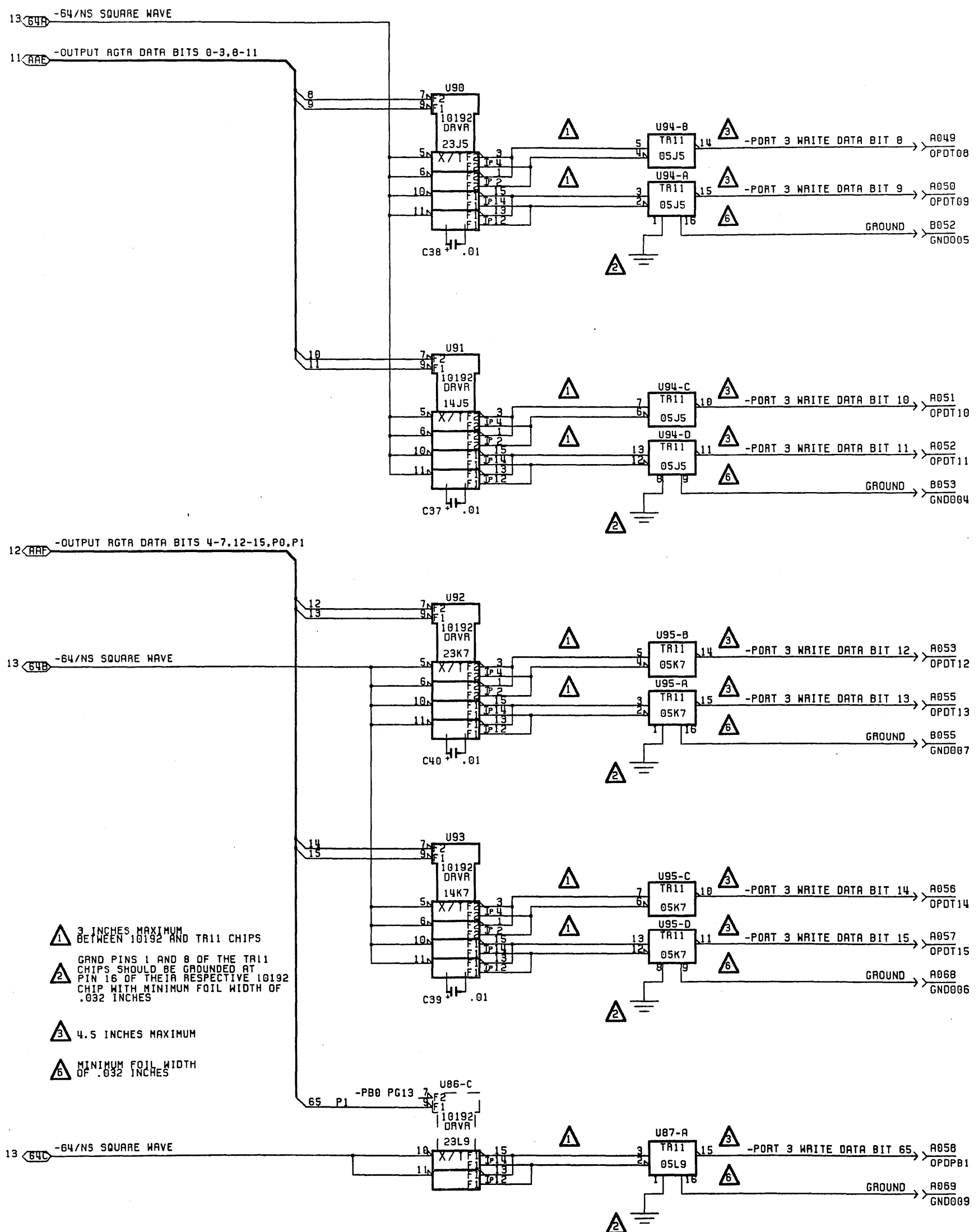
CMI DATA BOARD CMI OUTPUT DATA MUX AND OUTPUT REGISTER BITS 4-7,12-15,P0,P1 TYPE 1JHH	B	DWG NO.	DATE	REV
		53575507	11/01/85	A
		SHEET NO. 12	60462210	PAGE JH-12


DATA TRANSMITTERS BITS 0-7 & PAR 0



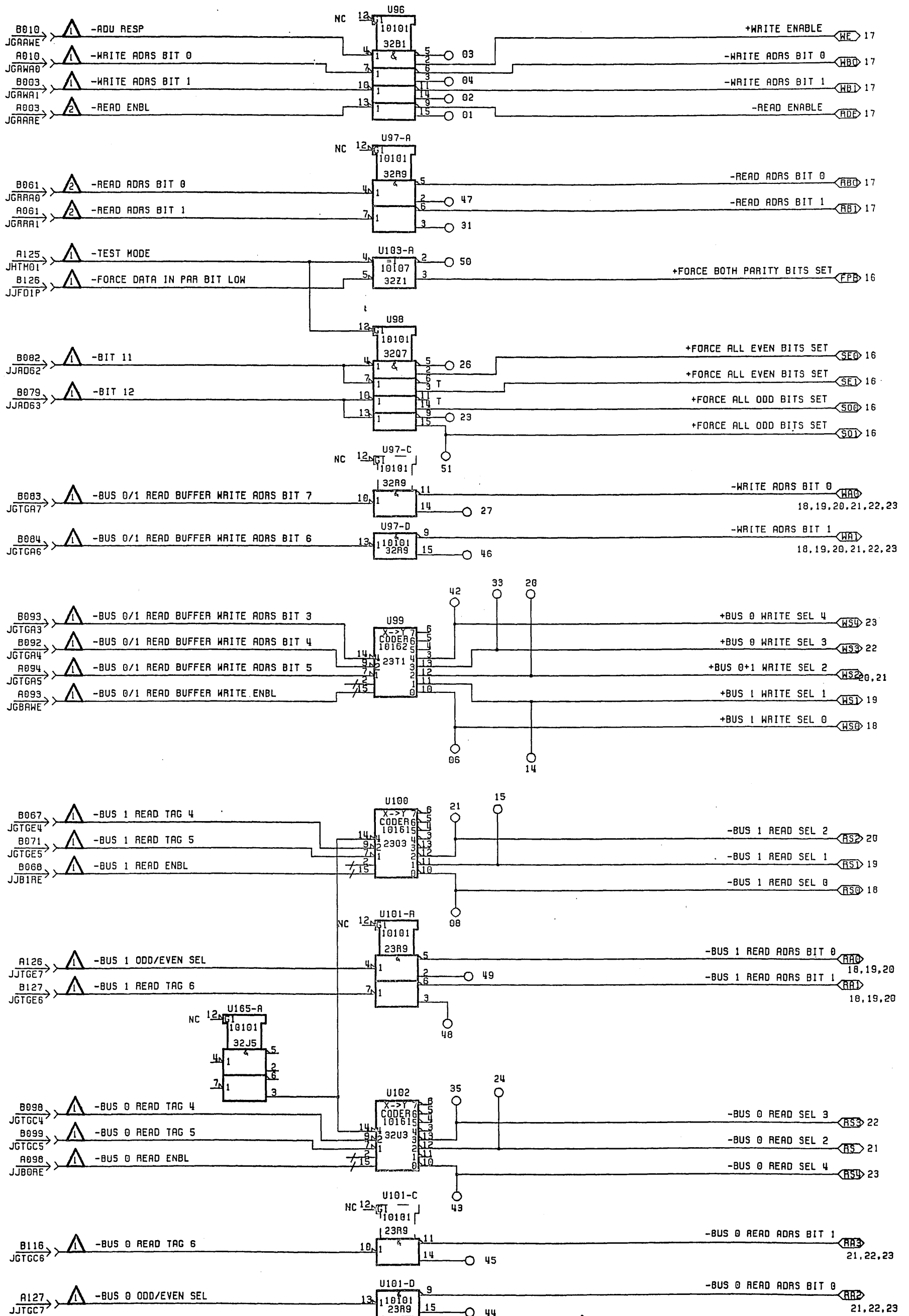
	CMI DATA BOARD		DWG NO.	DATE	REV
	DATA TRANSMITTERS TO CM		B	53575507	09/19/86
TYPE 1JHH		SHEET NO.	13	60462210	PAGE
		JH-13			

DATA TRANSMITTERS BITS 8-15 & PAR 1



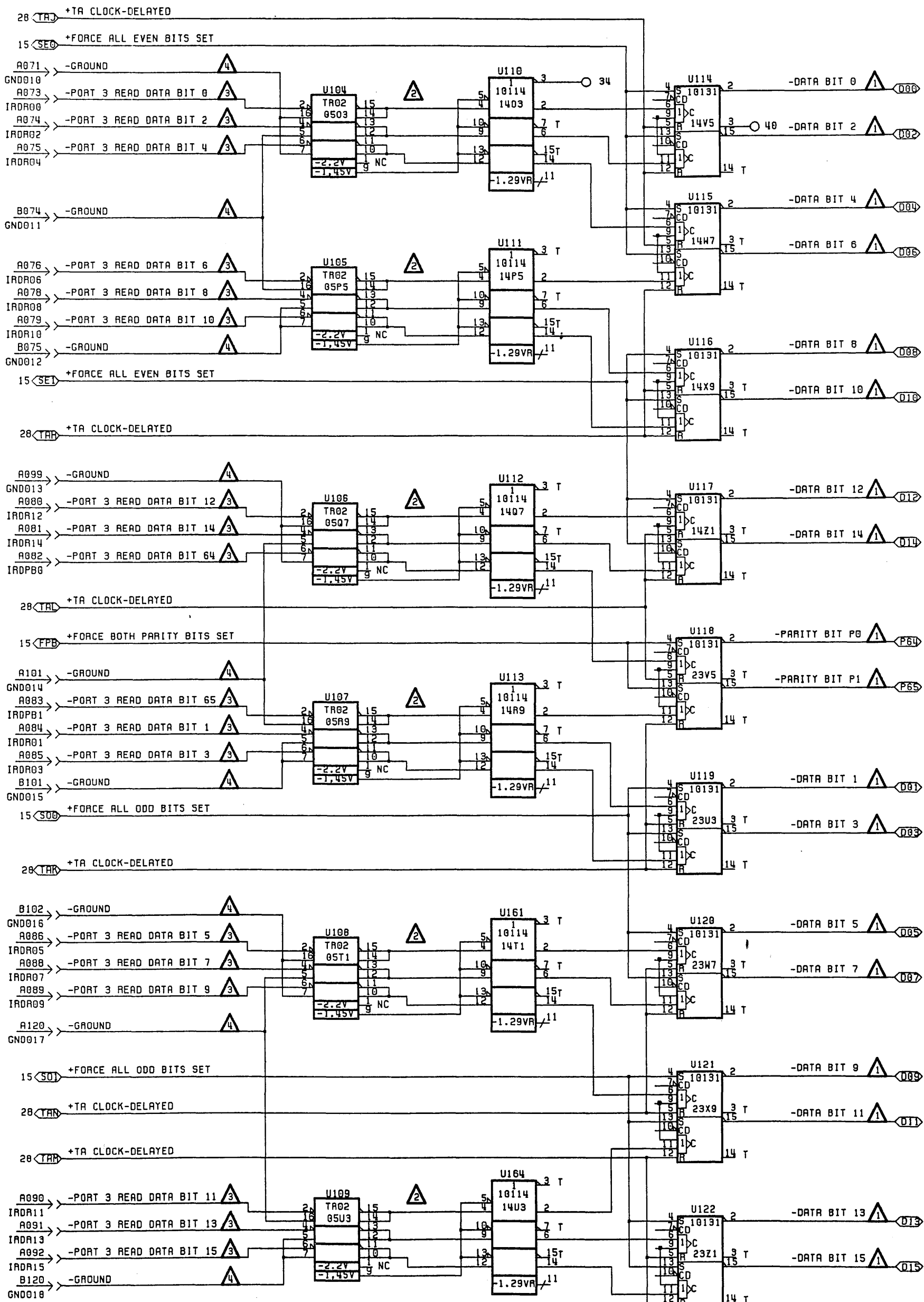
 CONTROL DATA	CMI DATA BOARD DATA TRANSMITTERS TO CM BITS 8-15 & P1 TYPE 1JHH	B	DWG NO.	DATE	REV
			53575507	11/01/85	A
			SHEET NO. 14		

CMI INPUT BUFFER ADRS DECODER AND F/O



CD CONTROL DATA	CMI DATA BOARD CMI INPUT BUFFER ADDRESS DECODE AND FANOUT TYPE 1JHM		B	DWG NO. 53575507	DATE 06/10/88	REV B
	SHEET NO.	15	60462210	PAGE	JH-15	

CMI READ DATA RECEIVERS AND F/O



1 ALL OUTPUTS FEED PAGES
17, 18, 19, 20, 21, 22, 23

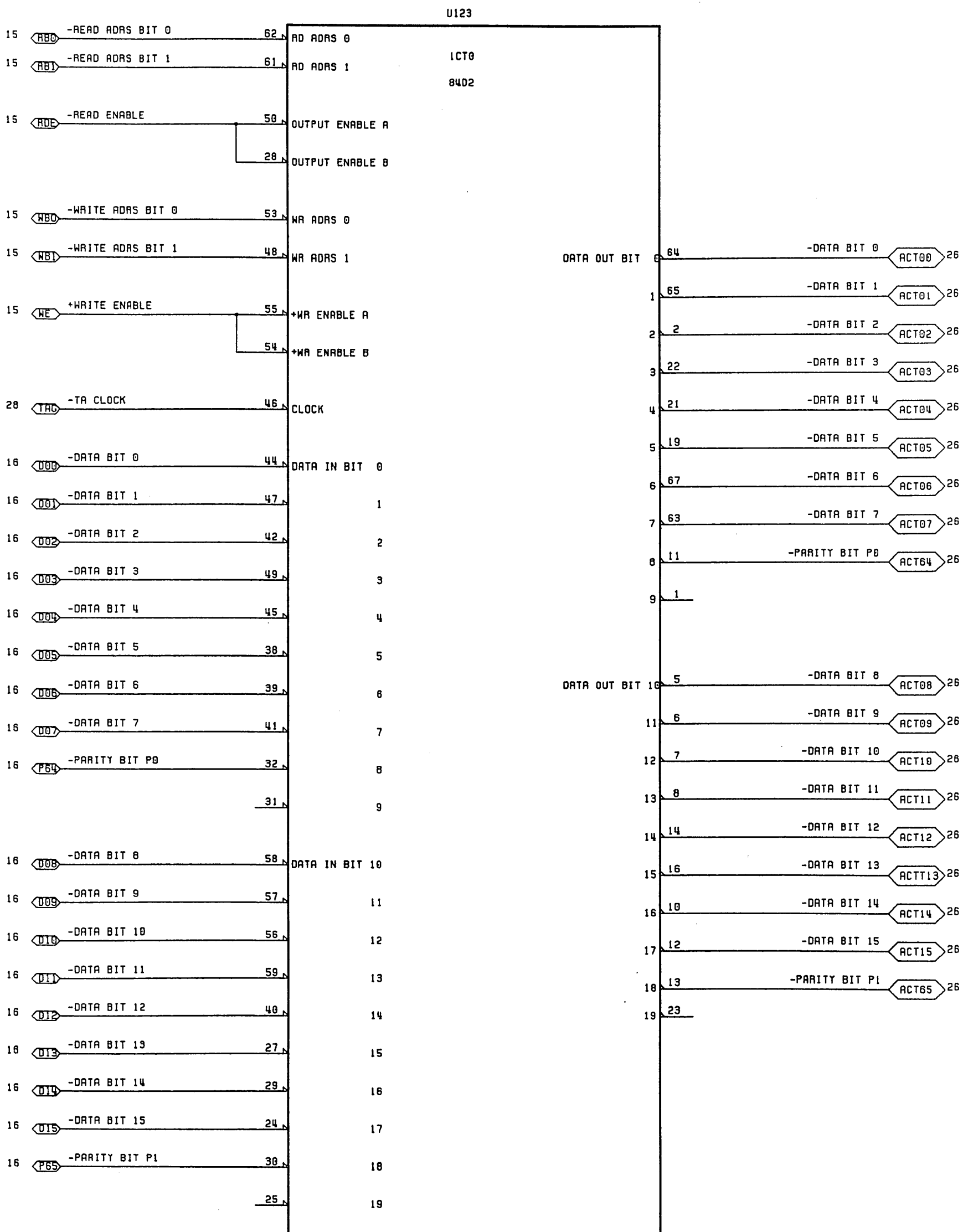
△ 3 4.5 INCH MAX

2 2 INCH MAX BETWEEN TAB2 AND 10114

 SEPARATE LINES TO CONNECTOR PINS

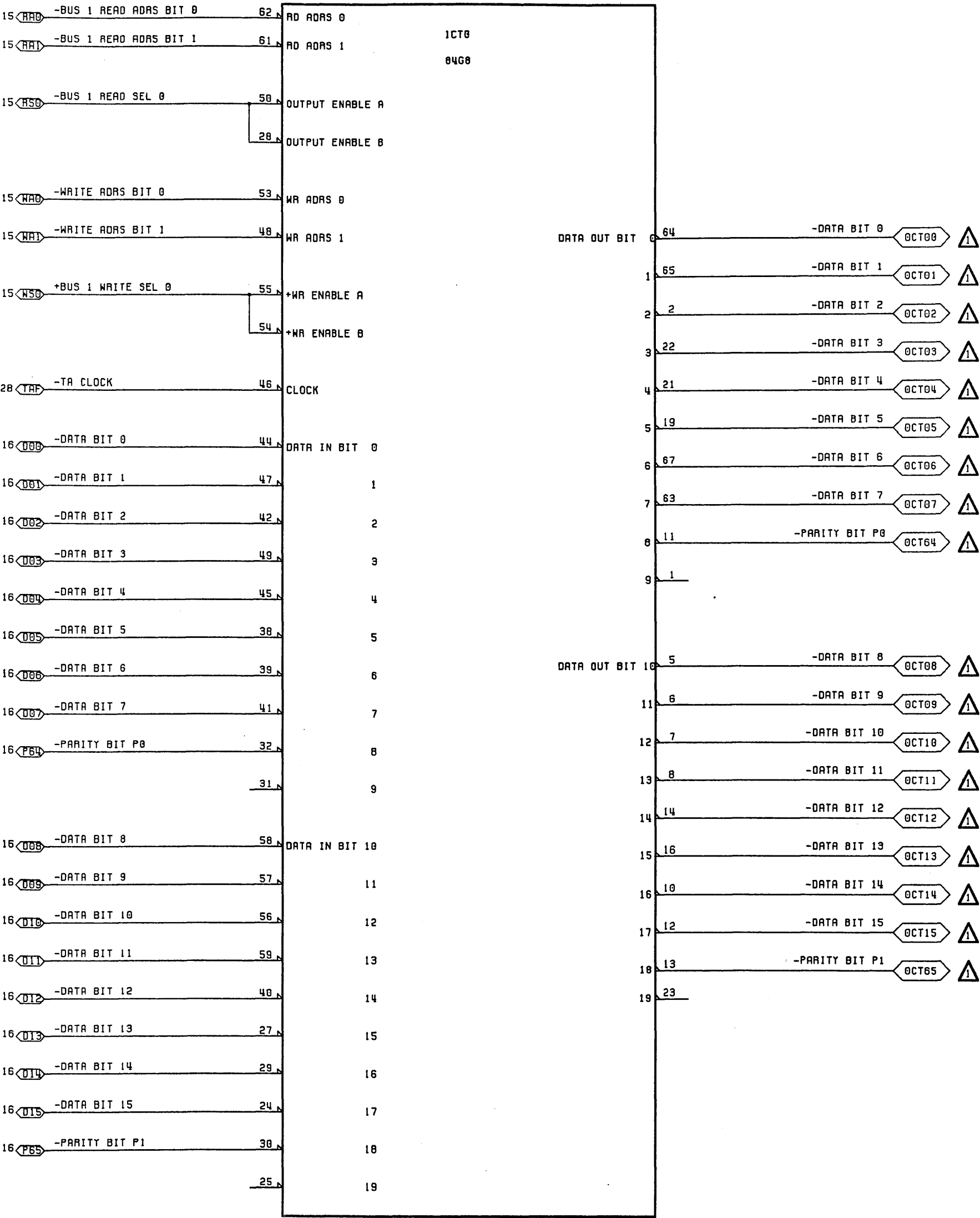
 CONTROL DATA	CMI DATA BOARD CMI READ DATA RECEIVERS AND FANOUT TYPE 1JHM		8	DWG NO. 53575507	DATE 11/01/85	REV A
	SHEET NO. 16		60462210		PAGE 16	

ADU CT MACRO CELL INPUT DATA



BUS 1 "0" CT MACRO CELL INPUT DATA

U124



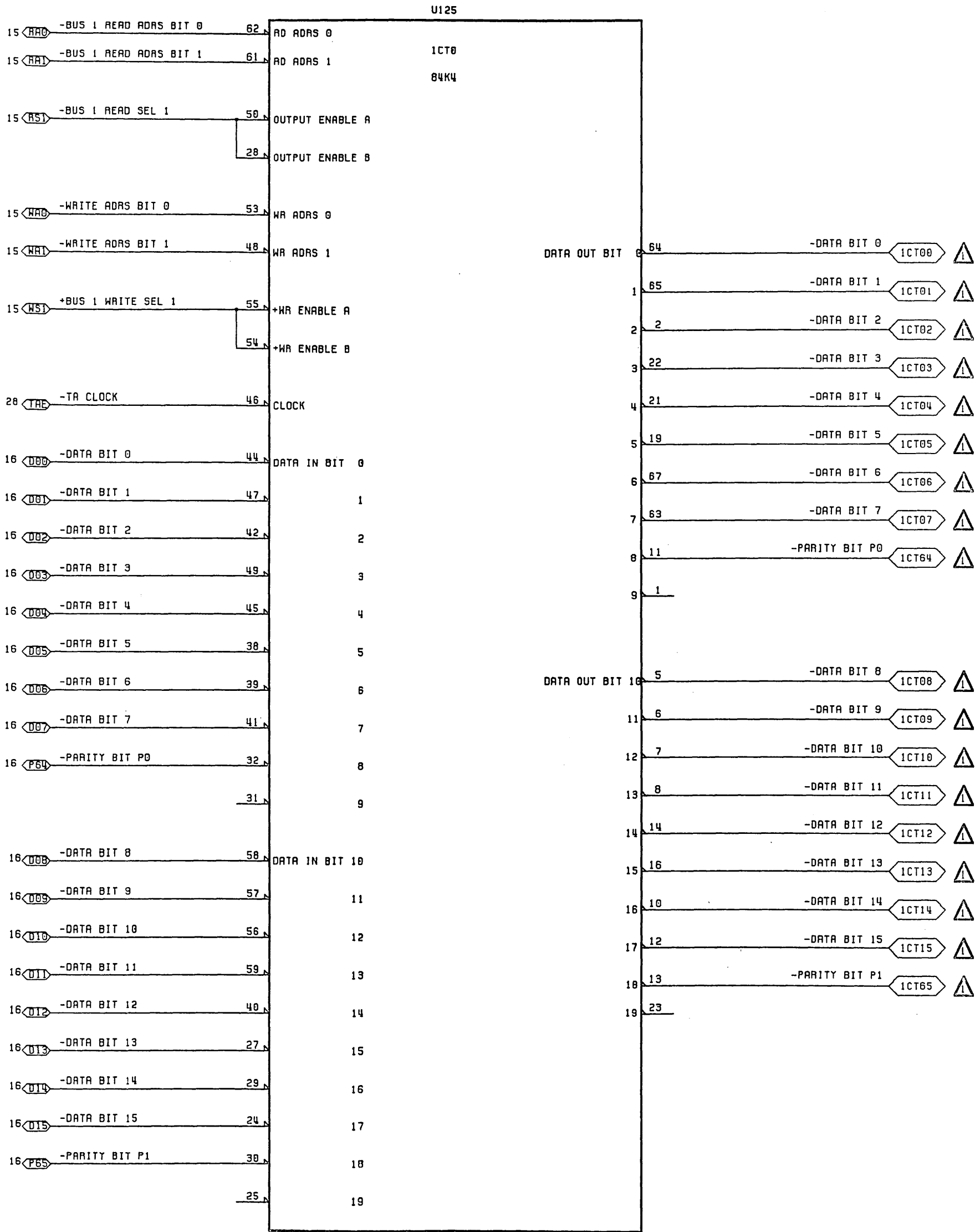
ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 24



CMI DATA BOARD
BUS 1 "0" CT MACRO CELL
INPUT DATA
TYPE 1JHH

B	DWG NO. 53575587	DATE 11/01/85	REV A
SHEET NO. 18		PAGE 60462210 JH-18	

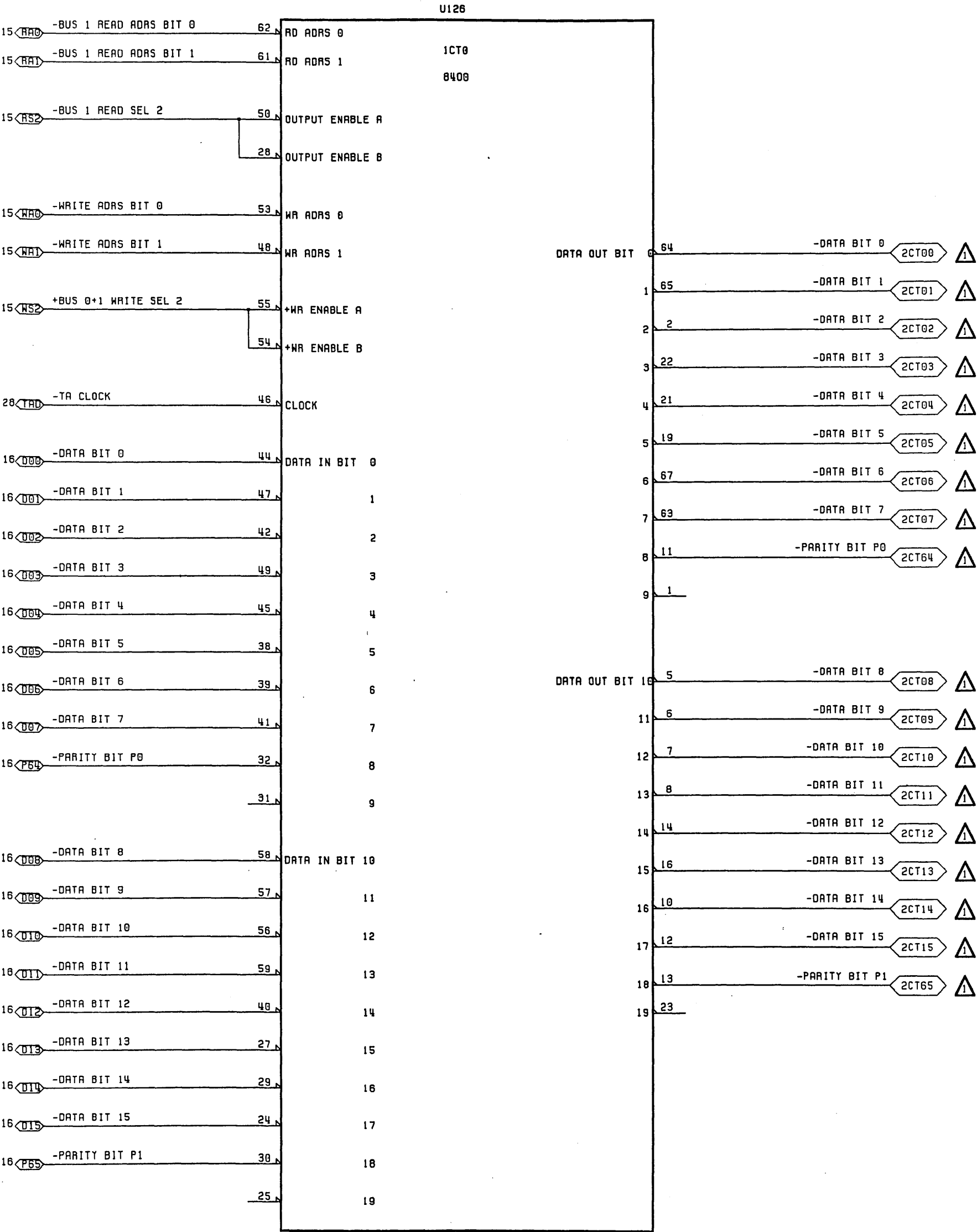
BUS 1 "1" CT MACRO CELL INPUT DATA



ALL OUTPUTS ARE WIRE "AND" ON PAGE 24

	CMI DATA BOARD		DWG NO.	DATE	REV
	BUS 1 "1" CT MACRO CELL		B	53575507	11/01/85
	INPUT DATA				A
TYPE 1JHH		SHEET NO. 19	60462210	PAGE	JH-19

BUS 1 "2" CT MACRO CELL INPUT DATA



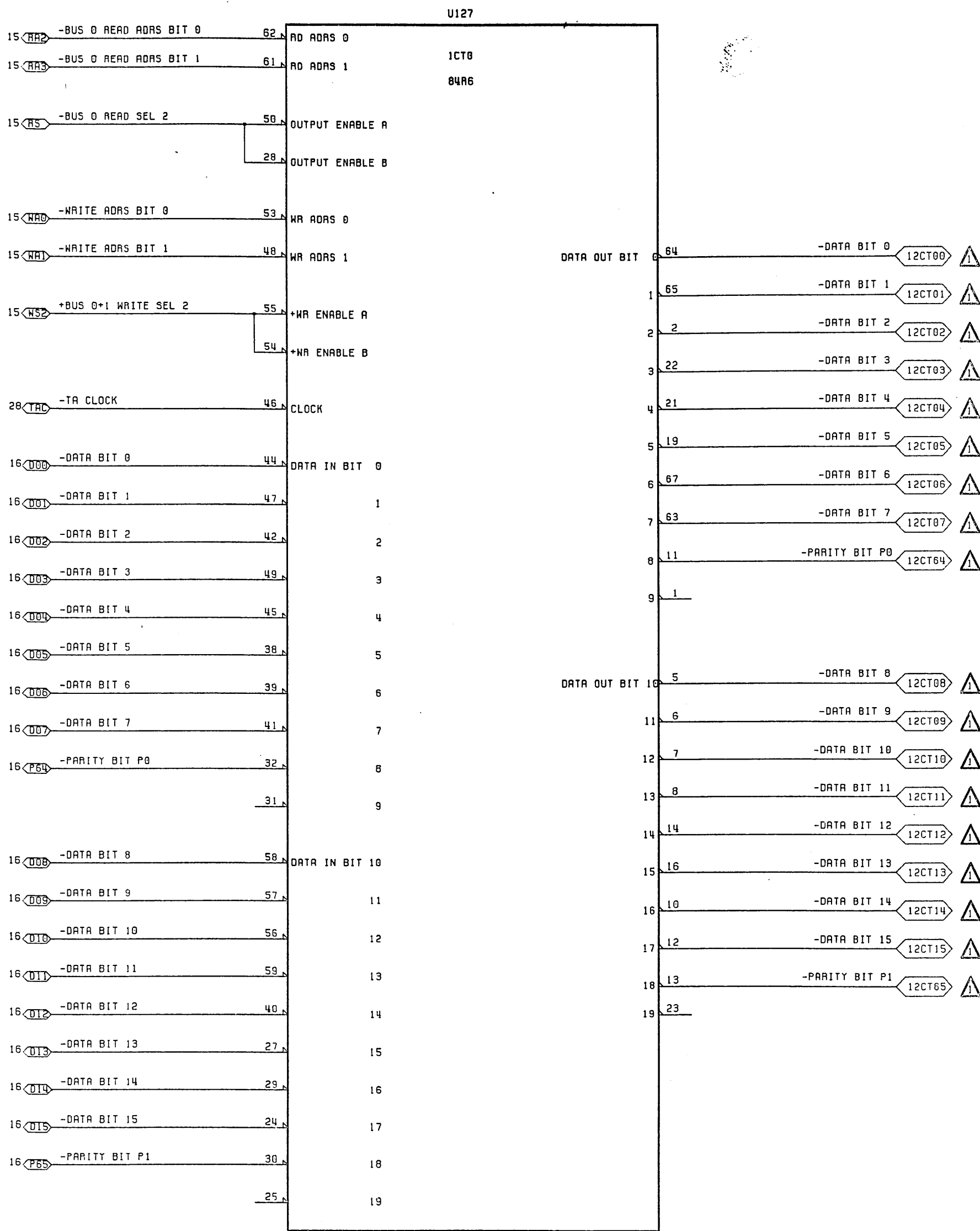
ALL OUTPUTS ARE WIRE "AND" ON PAGE 24




CMI DATA BOARD
BUS 1 "2" CT MACRO CELL
INPUT DATA
TYPE 1JHM

B	DWG NO. 53575507	DATE 11/01/85	REV A
SHEET NO. 20		60462210	PAGE JH-20

BUS 0 "2" CT MACRO CELL INPUT DATA

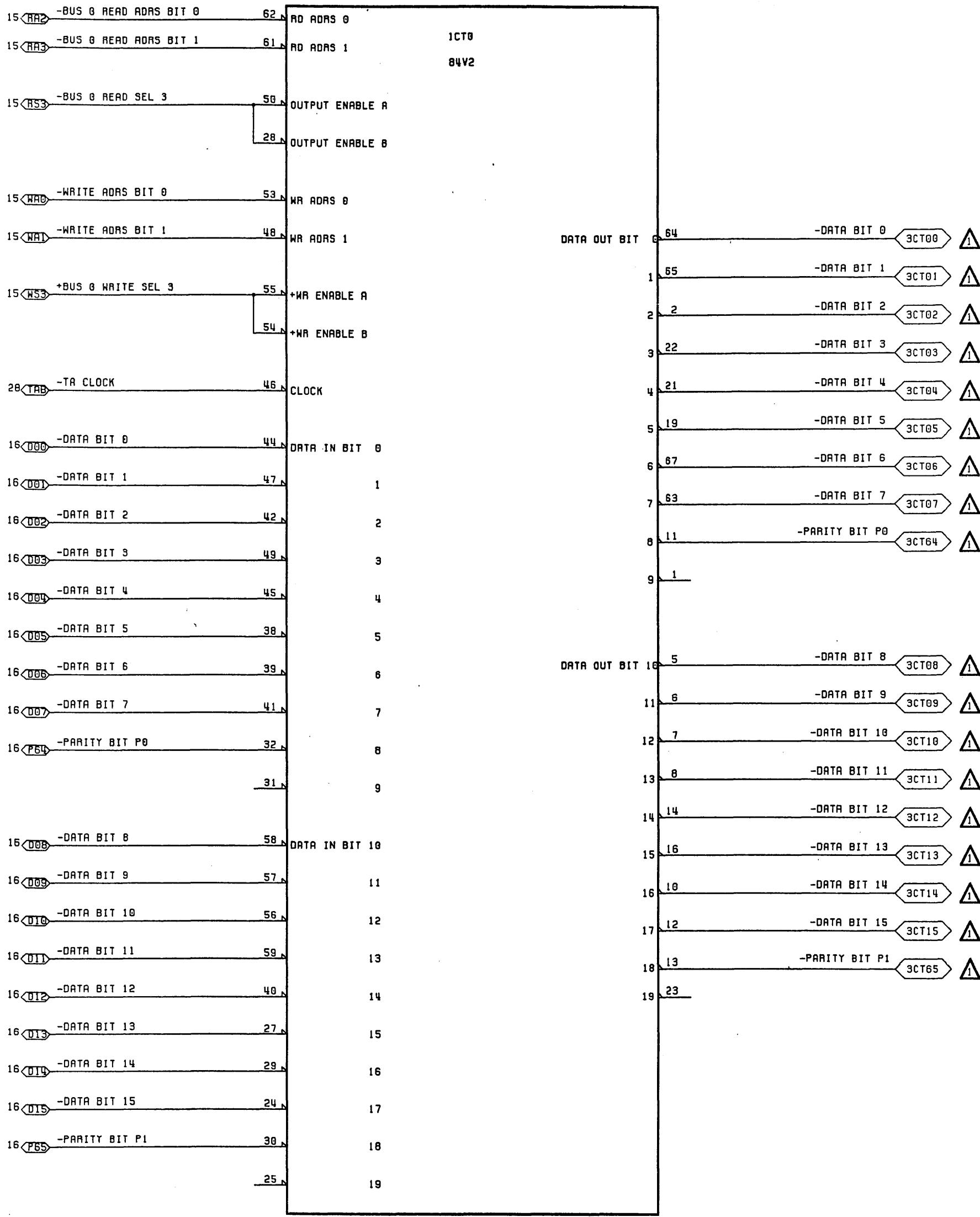


ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 25

 CONTROL DATA	CMI DATA BOARD BUS 0 "2" CT MACRO CELL INPUT DATA TYPE 1JHH	B	DWG NO.	DATE	REV
			53575507	11/01/85	A
			SHEET NO. 21		60462210

BUS 0 "3" CT MACRO CELL INPUT DATA

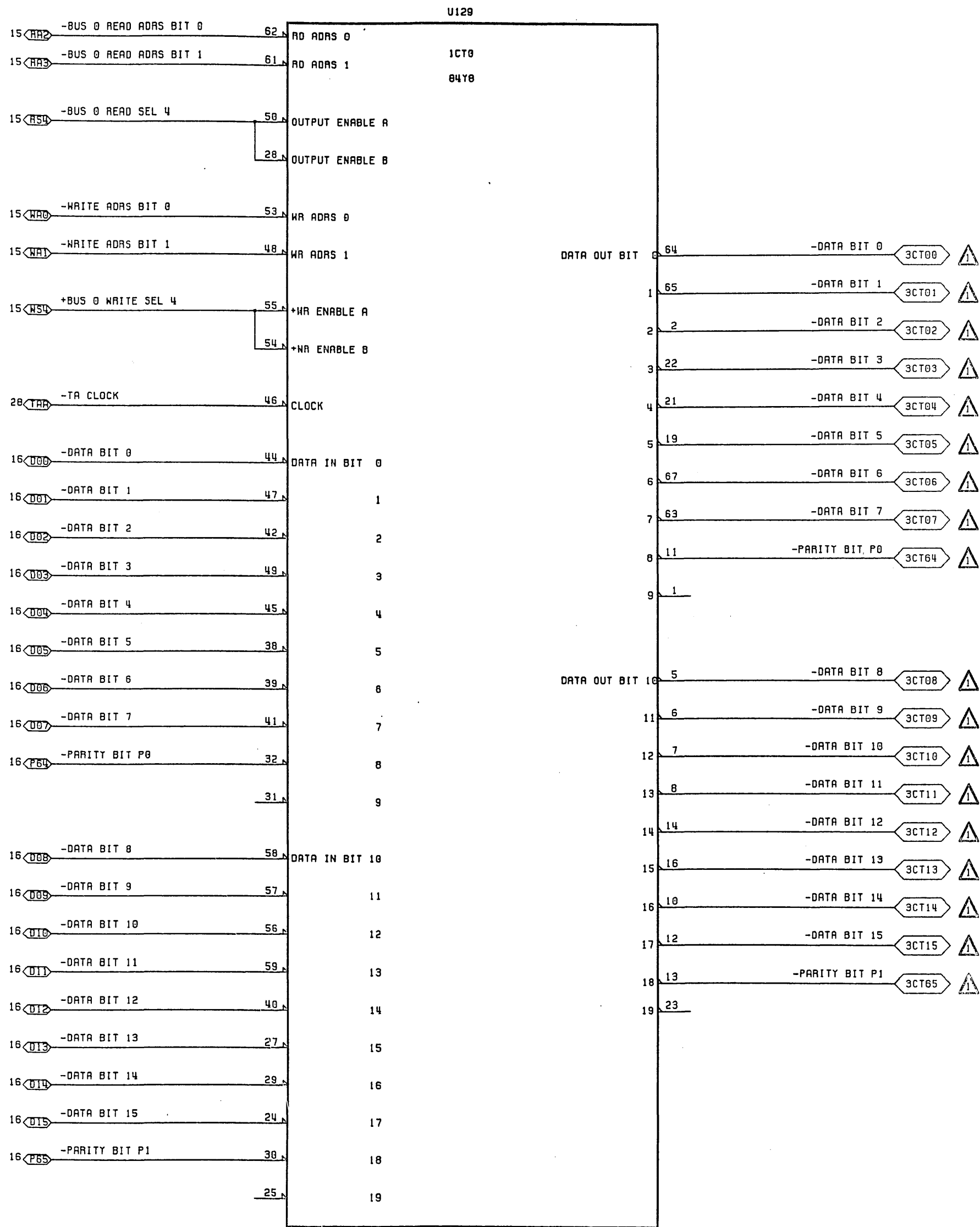
U128



ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 25

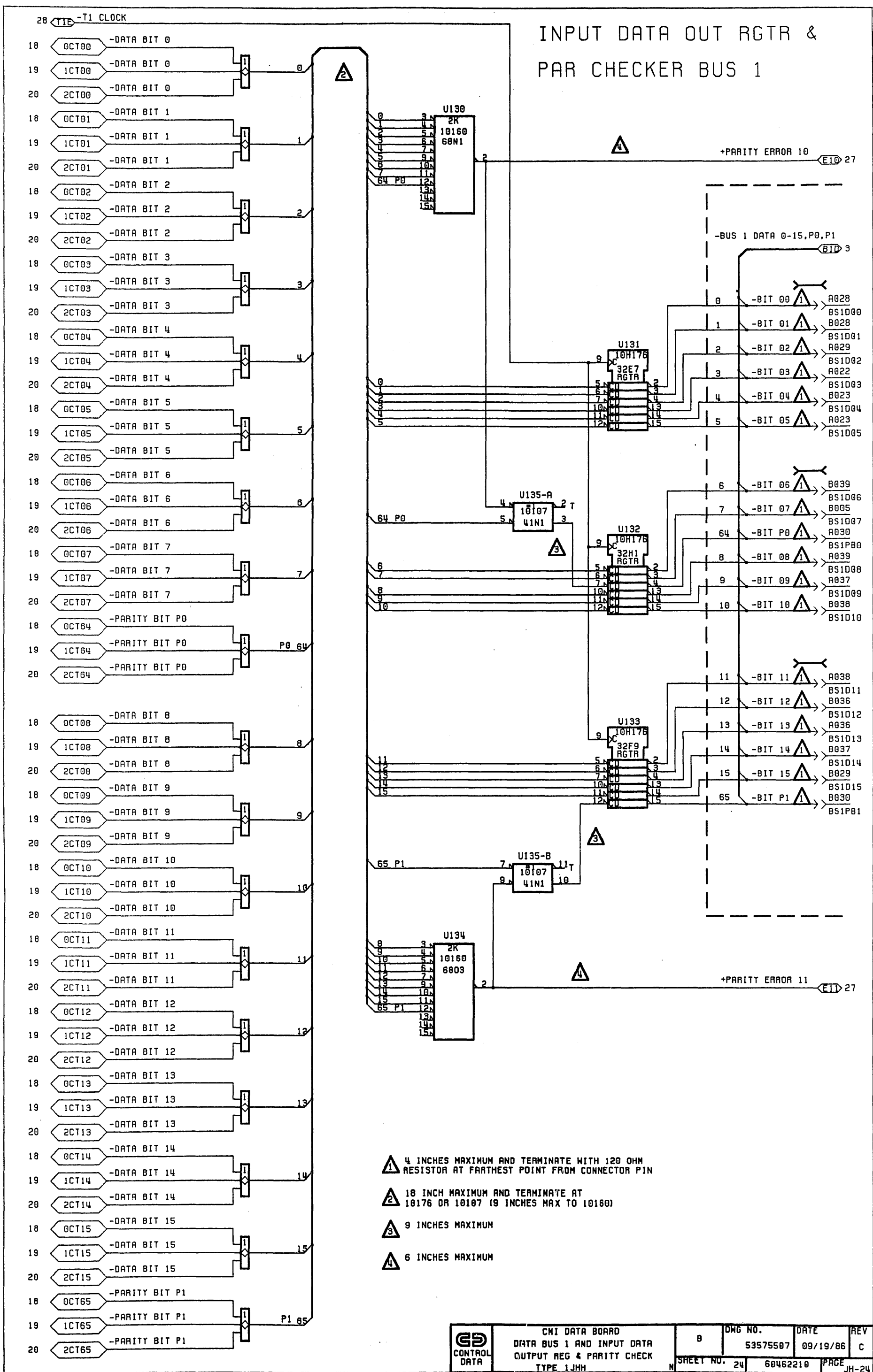
 CONTROL DATA	CM1 DATA BOARD		B	DWG NO.		DATE		REV	
	BUS 0 "3" CT MACRO CELL						A		
	INPUT DATA								
	TYPE 1JHH		N	SHEET NO. 22		60462210		PAGE	
				JH-22					

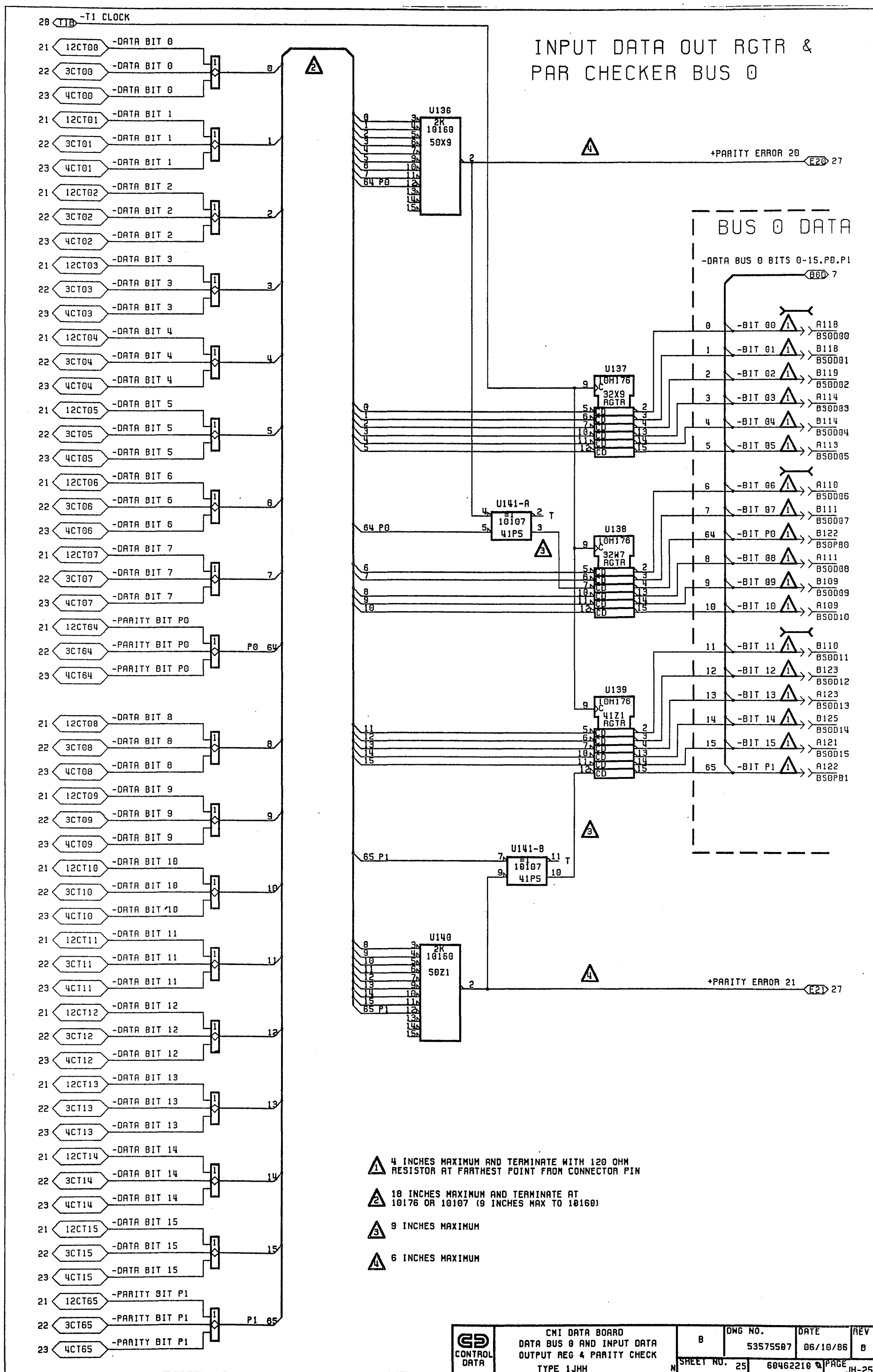
BUS 0 "4" CT MACRO CELL INPUT DATA



ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 25

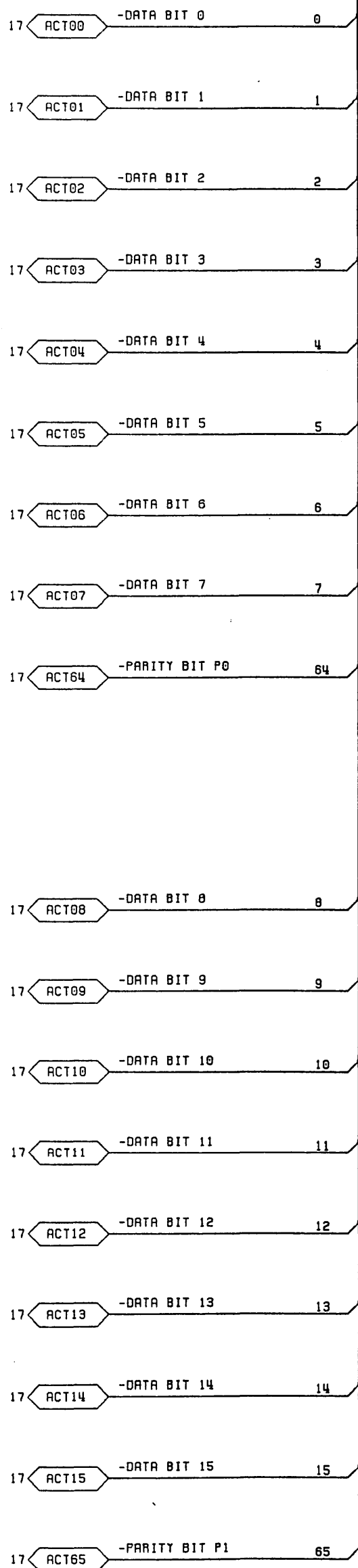
CONTROL DATA	CM1 DATA BOARD BUS 0 "4" CT MACRO CELL INPUT DATA TYPE 1JHH	8	DWG NO. 53575507	DATE 11/01/85	REV A
			SHEET NO. 23	60462210	PAGE JH-23






INPUT DATA OUT RGTRS & PAR CHECKER AND ADU DATA OUT

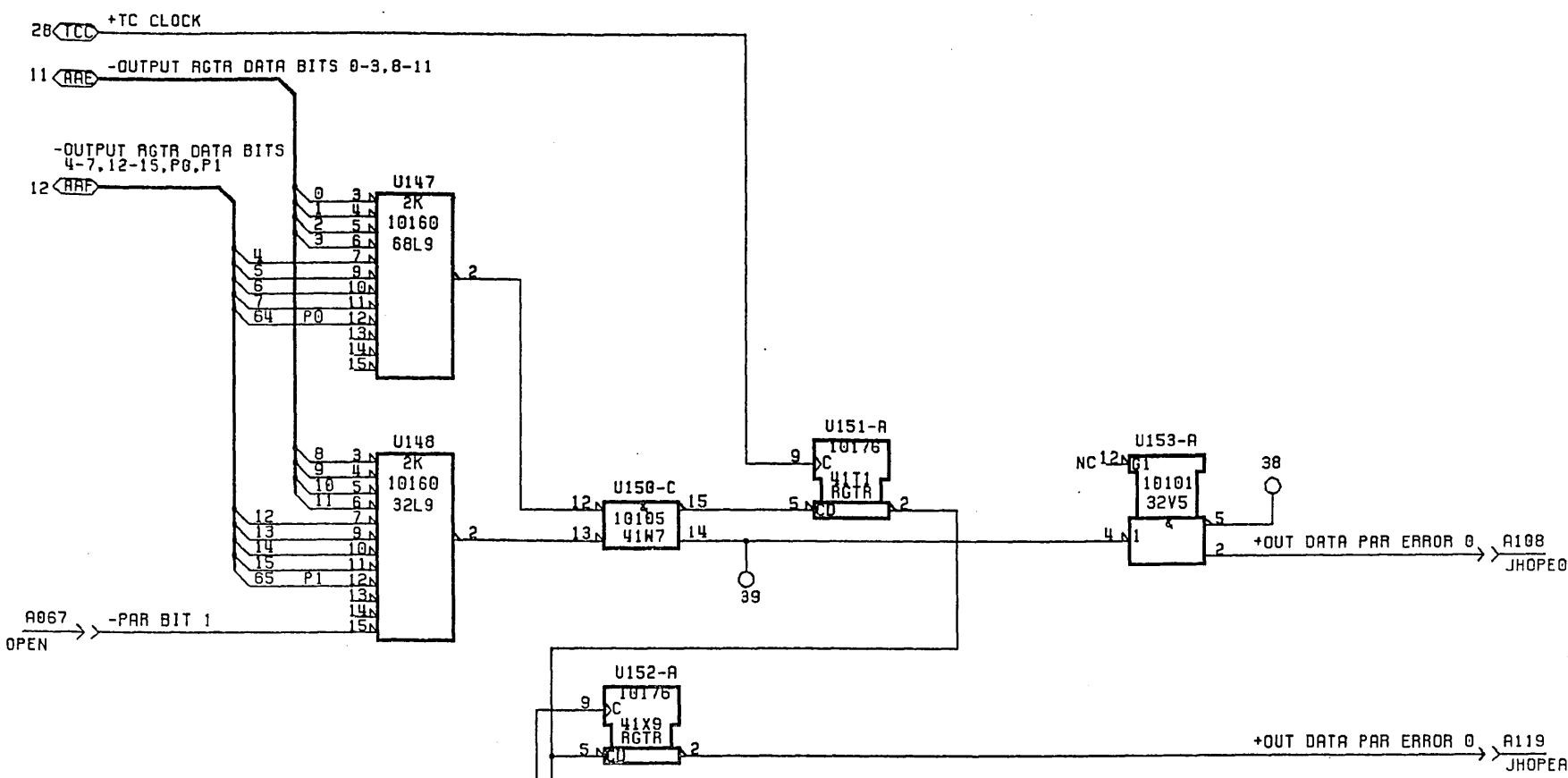
28 T1C -T1 CLOCK



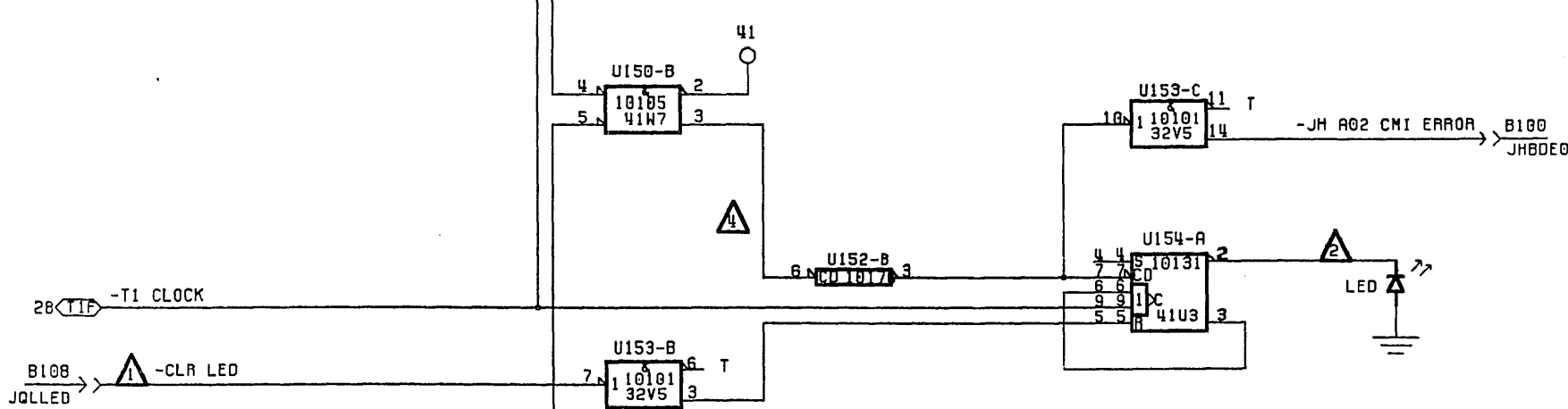
- △ 18 INCHES MAXIMUM AND TERMINATE AT 10176 OR 10107 (9 INCHES MAX TO 10160)
- △ 9 INCHES MAXIMUM
- △ 6 INCHES MAXIMUM

 CONTROL DATA	CMI DATA BOARD	B	DWG NO.	DATE	REV
	ADU DATA AND INPUT DATA		53575507	11/01/85	A
	OUTPUT REGISTER & PARITY CHECK				
TYPE 1JHH		SHEET NO.	26	60462210	PAGE JH-26

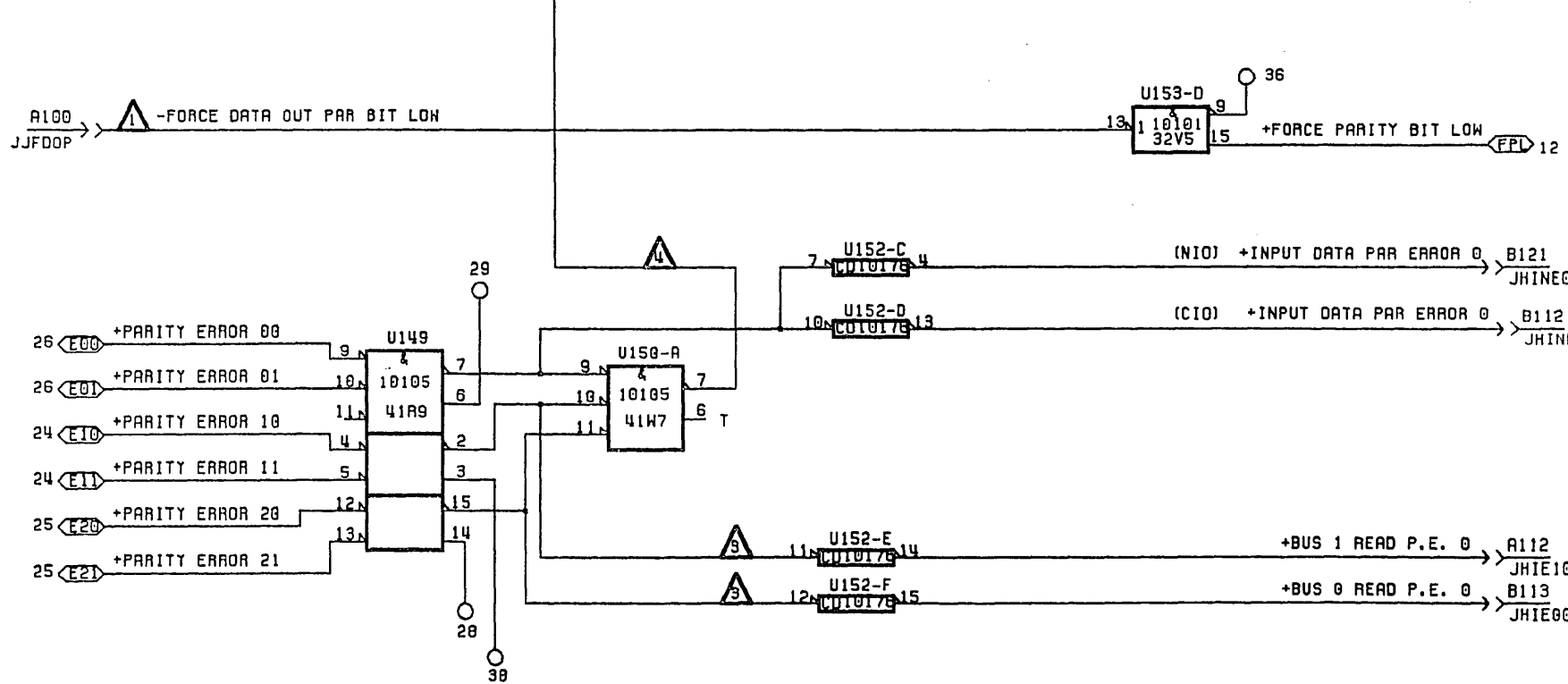
OUT DATA PAR CHECKER




ERROR LED



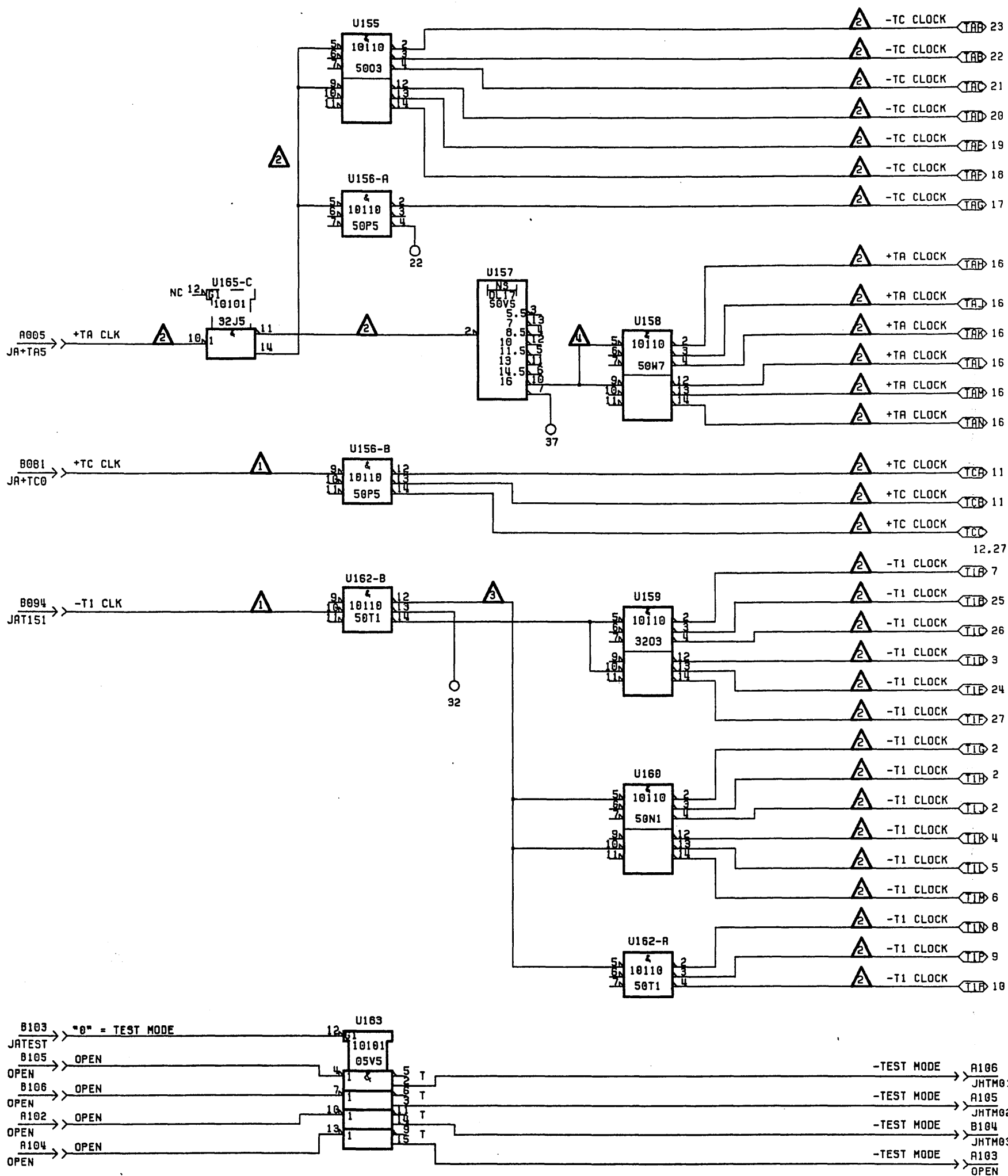
INPUT DATA PAR CHECKER



- 1 NOT TERMINATED ON THIS BOARD AND 6 INCHES MAXIMUM
- 2 TERMINATE
- 3 6 INCHES MAXIMUM
- 4 3 INCHES MAXIMUM

 CONTROL DATA	CMI DATA BOARD INPUT/OUTPUT PARITY CHECK AND ERROR LED TYPE 1JHH	B	DWG NO.	DATE	REV
			53575507	09/19/86	C
			SHEET NO. 27		

CLK F/O



8103 - "0" = TEST MODE
 JATEST 8105 - OPEN
 OPEN 8106 - OPEN
 OPEN 8102 - OPEN
 OPEN 8104 - OPEN
 OPEN


8095 - FORCE ADAS OUT PAR BIT LOW
 JJFAD0 8095 - FORCE DATA IN PAR BIT LOW
 JJFD1P 8096 - ADAS BIT 62
 JJAD62 8096 - ADAS BIT 63
 JJAD63 8115 - BUS 1 READ ENBL
 JJBIRE 8115 - BUS 0 READ ENBL
 JJB0RE 8116 - FORCE DATA OUT PAR BIT LOW
 JJFD0P 8116
 OPEN 8127
 OPEN 8127
 OPEN 8126
 OPEN 8128
 OPEN

7 INCHES MAXIMUM
 12 INCHES MAXIMUM
 4 INCHES MAXIMUM
 3 INCHES MAXIMUM

 CONTROL DATA	CMI DATA BOARD CLOCK FANOUT	B	DWG NO. 53575507	DATE 11/01/85	REV A
	TYPE 1JHH	SHEET NO. 20	60462210	PAGE	JH-20

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	15	+RD ENABLE ADU IN	27	15	+WR ADRS BIT0 BUS IN
02	15	+WRT ADRS BT0 ADU IN	28	27	-BUS0 DATA OUT ERROR
03	15	-WRT ENABLE ADU IN	29	27	-ADU DATA OUT ERROR
04	15	+WRT ADRS BT0 ADU IN	30	27	-BUS1 DATA OUT ERROR
05	11	+SEL BIT 0	31	15	+RD ADRS BIT2 ADU IN
06	15	+BUS 1 WRITE SEL 0	32	28	-T1 CLOCK
07	11	+SEL BIT 1	33	15	+BUS 0 WRITE SEL 3
08	15	-BUS 1 READ SEL 0	34		
09	03	-DATA BIT 0 BUS1 OUT	35	15	-BUS 0 READ SEL 3
10	02	-DATA BIT 0 ADU-CMI	36	27	-FRC DATAOUT PBS LOW
11	04	-DATA BIT 0 BUS1 CMI	37	28	+TA CLOCK
12	08	-DATA BIT 0 BUS0 OUT	38	27	-DATA OUTPUT ERROR
13	02	-DATA BIT 0 ADU OUT	39	27	-DATA OUTPUT ERROR
14	15	+BUS 1 WRITE SEL 1	40		
15	15	-BUS 1 READ SEL 1	41	27	+BOARD ERROR
16	03	-ADRS BIT 0 BUS1 OUT	42	15	+BUS 0 WRITE SEL 4
17	11	-DATA BIT 0 CMI-CMC	43	15	-BUS 0 READ SEL 4
18	11	-DATA BIT 0 OUT MUX	44	15	+RD ADR BIT0 BUS0 IN
19	13	-64 ns SQUARE WAVE	45	15	+RD ADR BIT1 BUS0 IN
20	15	+BUS 0+1 WRT SEL 2	46	15	+WR ADRS BIT1 BUS IN
21	15	-BUS 1 READ SEL 2	47	15	+RD ADRS BIT0 ADU IN
22	28	-TC CLOCK	48	15	+RD ADR BIT1 BUS1 IN
23	15	-FORCE ODD BITS SET	49	15	+RD ADR BIT0 BUS1 IN
24	15	-BUS 0 READ SEL 2	50	15	+FRC DATA IN PBS LOW
25	07	-DATA BIT 0 BUS0-CMI	51	15	-FORCE ODD BITS SET
26	15	-FORCE EVEN BITS SET			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 [NOT USED]
TERM	A095, B095, A096, B096, A115, B115, A116
UNUSED	A040, B040, A128
ISOLATED GROUND	B011, B049, B050, B051, B052, B053, B055, A068, A069, B069, A071, B074, B075, A099, A101, B101, B102, A120, B120

 CONTROL DATA	CMI DATA BOARD	8	DWG NO.	DATE	REV
	TESTPOINTS & SIGNAL NAMES		53565507	09/19/86	C
	AND CONNECTOR PINS				
	TYPE 1JHH	N	SHEET NO. 29	60462210	PAGE JH-29

CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

CMI DATA BOARD

[illegible]

LOC: A02, A03, A04, A05

DWN	S L PJESCICH	03/14/86
CHKD	L H JOHNSON	04/23/86
ENG	J P STROMBECK	04/23/86
PUBS	R K BONDE	04/24/86
APP	J P STROMBECK	04/23/86



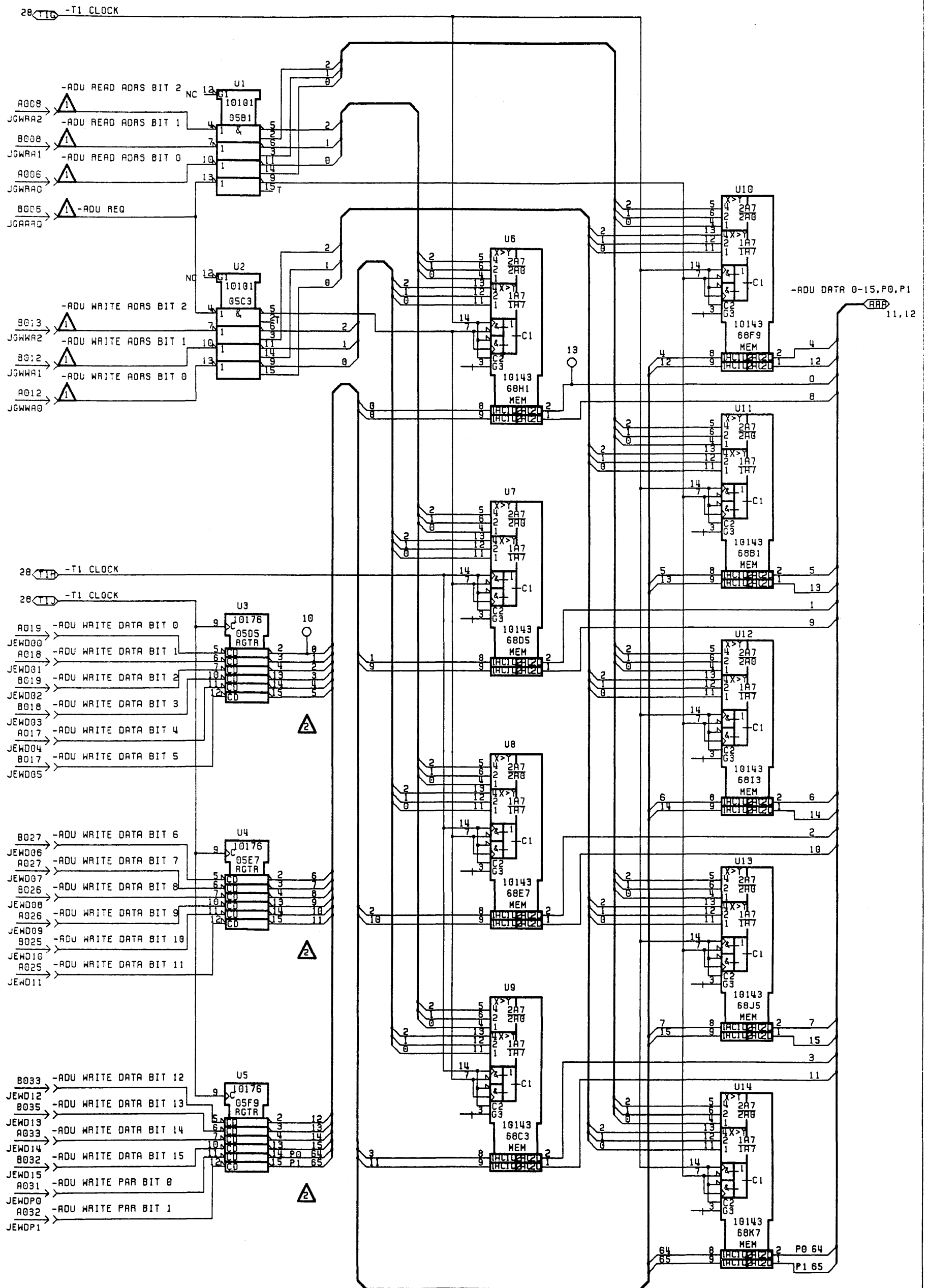
TYPE 1JHH

SHEET NO. 1

60462210

PAGE 11

WRITE BUFFER ADU DATA BITS 0-15, PAR 0,1

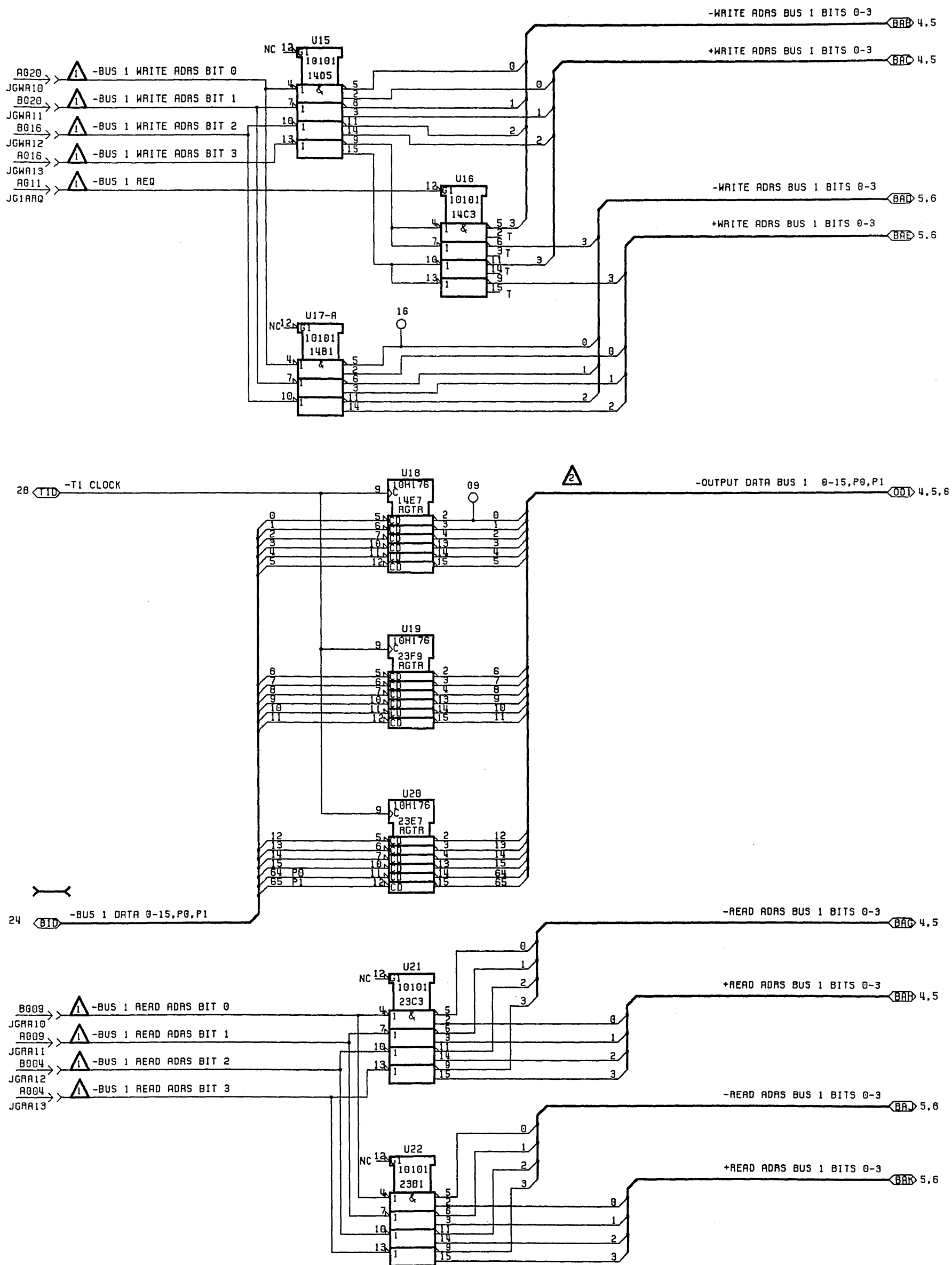


⚠ NOT TERMINATED ON THIS BOARD AND 3 INCHES MAXIMUM

⚠ 6 INCHES MINIMUM LENGTH


 CONTROL DATA	CMI DATA BOARD		DWG NO.	DATE	REV
	WRITE BUFFER ADU DATA		B	22105679	03/14/86
	BITS 0-15, PAR 0,1		SHEET NO. 2	60462210	PAGE JH-02
TYPE 1JHH					

CMI BUS 1 ADRS AND DATA OUT BUFFER

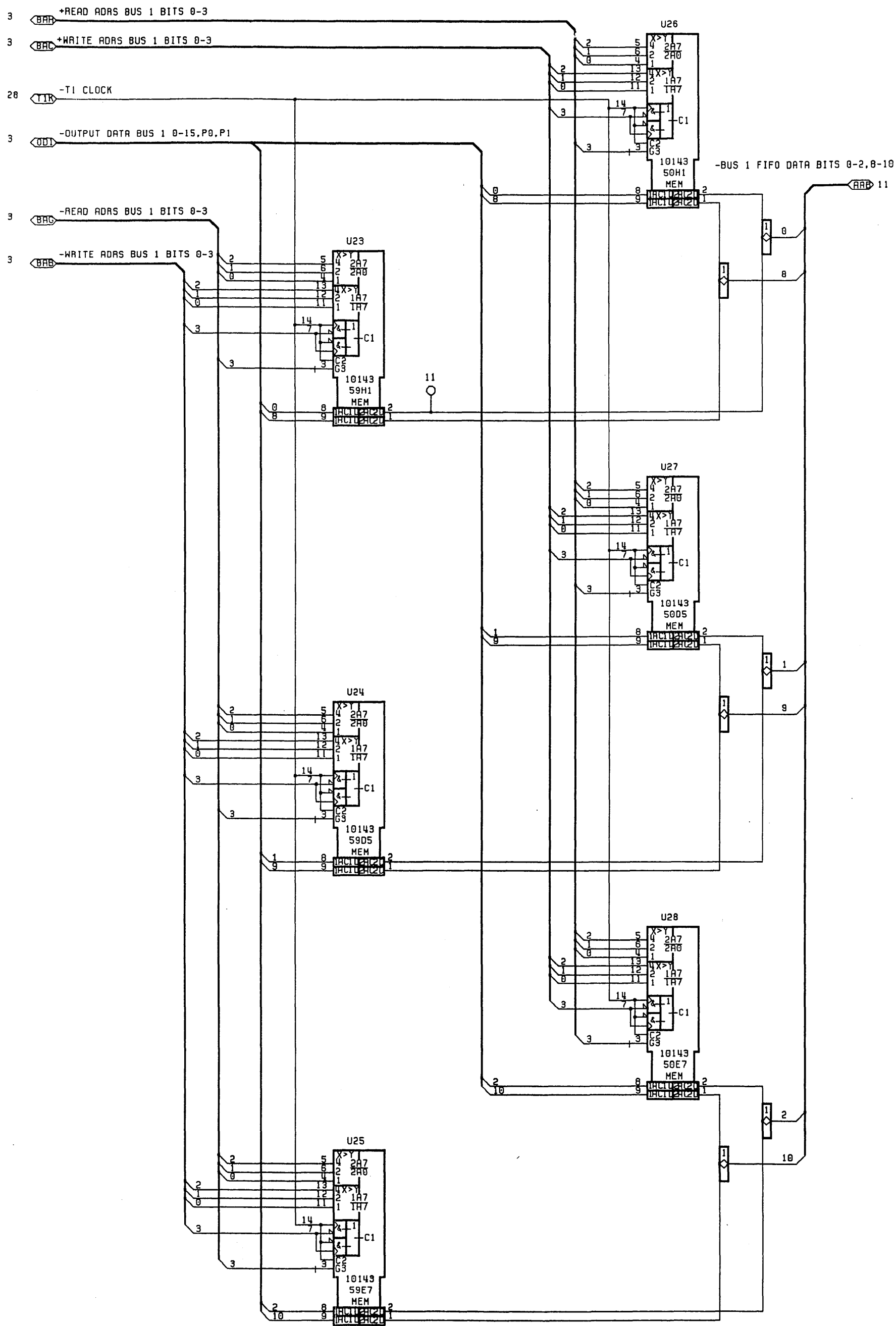



NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

 6 INCHES MINIMUM LENGTH

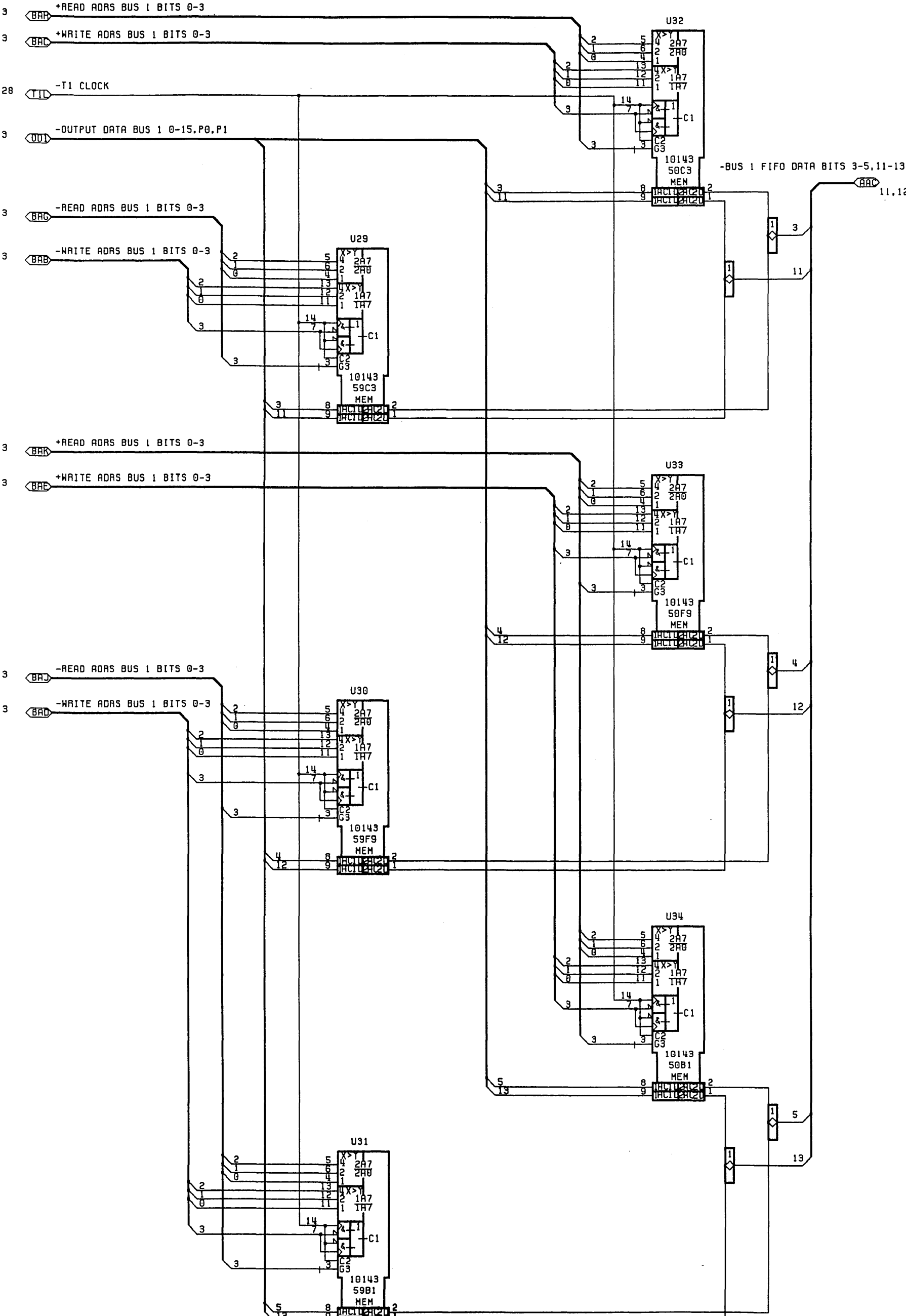
 CONTROL DATA	CMI DATA BOARD CMI BUS 1 ADDR AND DATA OUTPUT BUFFER TYPE 1JHH	B	DWG NO. 22105679	DATE 03/14/86	REV A
			SHEET NO. 3	60462210	PAGE JH-03


CMI FIFO BUS 1 BITS 0-2, 8-10 OUT BUFFER



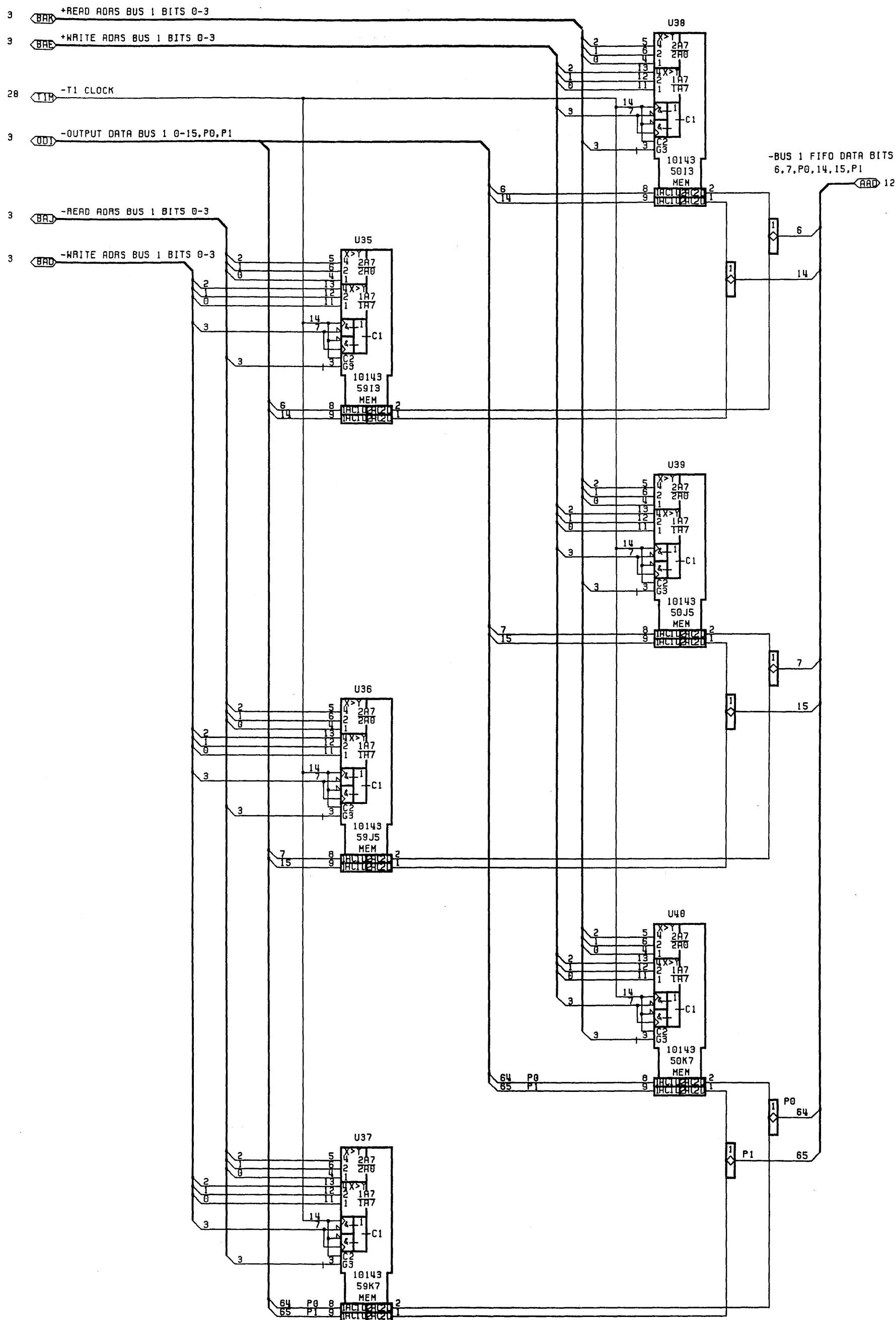
 CONTROL DATA	CMI DATA BOARD		DWG NO.	DATE	REV
	CMI FIFO BUS 1 0-2,		8	22105679	03/14/86
	8-10 OUTPUT BUFFER		SHEET NO. 4	60462210	PAGE JH-04

CMI FIFO BUS 1 BITS 3-5, 11-13 OUT BUFFER



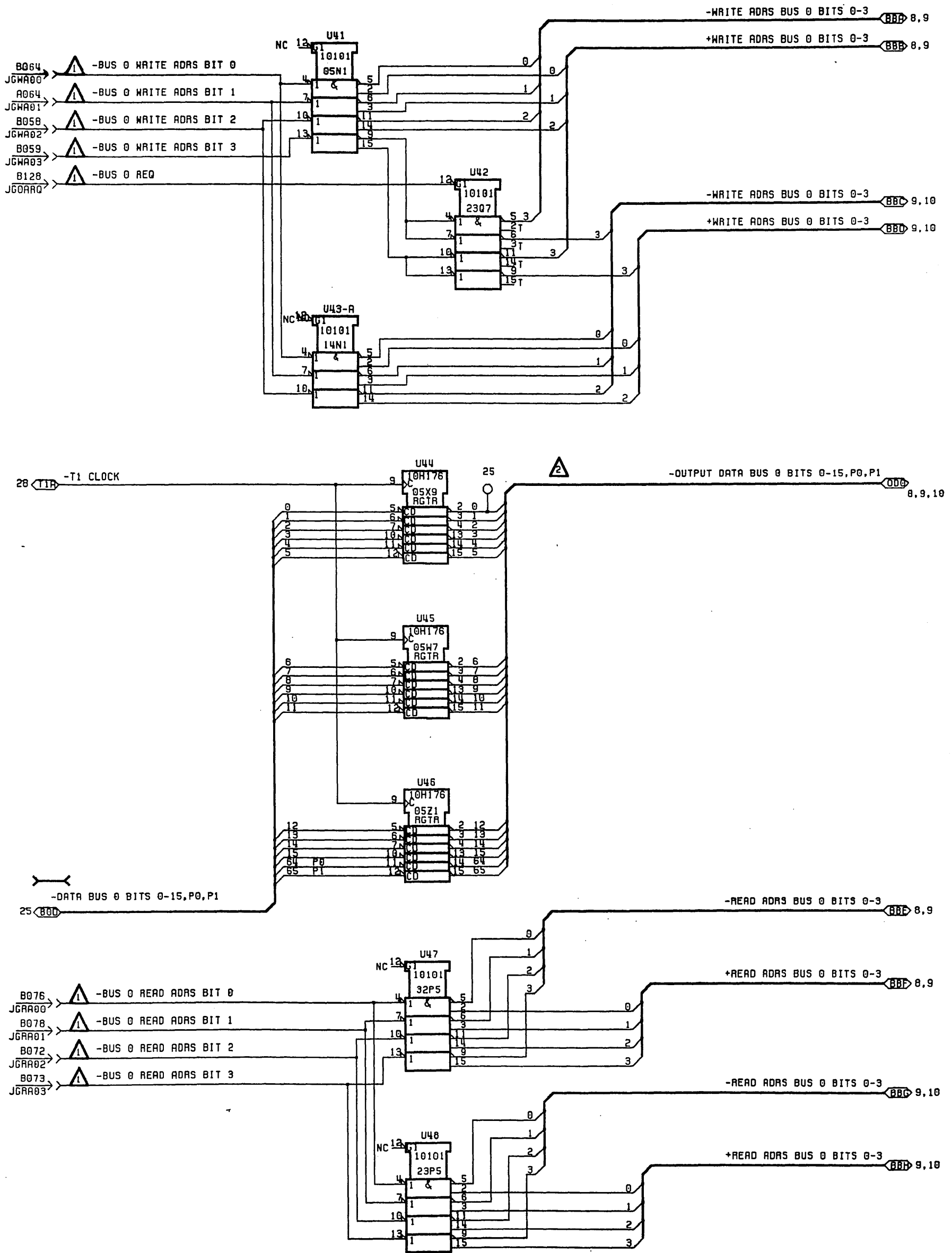
 CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 1 BITS 3-5, 11-13 OUTPUT BUFFER TYPE 1JHH	B	DWG NO. 22105679	DATE 03/14/86	REV. A
	SHEET NO. 5	60462210	PAGE 14-0		

CMI FIFO BUS 1 BITS 6,7,PAR 0, 14,15,PAR 1 OUT BUFFER




GD CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 1 BITS 6,7,P0, 14,15,P1 OUTPUT BUFFER TYPE 1JHH		DWG NO. B 22105679	DATE 03/14/86	REV A
	SHEET NO. 6		60462210	PAGE	JH-06

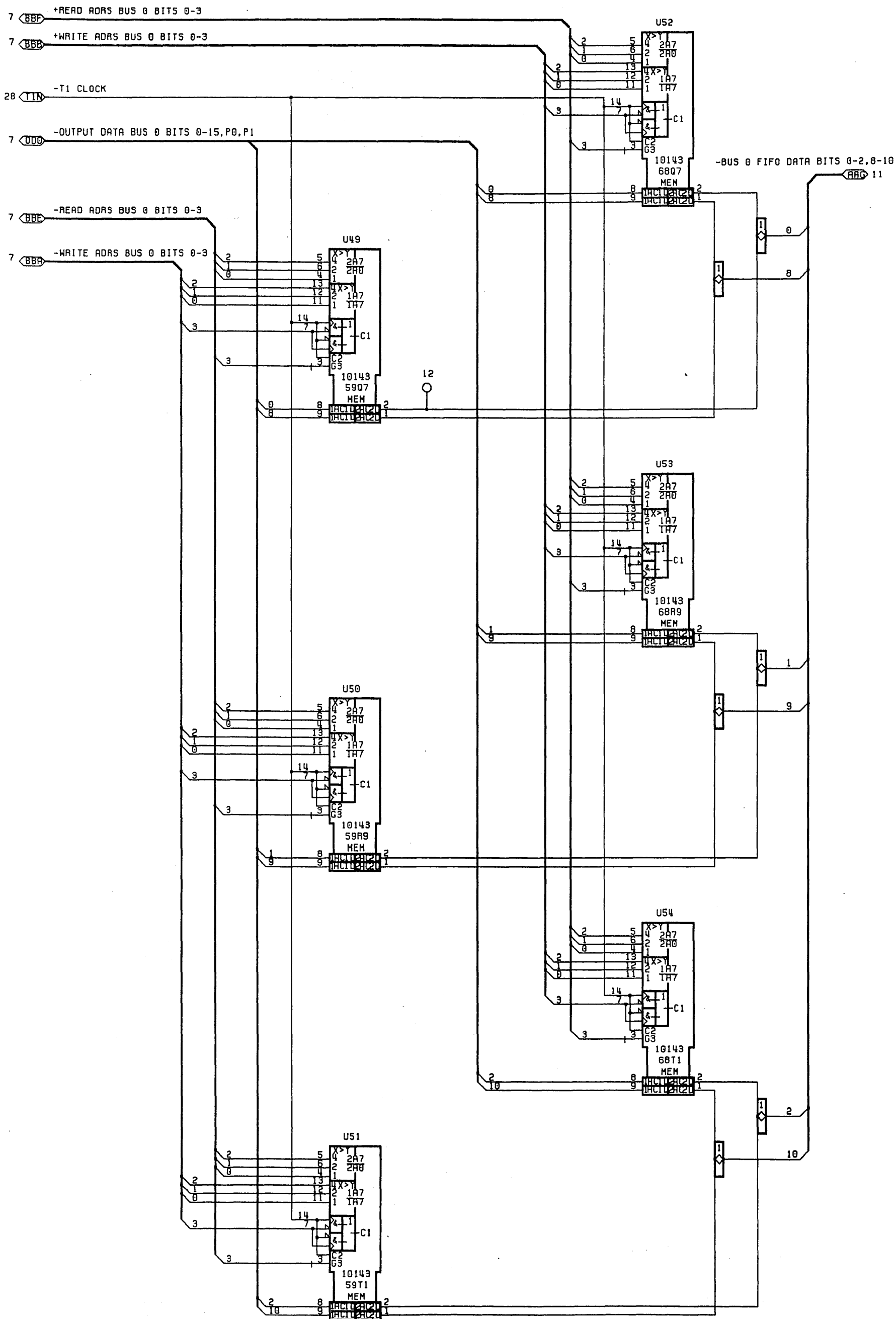
CMI BUS 0 ADRS AND DATA OUT BUFFER



2 6 INCHES MINIMUM LENGTH

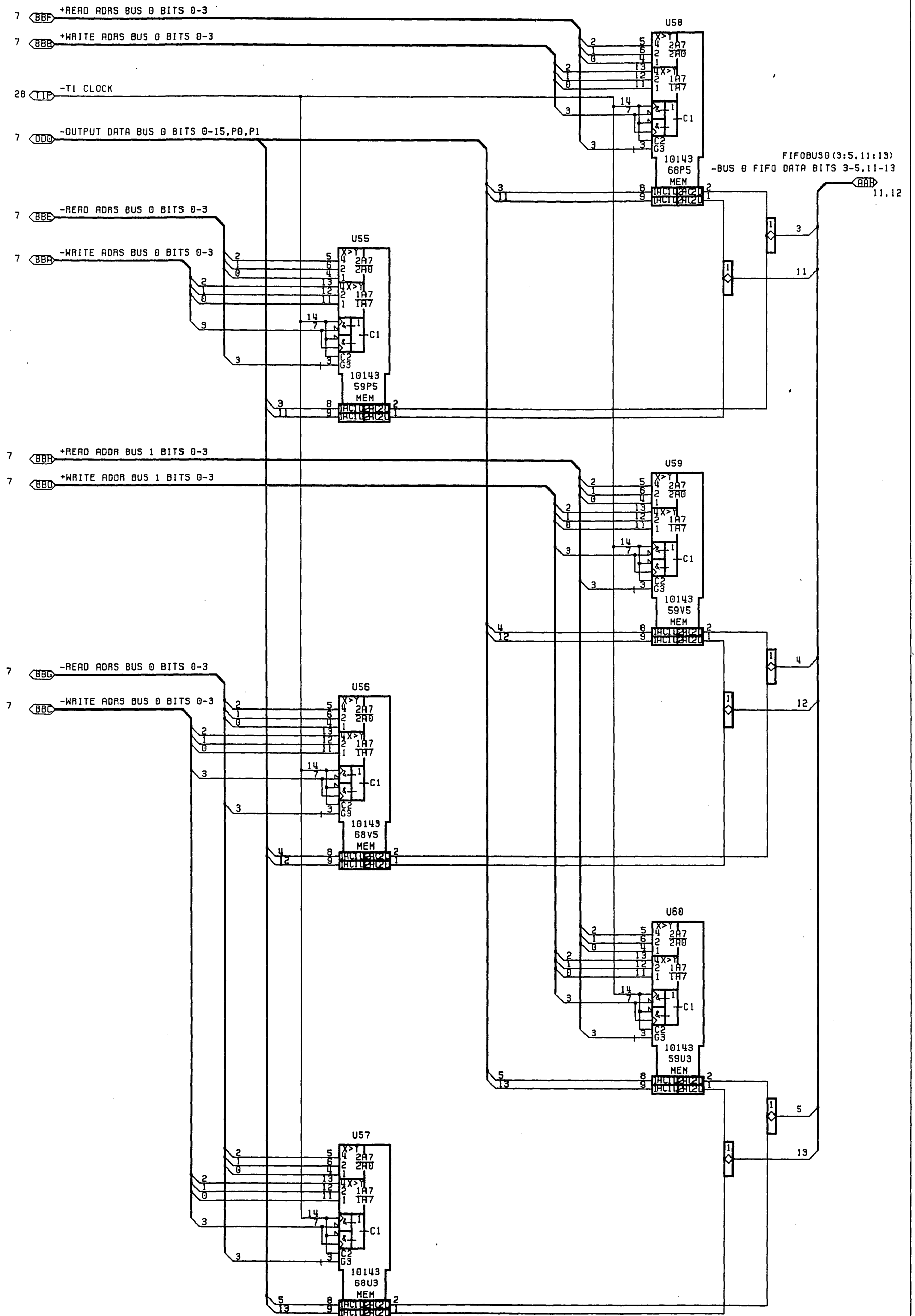
 CONTROL DATA	CMI DATA BOARD CMI BUS 8 ADDRESS AND DATA OUTPUT BUFFER TYPE 1JHH	B	DWG NO. 22185679	DATE 06/10/88	REV B
		SHEET NO. 7	60462210	PAGE	JH-87


CMI FIFO BUS 0 BITS 0-2, 8-10 OUT BUFFER



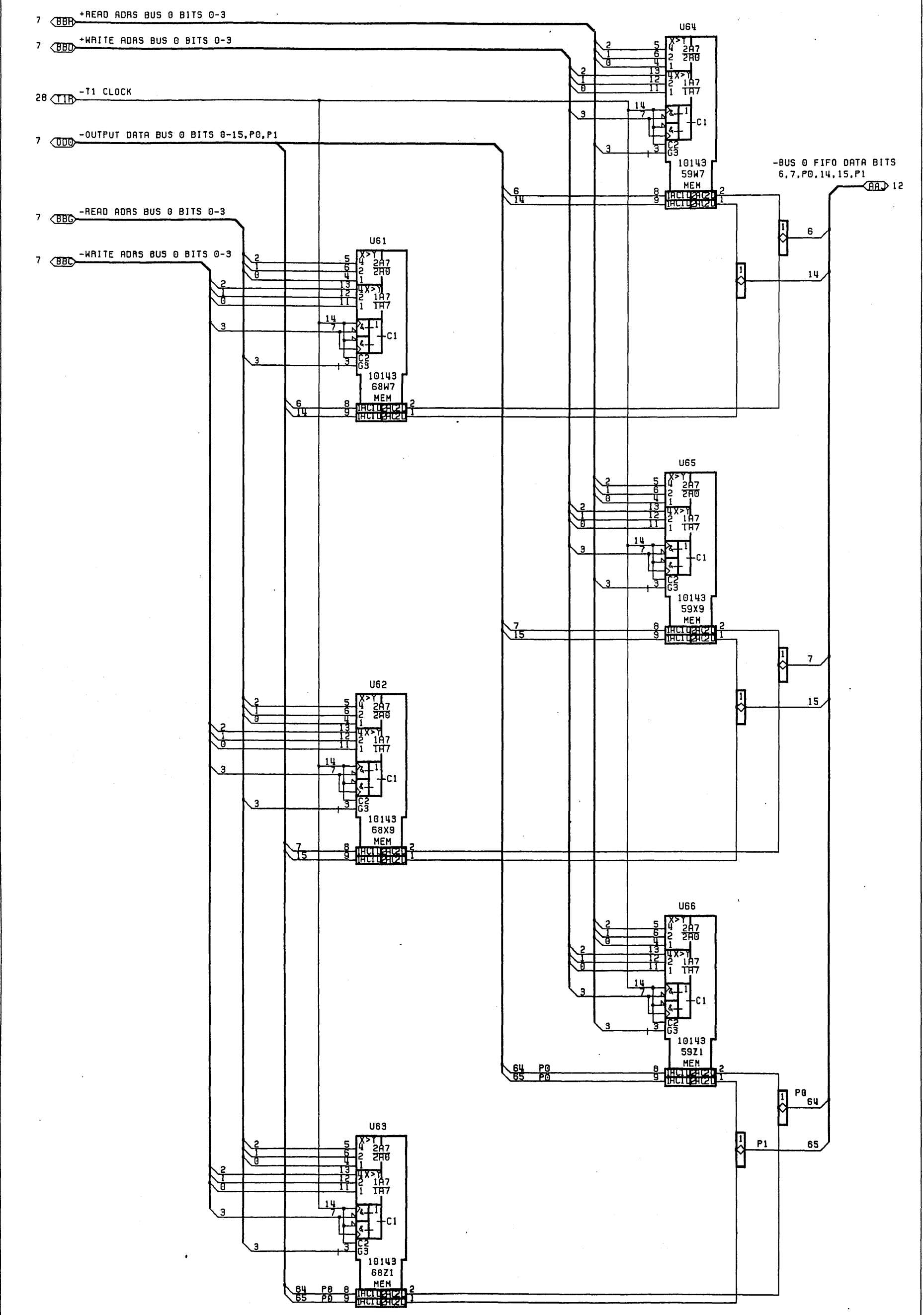
CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 0 BITS 0-2, 8-10 OUTPUT BUFFER TYPE 1JHH	B	DWG NO. 22105679	DATE 03/14/86	REV A
			SHEET NO. 8	60462210	PAGE JH-08

CMI FIFO BUS 0 BITS 3-5, 11-13 OUT BUFFER



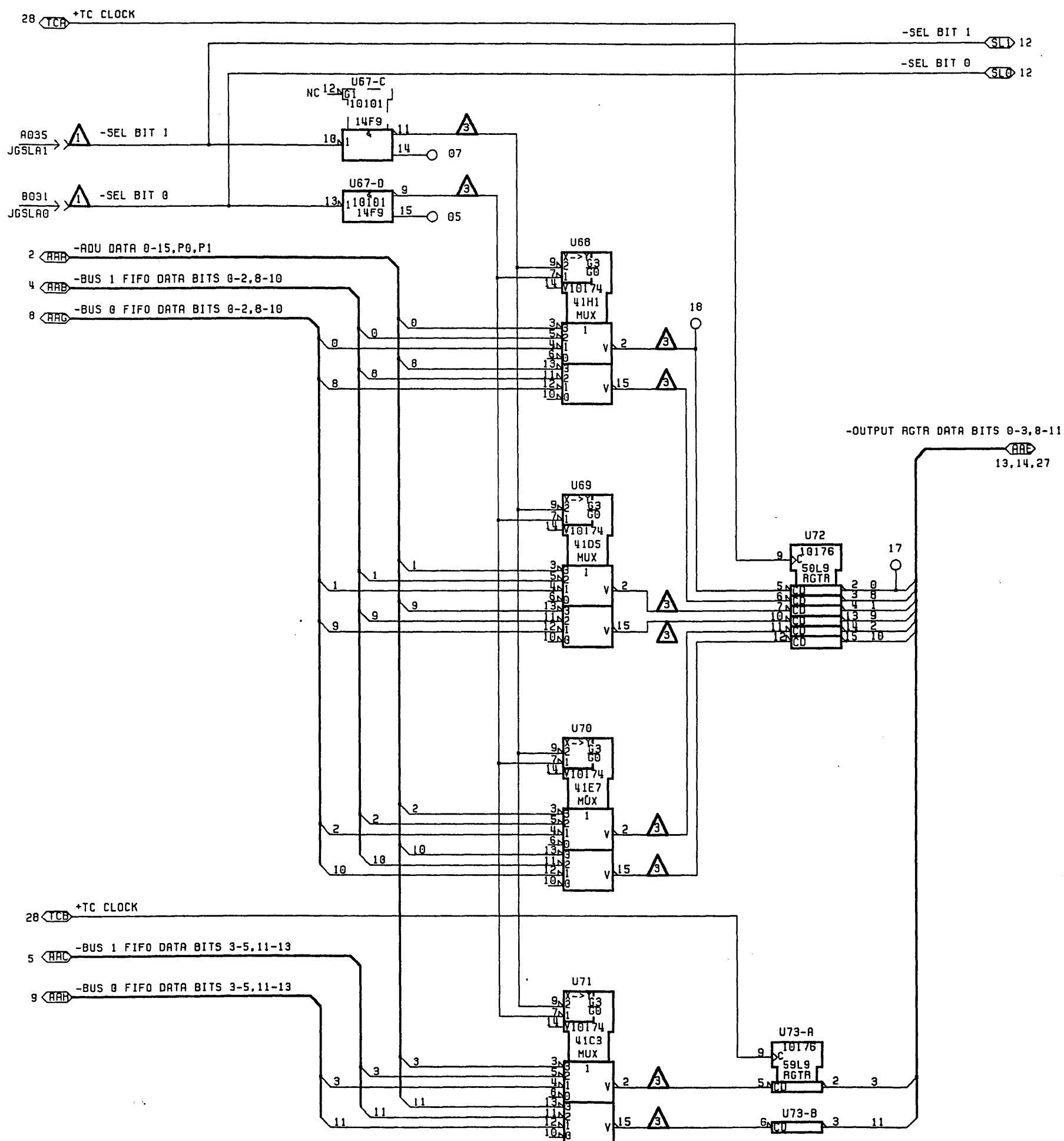
 CONTROL DATA	CMI DATA BOARD CMI FIFO BUS 0 BITS 3-5, 11-13 OUTPUT BUFFER TYPE 1JHH	B	DWG NO.	DATE	REV
			22105679	03/14/86	A
			SHEET NO. 9		

CMI FIFO BUS 0 BITS 6,7,PAR 0, 14,15,PAR 1 OUT BUFFER




	CMI DATA BOARD		DWG NO.	DATE	REV
	CMI FIFO BUS 0 BITS 6,7,P0, 14,15,P1 OUTPUT BUFFER		B 22105679	03/14/86	A
	TYPE 1JHH		SHEET NO. 10	60462210	PAGE JH-10

CMI OUT DATA MUX AND OUT RGTR BITS 0-3, 8-11

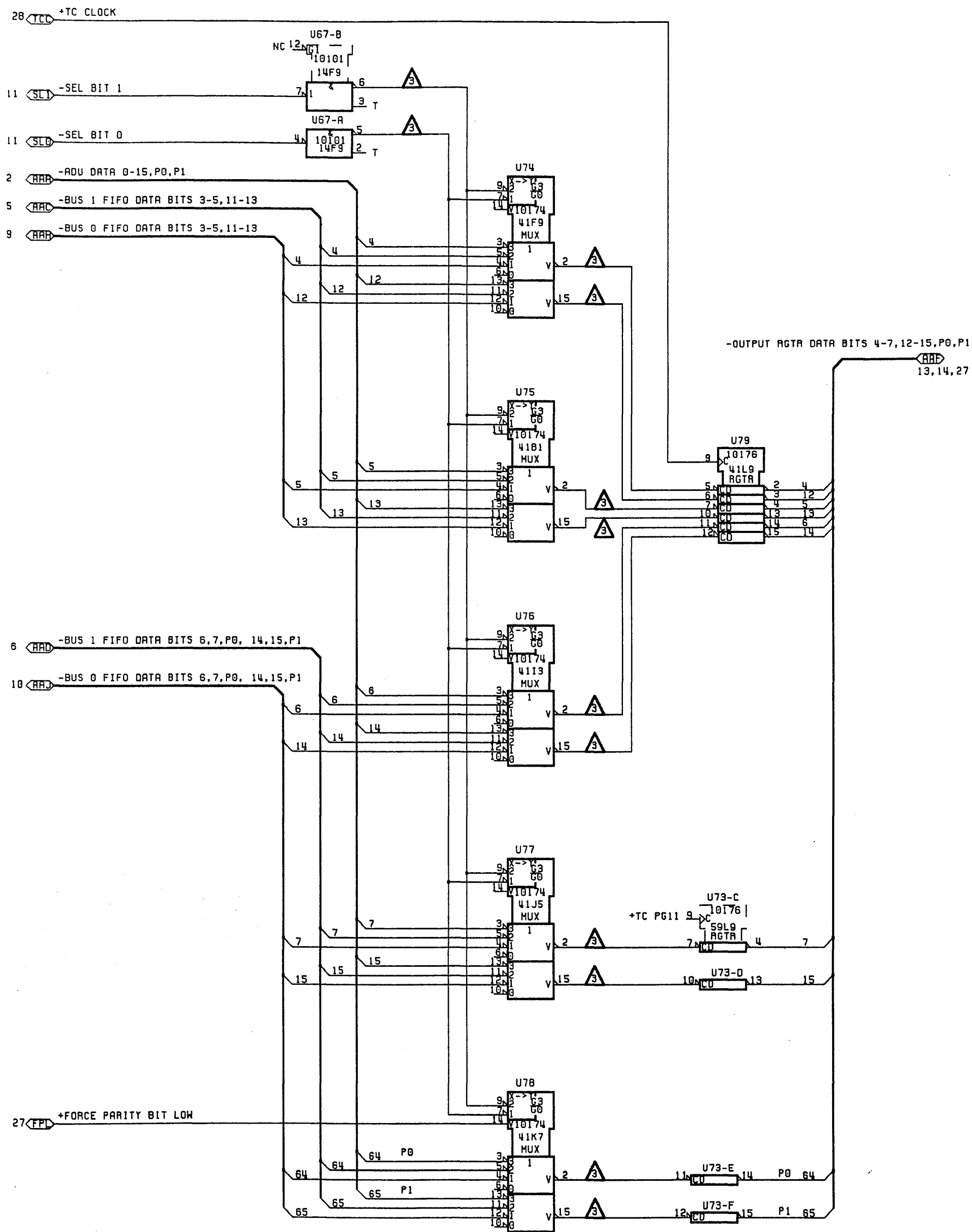


1 NOT TERMINATED ON THIS BOARD
AND 3 INCHES MAXIMUM

△ 6 INCHES MAXIMUM

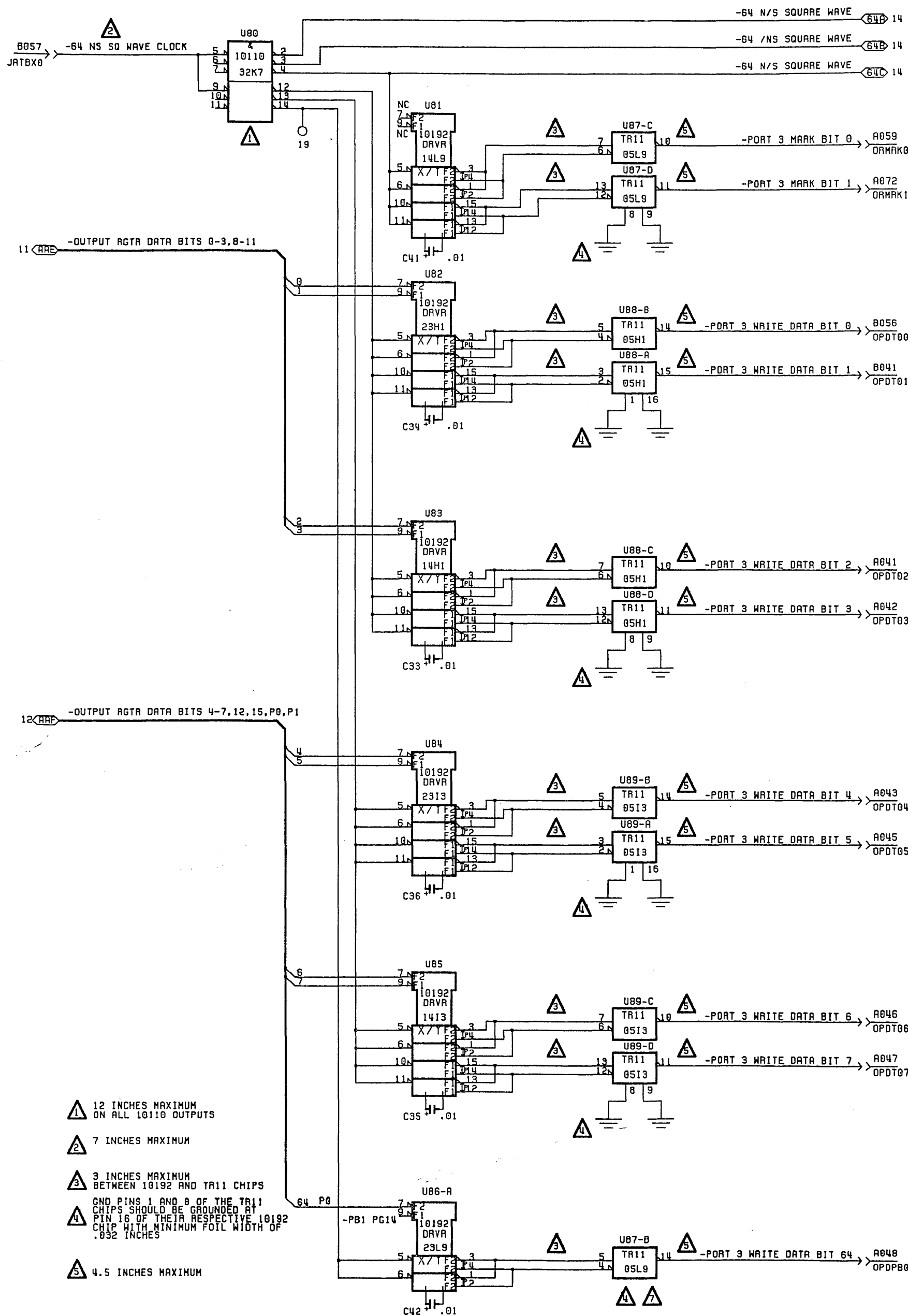
 CONTROL DATA	CMI DATA BOARD CMI OUTPUT DATA MUX AND OUTPUT REGISTER BITS 0-3, 8-11 TYPE 1JHM	B	DWG NO. 22105679	DATE 03/14/86	REV A
		SHEET NO. 11	60462210	PAGE 11	JH-1

CMI OUT DATA MUX AND OUT RGTR BITS 4-7,12-15,PAR 0,1



GD CONTROL DATA	CMI DATA BOARD CMI OUTPUT DATA MUX AND OUTPUT REGISTER BITS 4-7, 12-15, P0, P1 TYPE 1JHH	B	DWG NO.	DATE	REV
			22105679	03/14/86	A
			SHEET NO. 12	60462210	PAGE JH-12

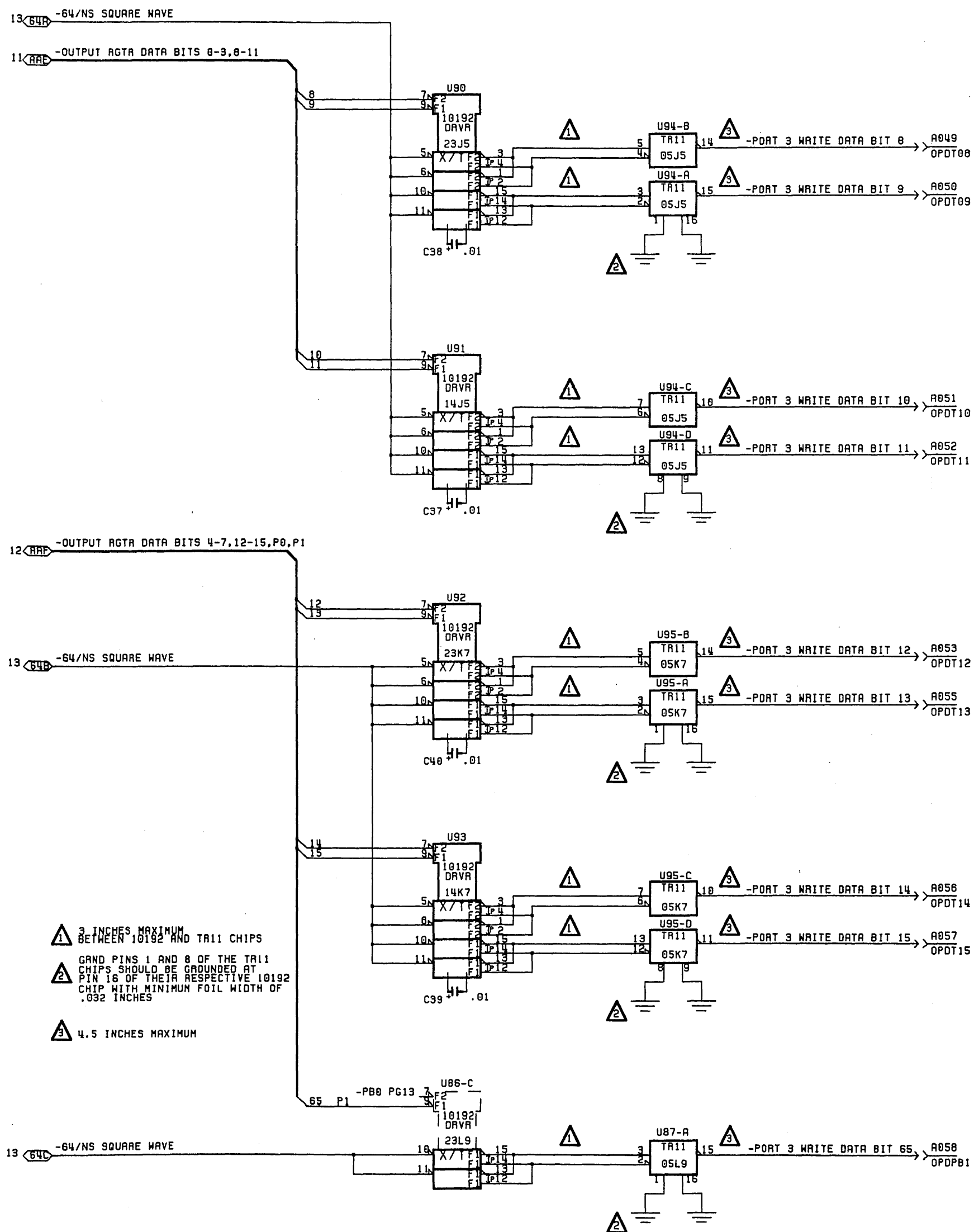
DATA TRANSMITTERS BITS 0-7 & PAR 0



- 1 12 INCHES MAXIMUM ON ALL 10110 OUTPUTS
- 2 7 INCHES MAXIMUM
- 3 3 INCHES MAXIMUM BETWEEN 10192 AND TR11 CHIPS
- 4 GND PINS 1 AND 8 OF THE TR11 CHIPS SHOULD BE GROUNDED AT PIN 16 OF THEIR RESPECTIVE 10192 CHIP WITH MINIMUM FOIL WIDTH OF .032 INCHES
- 5 4.5 INCHES MAXIMUM
- 7 SEE SHEET 14 FOR PINS 1 AND 16 OF THIS CHIP

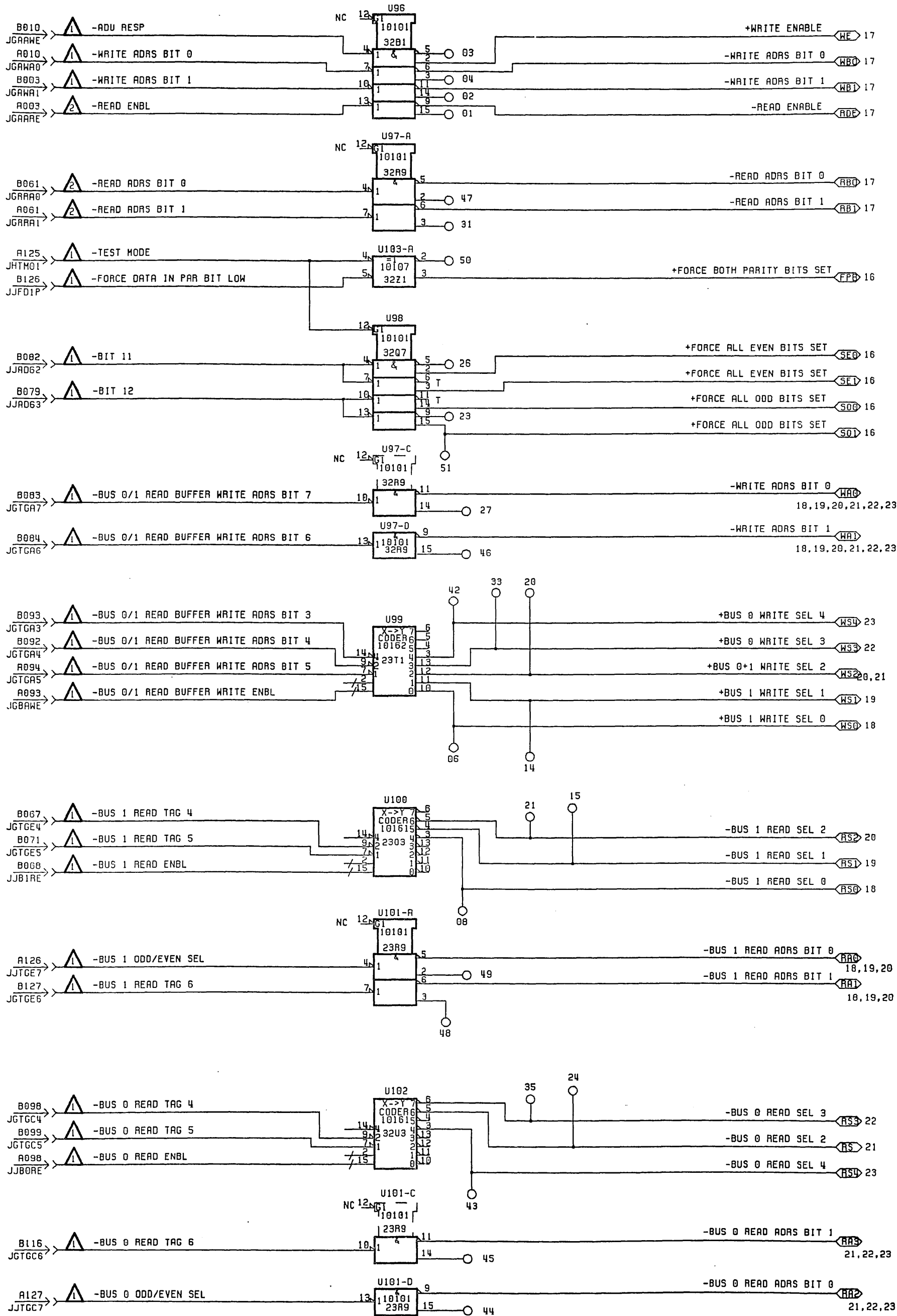
CONTROL DATA	CMI DATA BOARD DATA TRANSMITTERS TO CM BITS 0-7 & P0 TYPE 1JHH		DWG NO. B 22105679	DATE 09/19/86	REV D
			SHEET NO. 13	60462210	PAGE JH-13

DATA TRANSMITTERS BITS 8-15 & PAR 1




	CMI DATA BOARD		DWG NO.	DATE	REV
	DATA TRANSMITTERS TO CM		B	22105679	03/14/86
	BITS 8-15 & P1		SHEET NO. 14	60462210	PAGE 14-14

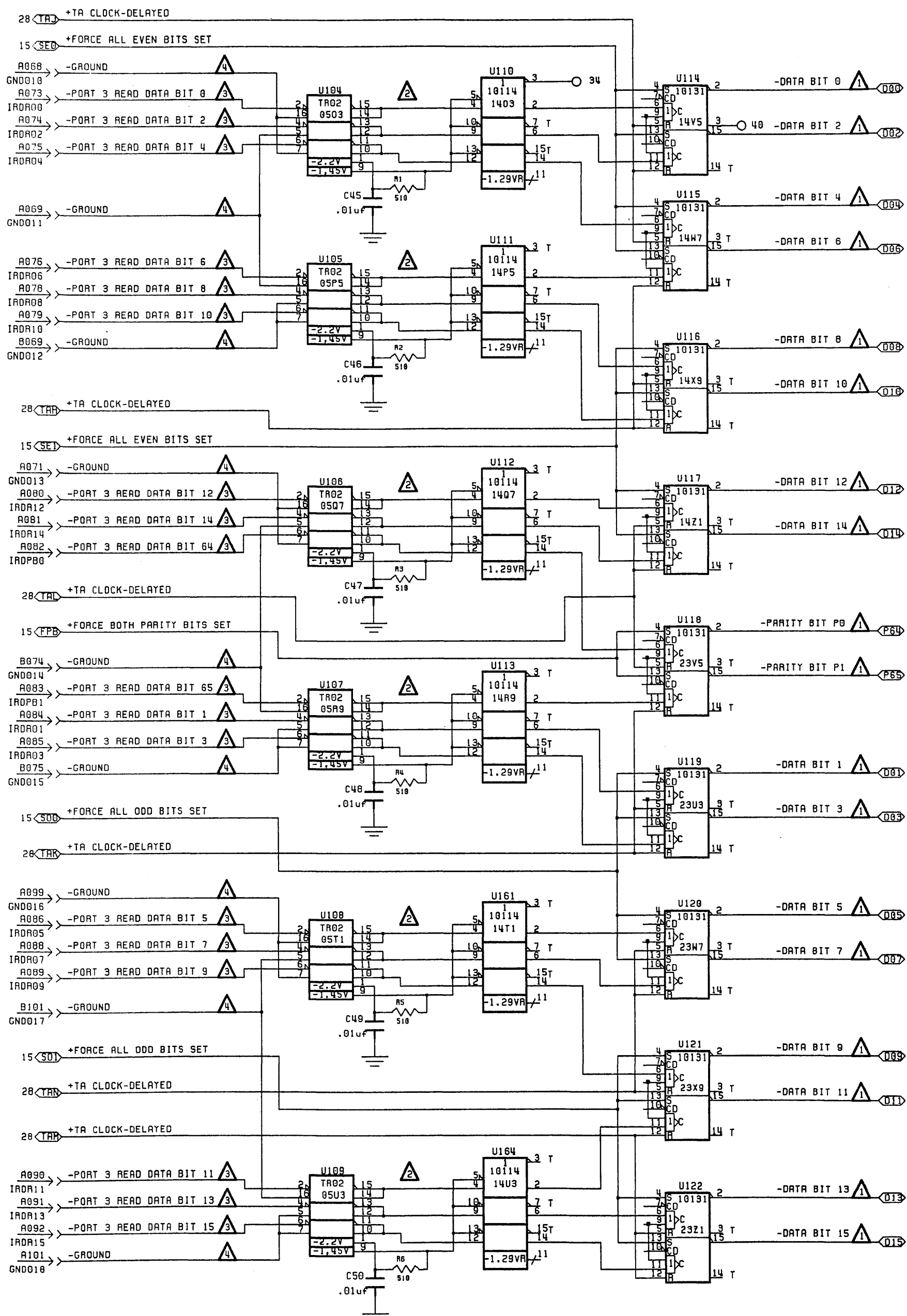
CMI INPUT BUFFER ADRS DECODER AND F/O



- 1 NOT TERMINATED ON THIS BOARD AND 3 INCHES MAXIMUM LENGTH
- 2 6 INCH MAXIMUM LENGTH AND TERMINATE

 CONTROL DATA	CMI DATA BOARD CMI INPUT BUFFER ADDRESS DECODE AND FANOUT TYPE 1JHH	B	DWG NO.	DATE	REV
			22105679	06/10/86	8
			SHEET NO. 15		

CMI READ DATA RECEIVERS AND F/O



1 ALL OUTPUTS FEED PAGES 17, 18, 19, 20, 21, 22, 23

3 4.5 INCH MAX

2 2 INCH MAX BETWEEN TR02 AND 10114 AND NOT TERMINATED.

4 SEPARATE LINES TO CONNECTOR PINS AND PARALLEL TO ASSOCIATED SIGNAL LINE.



CMI DATA BOARD
CMI READ DATA RECEIVERS
AND FANOUT
TYPE 1JHH

B
SHEET NO. 16

DWG NO.
22105679

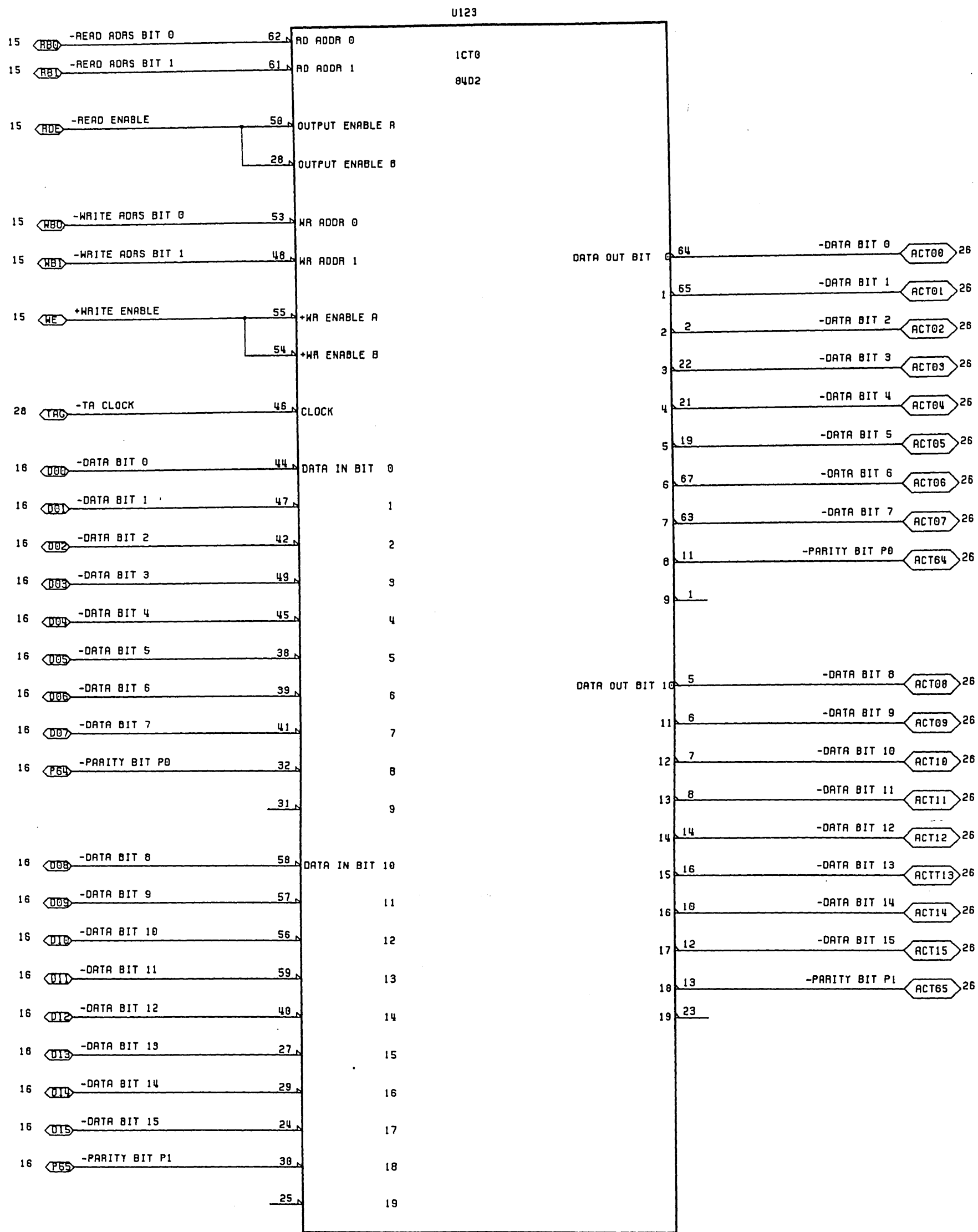
DATE
03/14/86

REV
A

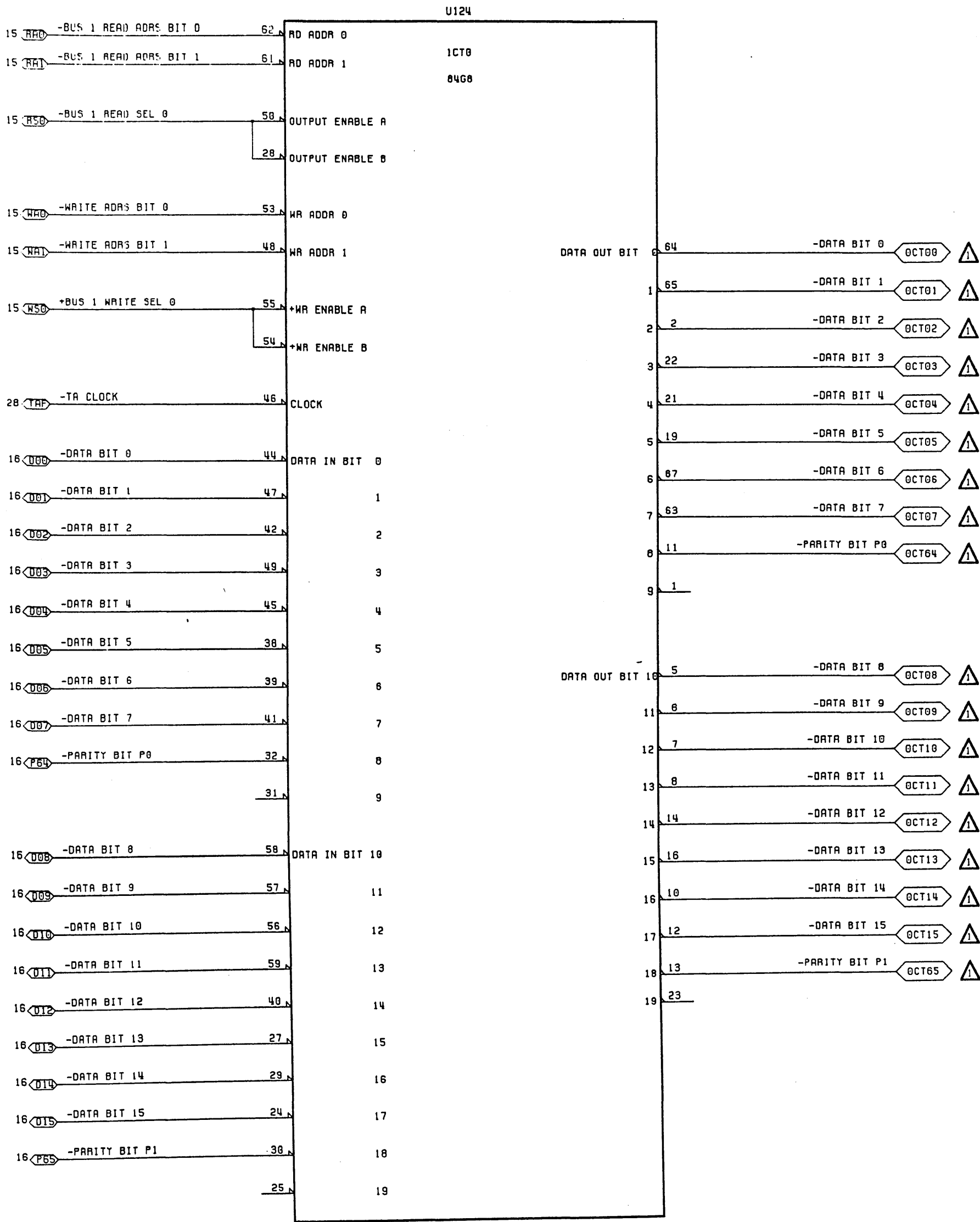
60462210

PAGE
JH-16


ADU CT MACRO CELL INPUT DATA



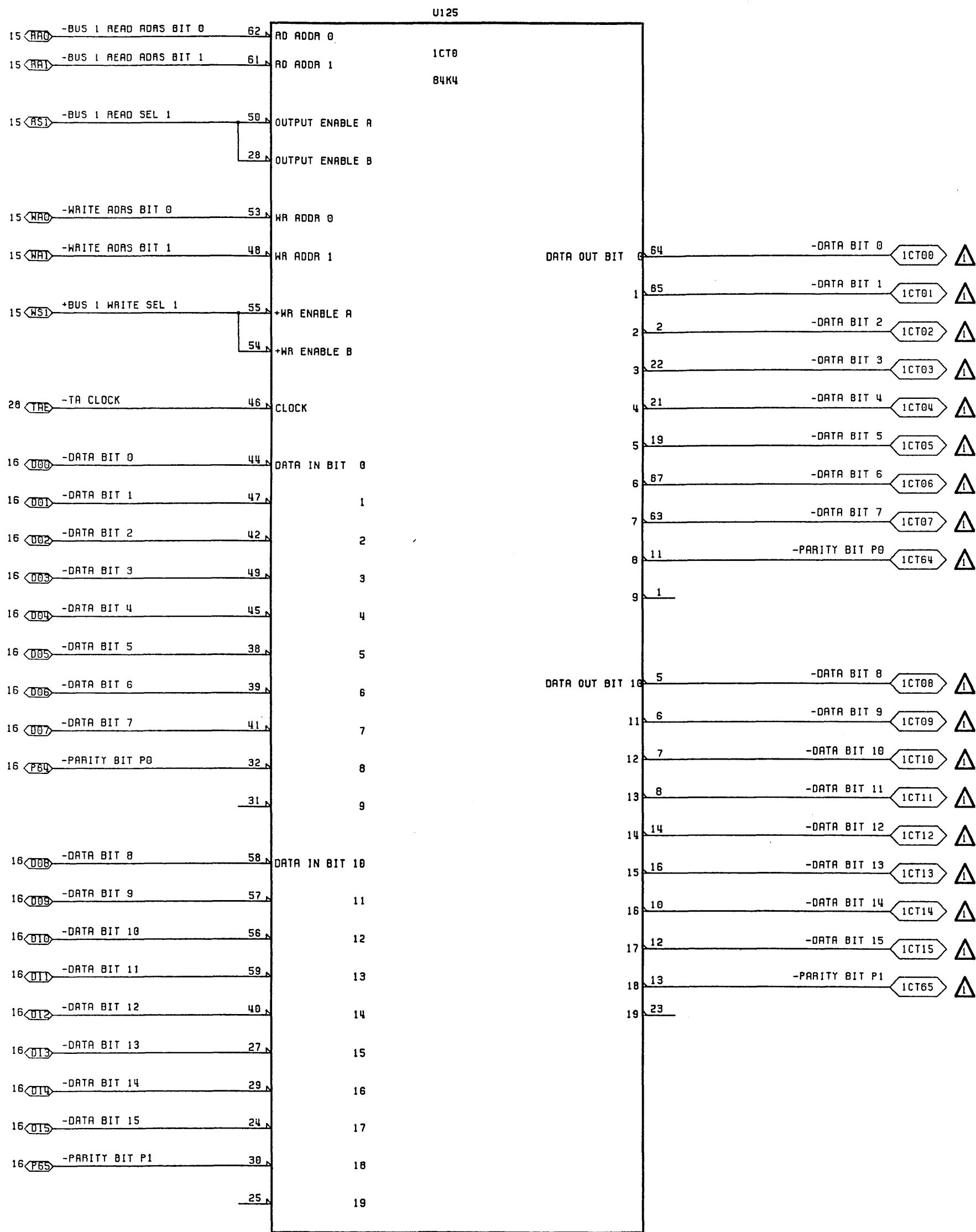
BUS 1 "0" CT MACRO CELL INPUT DATA



1 ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 24

 CONTROL DATA	CMI DATA BOARD BUS 1 "0" CT MACRO CELL INPUT DATA TYPE 1JHH		B	DWG NO. 22105679	DATE 03/14/86	REV A
		N	SHEET NO. 18		60462210	PAGE JH-18

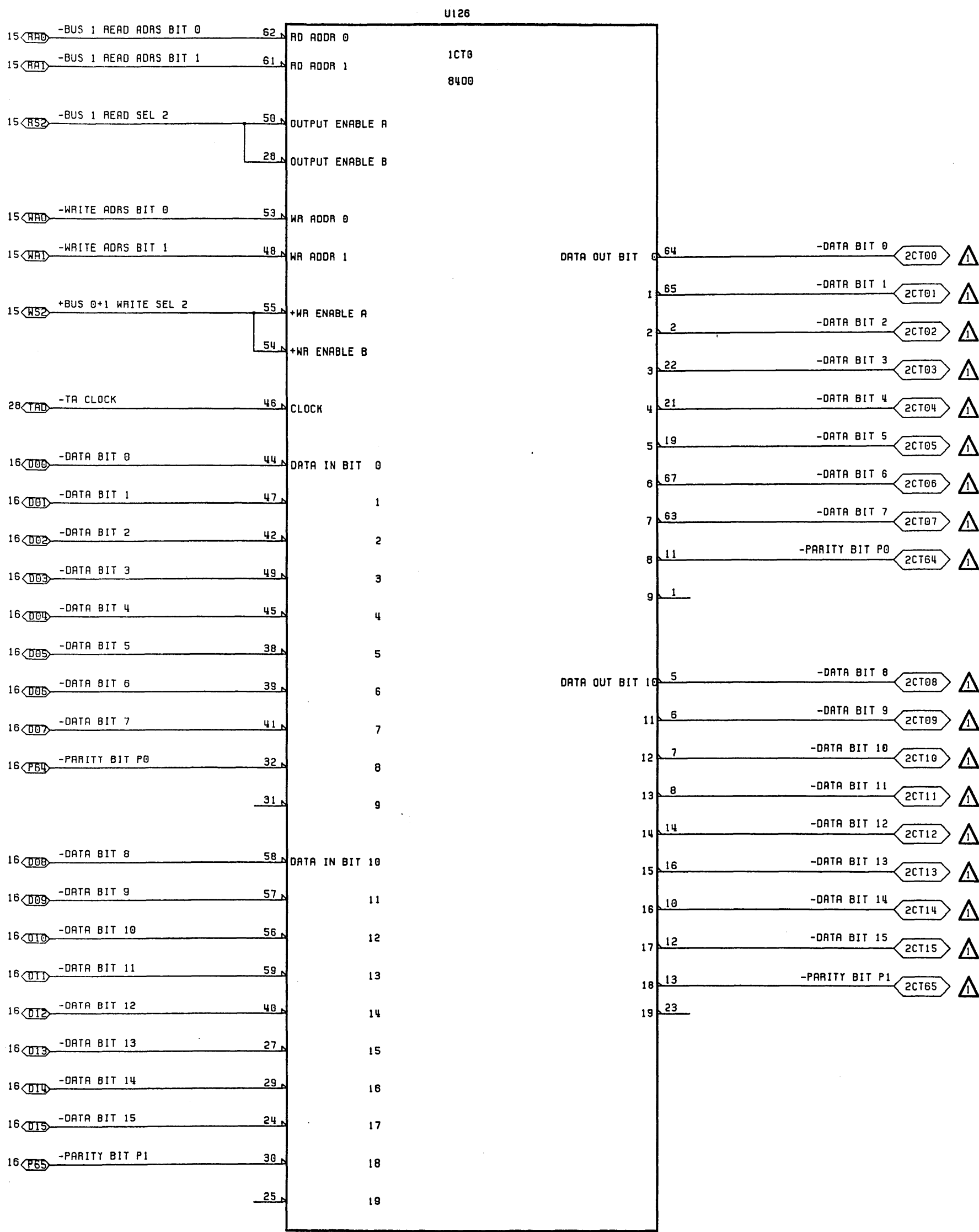
BUS 1 "1" CT MACRO CELL INPUT DATA



ALL OUTPUTS ARE WIRE "AND'ED"
ON PAGE 24

 CONTROL DATA	CMI DATA BOARD BUS 1 "1" CT MACRO CELL INPUT DATA TYPE 1JHH	B	DWG NO.	DATE	REV
			22105679	03/14/86	A
			SHEET NO. 19		

BUS 1 "2" CT MACRO CELL INPUT DATA



1 ALL OUTPUTS ARE WIRE "AND" ON PAGE 24



CMI DATA BOARD
BUS 1 "2" CT MACRO CELL
INPUT DATA
TYPE 1JHH

8

DWG NO.
22105679

DATE
03/14/86

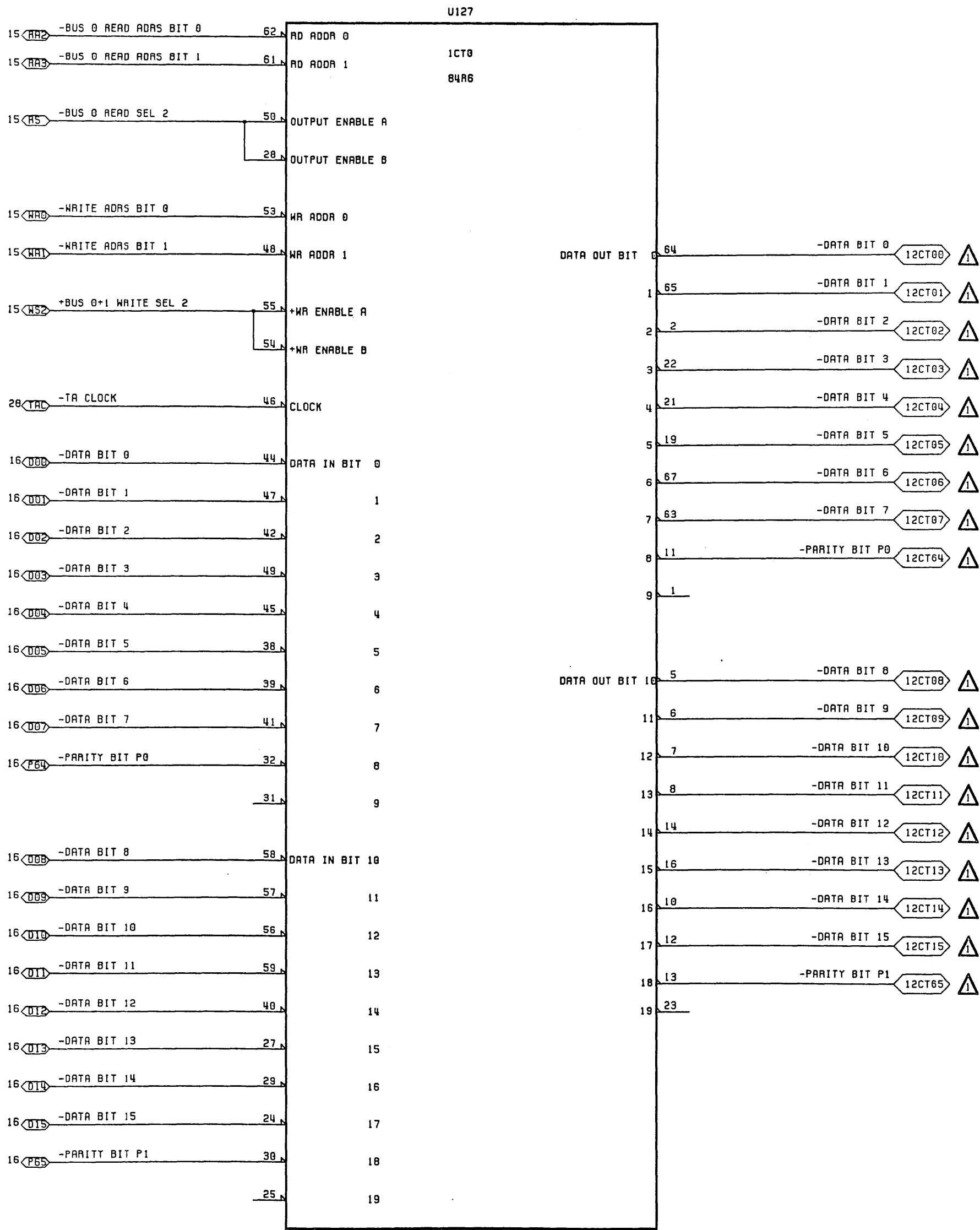
REV
A

SHEET NO. 28

60462210

PAGE JH-20

BUS 0 "2" CT MACRO CELL INPUT DATA



ALL OUTPUTS ARE WIRE "AND"ED"
ON PAGE 25



CMI DATA BOARD
BUS 0 "2" CT MACRO CELL
INPUT DATA
TYPE 1JHH

B

DWG NO.
22105679

DATE
03/14/86

REV
A

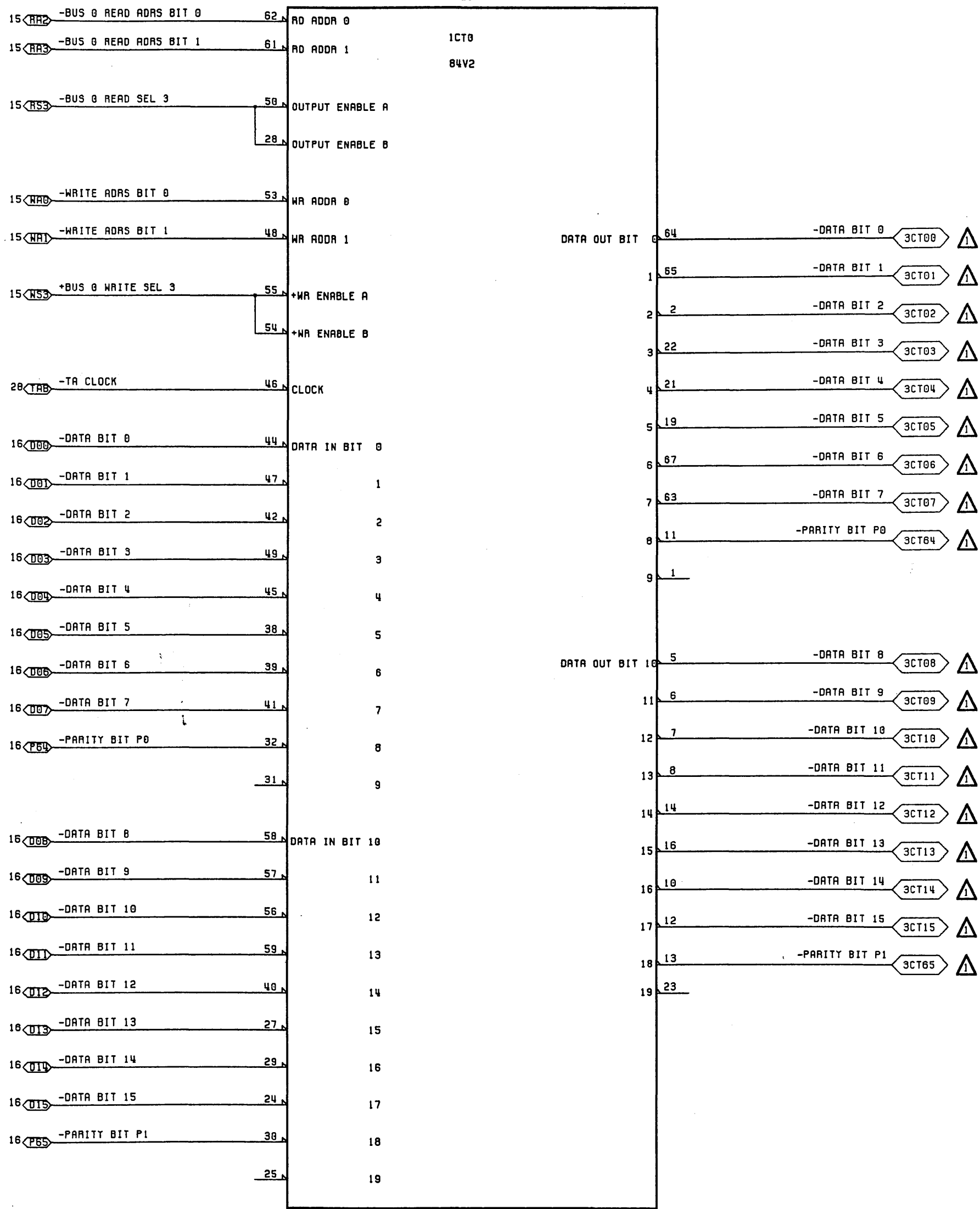
SHEET NO. 21

60462210


PAGE JH-21

BUS 0 "3" CT MACRO CELL INPUT DATA

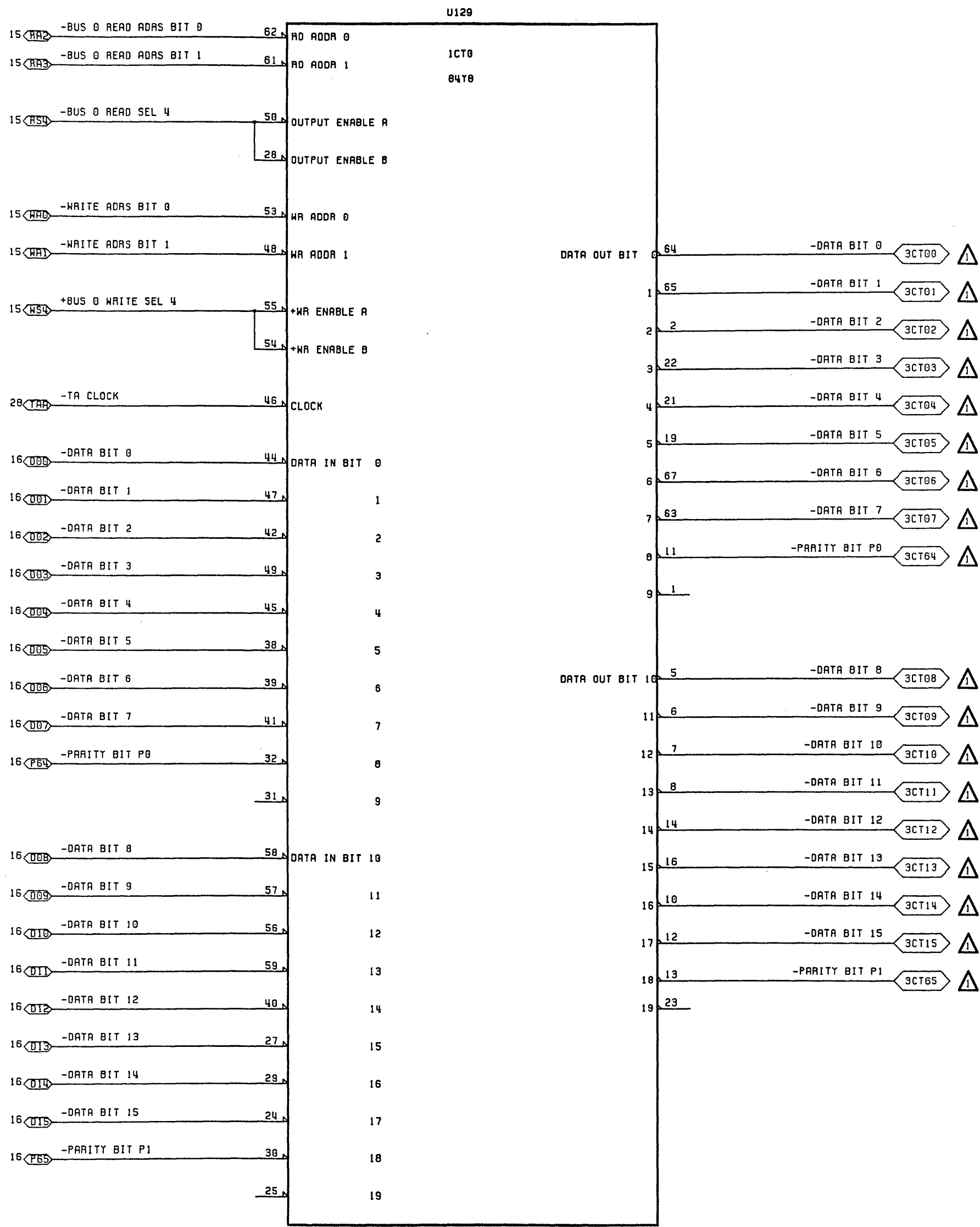
U128



ALL OUTPUTS ARE WIRE "ANDED" ON PAGE 25

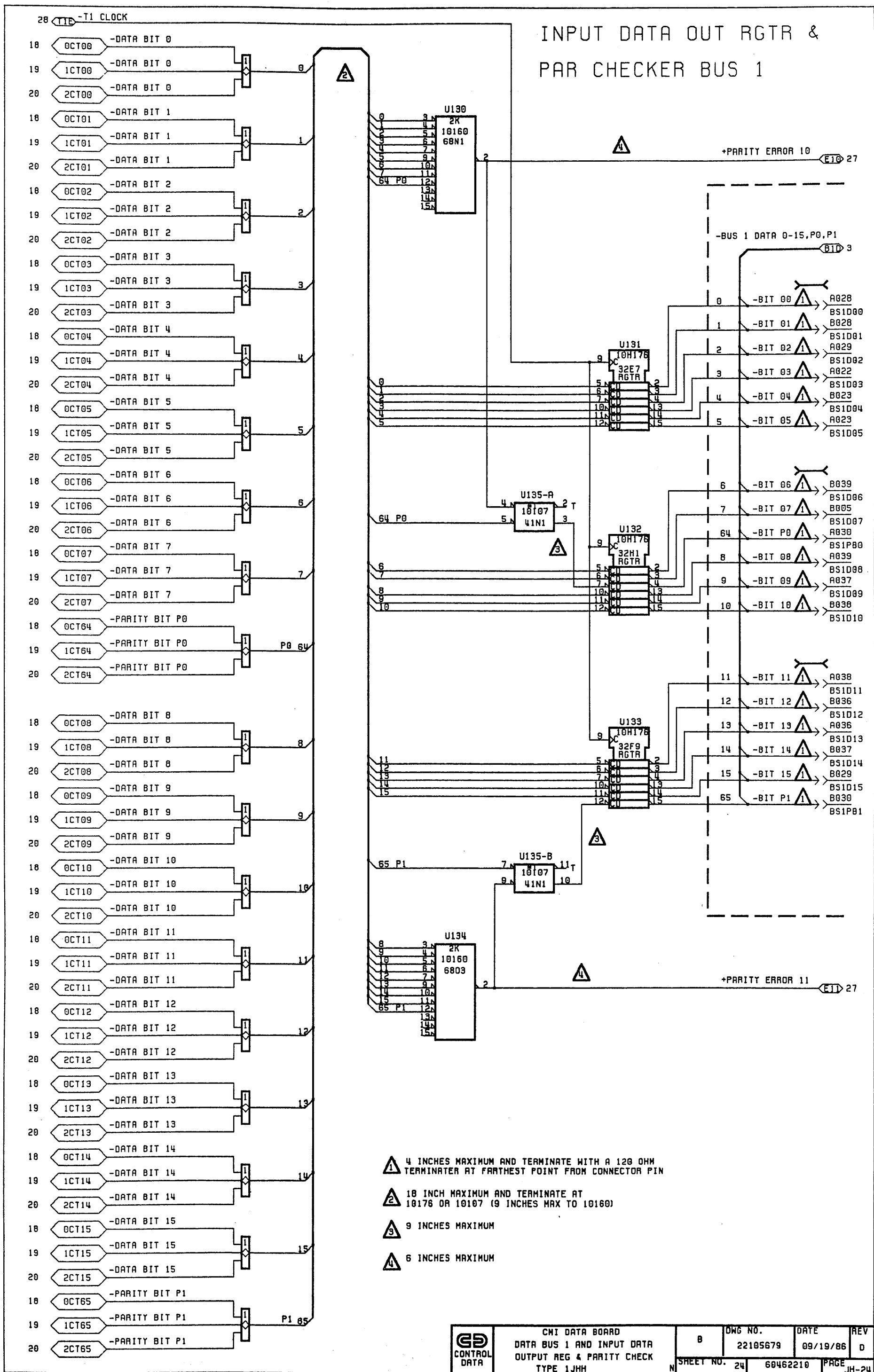
 CONTROL DATA	CMI DATA BOARD BUS 0 "3" CT MACRO CELL INPUT DATA TYPE 1JHM			B	DWG NO. 22105679	DATE 03/14/86	REV A
					SHEET NO. 22	60462210	PAGE JH-22

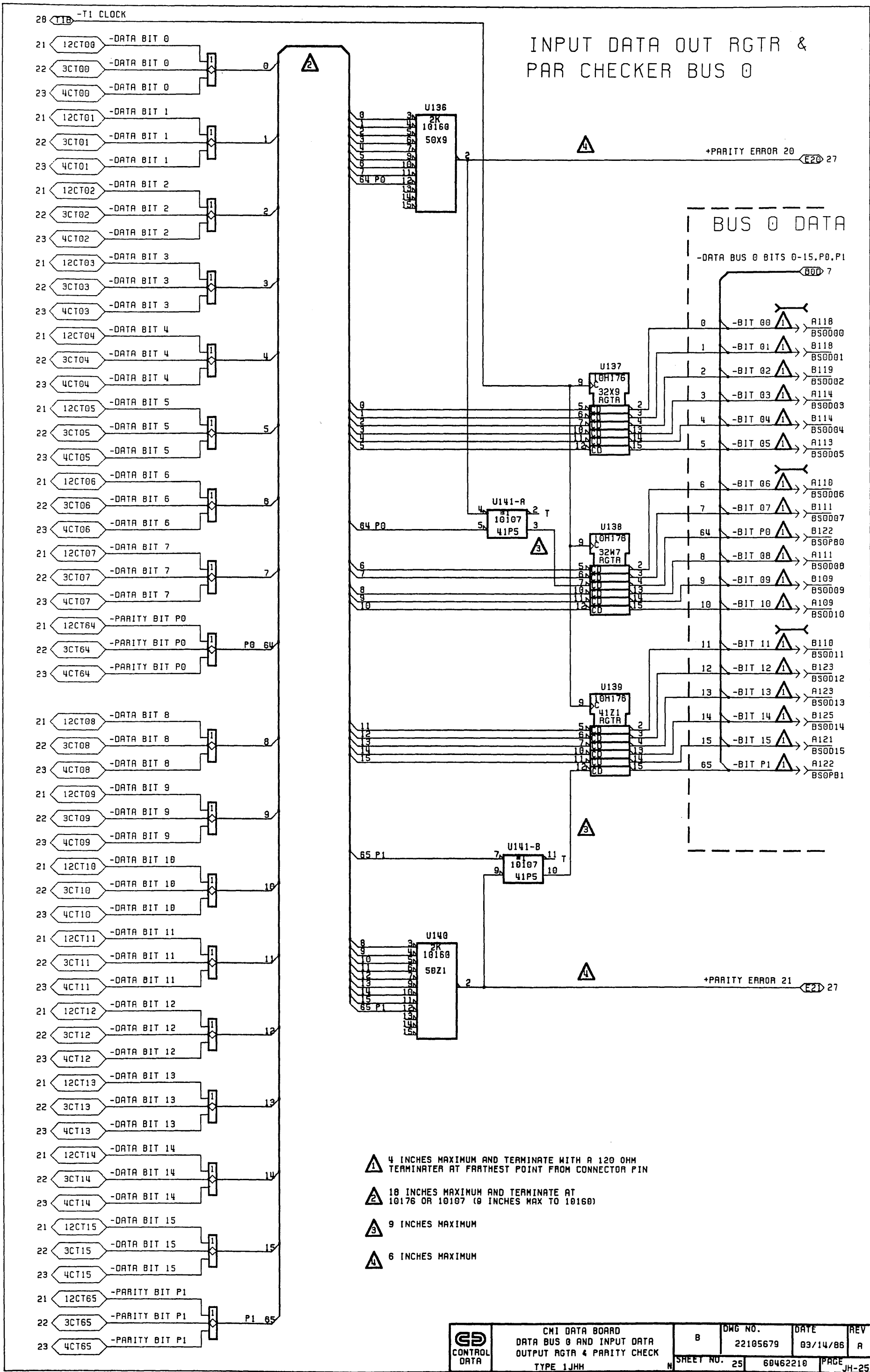
BUS 0 "4" CT MACRO CELL INPUT DATA



ALL OUTPUTS ARE WIRE "ANDED"
ON PAGE 25

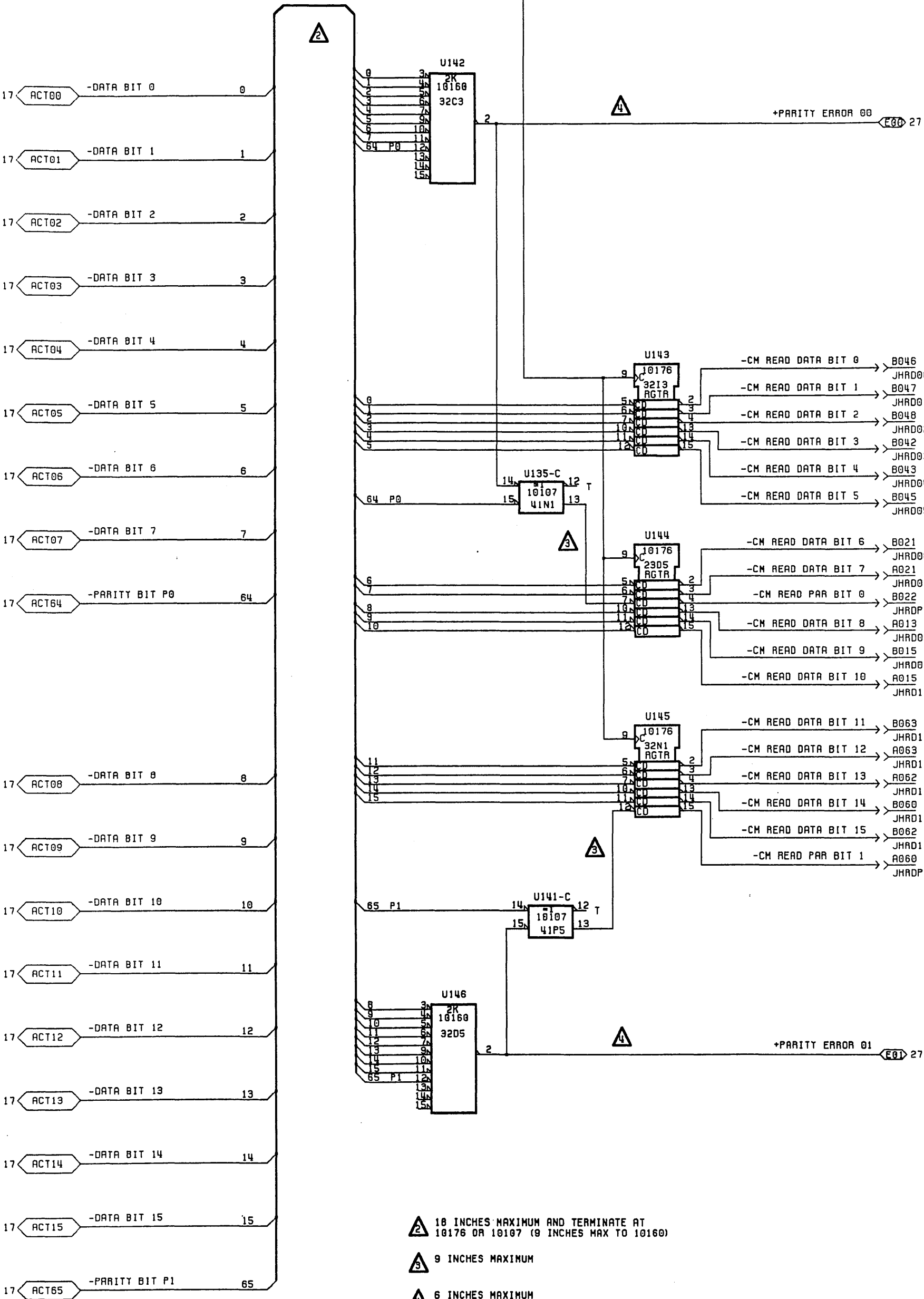
CD CONTROL DATA	CMJ DATA BOARD BUS 0 "4" CT MACRO CELL INPUT DATA TYPE 1JMH	B	DWG NO. 22105679	DATE 03/14/86	REV A
			SHEET NO. 23	60462210	PAGE JH-23






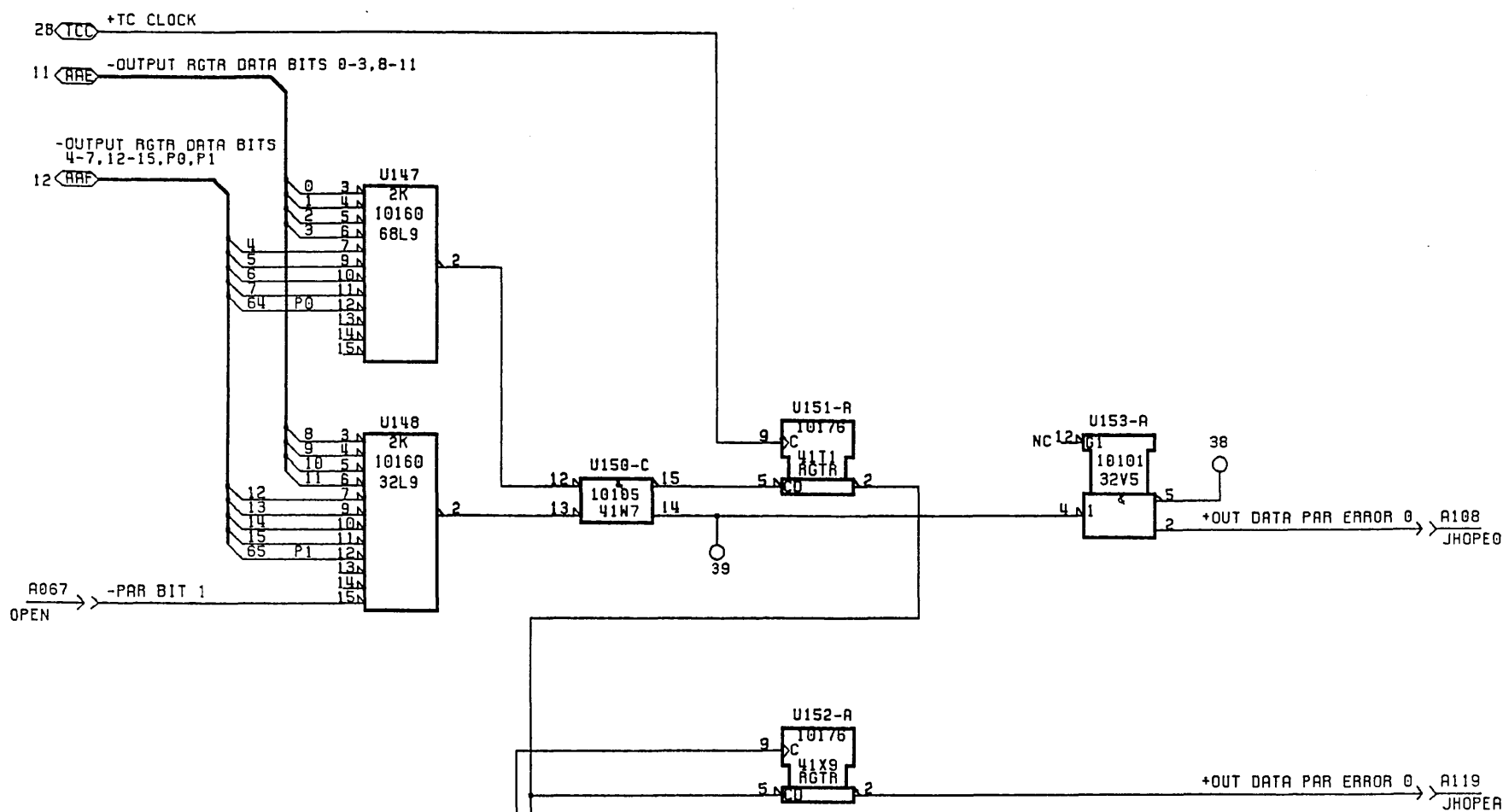
INPUT DATA OUT RGTRS & PAR CHECKER AND ADU DATA OUT

28 TTD -T1 CLOCK

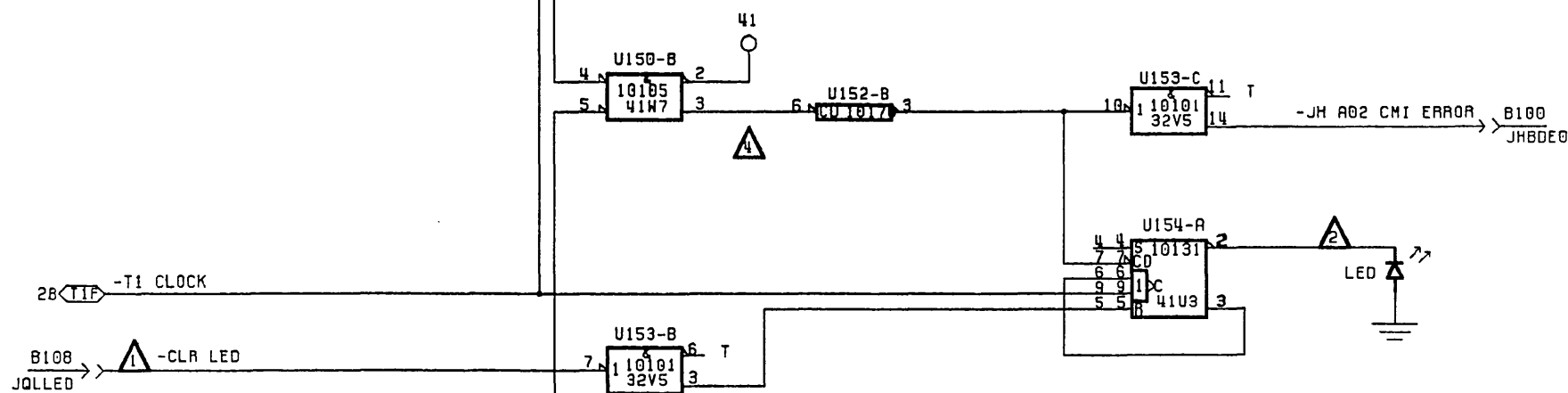


 CONTROL DATA	CMI DATA BOARD		B	DWG NO.	DATE	REV	
	ADU DATA AND INPUT DATA			22105679	03/14/86	A	
	OUTPUT REGISTER & PARITY CHECK						
	TYPE 1JHH						
			N	SHEET NO. 26	60462210	PAGE	JH-26

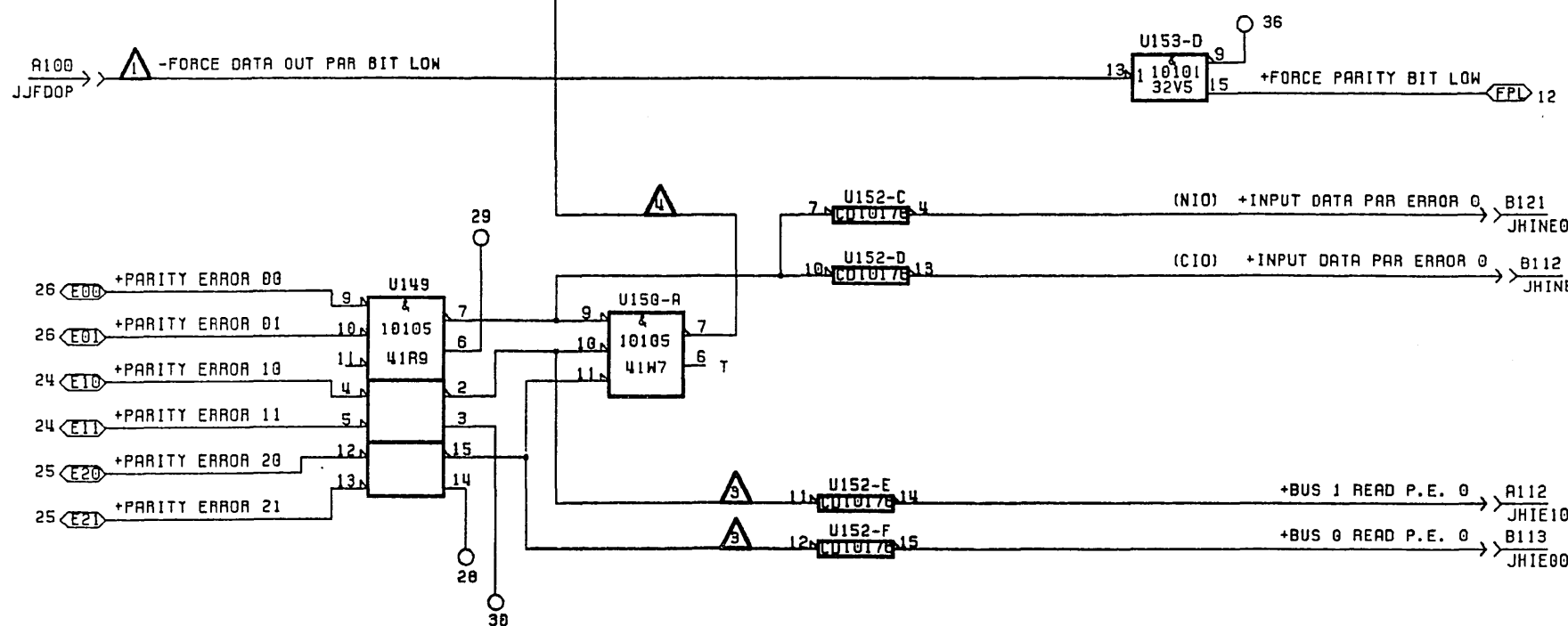
OUT DATA PAR CHECKER




ERROR LED



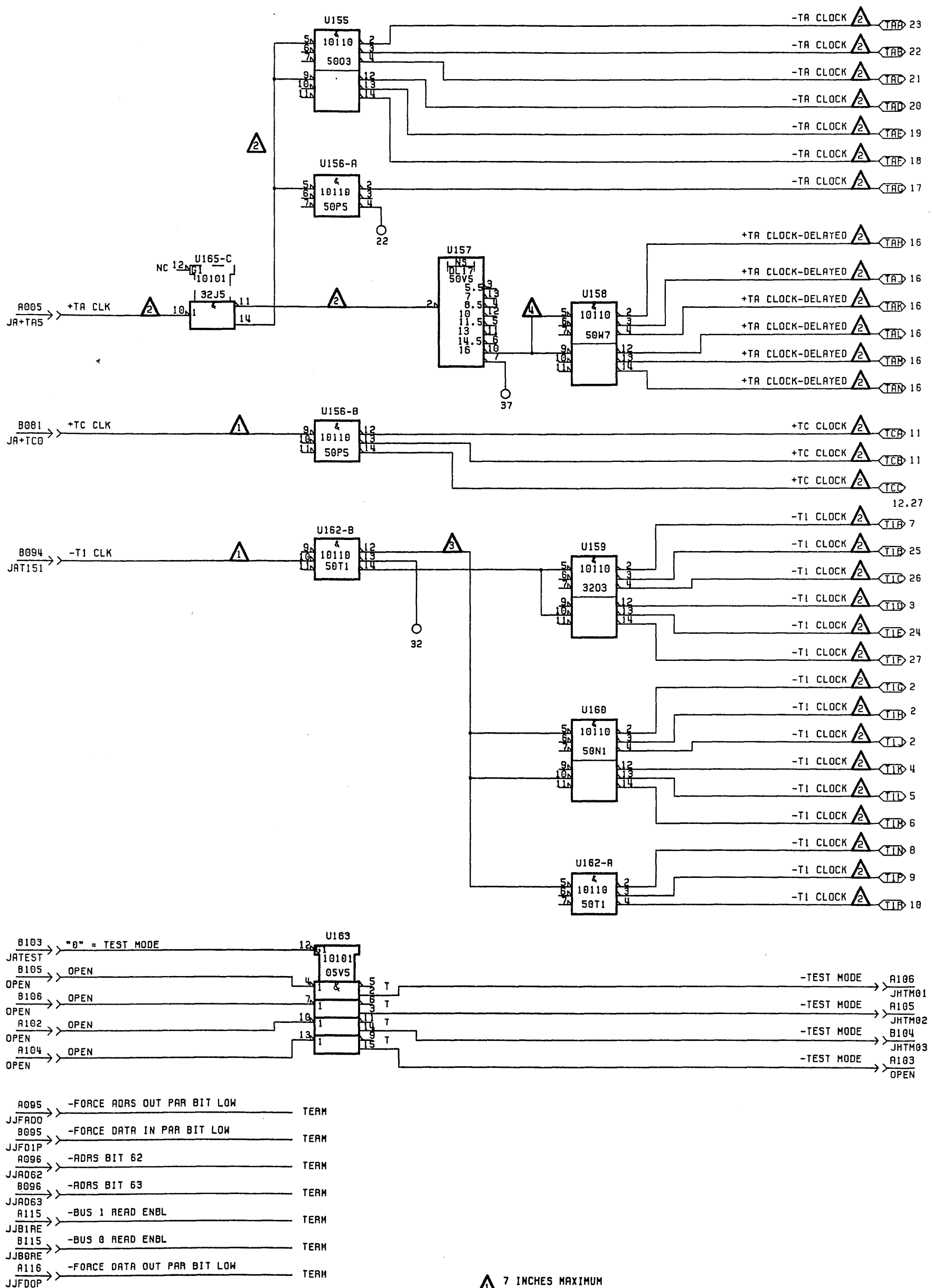
INPUT DATA PAR CHECKER



- 1 NOT TERMINATED ON THIS BOARD AND 6 INCHES MAXIMUM
2 TERMINATE
3 6 INCHES MAXIMUM
4 3 INCHES MAXIMUM

 CONTROL DATA	CMI DATA BOARD INPUT/OUTPUT PARITY CHECK AND ERROR LED TYPE 1JHH	8	DWG NO. 22105679	DATE 09/19/86	REV D
SHEET NO. 27		60462210		PAGE JH-27	


CLK F/O



CMI DATA BOARD CONTROL DATA	CLOCK FANOUT TYPE 1JHH	B	DWG NO. 22105679	DATE 03/14/86	REV A
			SHEET NO. 28	60462210	PAGE JH-28

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	15	+RD ENABLE ADU IN	27	15	+WR ADRS BIT0 BUS IN
02	15	+WRT ADRS BT0 ADU IN	28	27	-BUS0 DATA OUT ERROR
03	15	-WRT ENABLE ADU IN	29	27	-ADU DATA OUT ERROR
04	15	+WRT ADRS BT0 ADU IN	30	27	-BUS1 DATA OUT ERROR
05	11	+SEL BIT 0	31	15	+RD ADRS BIT2 ADU IN
06	15	+BUS 1 WRITE SEL 0	32	28	-T1 CLOCK
07	11	+SEL BIT 1	33	15	+BUS 0 WRITE SEL 3
08	15	-BUS 1 READ SEL 0	34		
09	03	-DATA BIT 0 BUS1 OUT	35	15	-BUS 0 READ SEL 3
10	02	-DATA BIT 0 ADU-CMI	36	27	-FRC DATAOUT PBS LOW
11	04	-DATA BIT 0 BUS1 CMI	37	28	+TA CLOCK
12	08	-DATA BIT 0 BUS0 OUT	38	27	-DATA OUTPUT ERROR
13	02	-DATA BIT 0 ADU OUT	39	27	-DATA OUTPUT ERROR
14	15	+BUS 1 WRITE SEL 1	40		
15	15	-BUS 1 READ SEL 1	41	27	+BOARD ERROR
16	03	-ADRS BIT 0 BUS1 OUT	42	15	+BUS 0 WRITE SEL 4
17	11	-DATA BIT 0 CMI-CMC	43	15	-BUS 0 READ SEL 4
18	11	-DATA BIT 0 OUT MUX	44	15	+RD ADR BIT0 BUS0 IN
19	13	-64 ns SQUARE WAVE	45	15	+RD ADR BIT1 BUS0 IN
20	15	+BUS 0+1 WRT SEL 2	46	15	+WR ADRS BIT1 BUS IN
21	15	-BUS 1 READ SEL 2	47	15	+RD ADRS BIT0 ADU IN
22	28	-TC CLOCK	48	15	+RD ADR BIT1 BUS1 IN
23	15	-FORCE ODD BITS SET	49	15	+RD ADR BIT0 BUS1 IN
24	15	-BUS 0 READ SEL 2	50	15	+FRC DATA IN PBS LOW
25	07	-DATA BIT 0 BUS0-CMI	51	15	-FORCE ODD BITS SET
26	15	-FORCE EVEN BITS SET			

CONNECTOR PINS	
GND	B011, A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117, A120, B120, A128, B049, B050, B051, B052, B053, A054, B054, B055, A077, B077, A097, B097, B102
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A070, B070 [NOT USED]
TERM	A095, B095, A096, B096, A115, B115, A116
UNUSED	A040, B040, A128
ISOLATED GROUND	B011, B049, B050, B051, B052, B053, B055, A068, A069, B069, A071, B074, B075, A099, A101, B101, B102, A120, B120

 CONTROL DATA	CHI DATA BOARD TESTPOINTS & SIGNAL NAMES AND CONNECTOR PINS TYPE 1JHH	B	DWG NO.	DATE	REV
			22105679	09/19/86	D
			SHEET NO. 29	60462210	PAGE

CAUTION

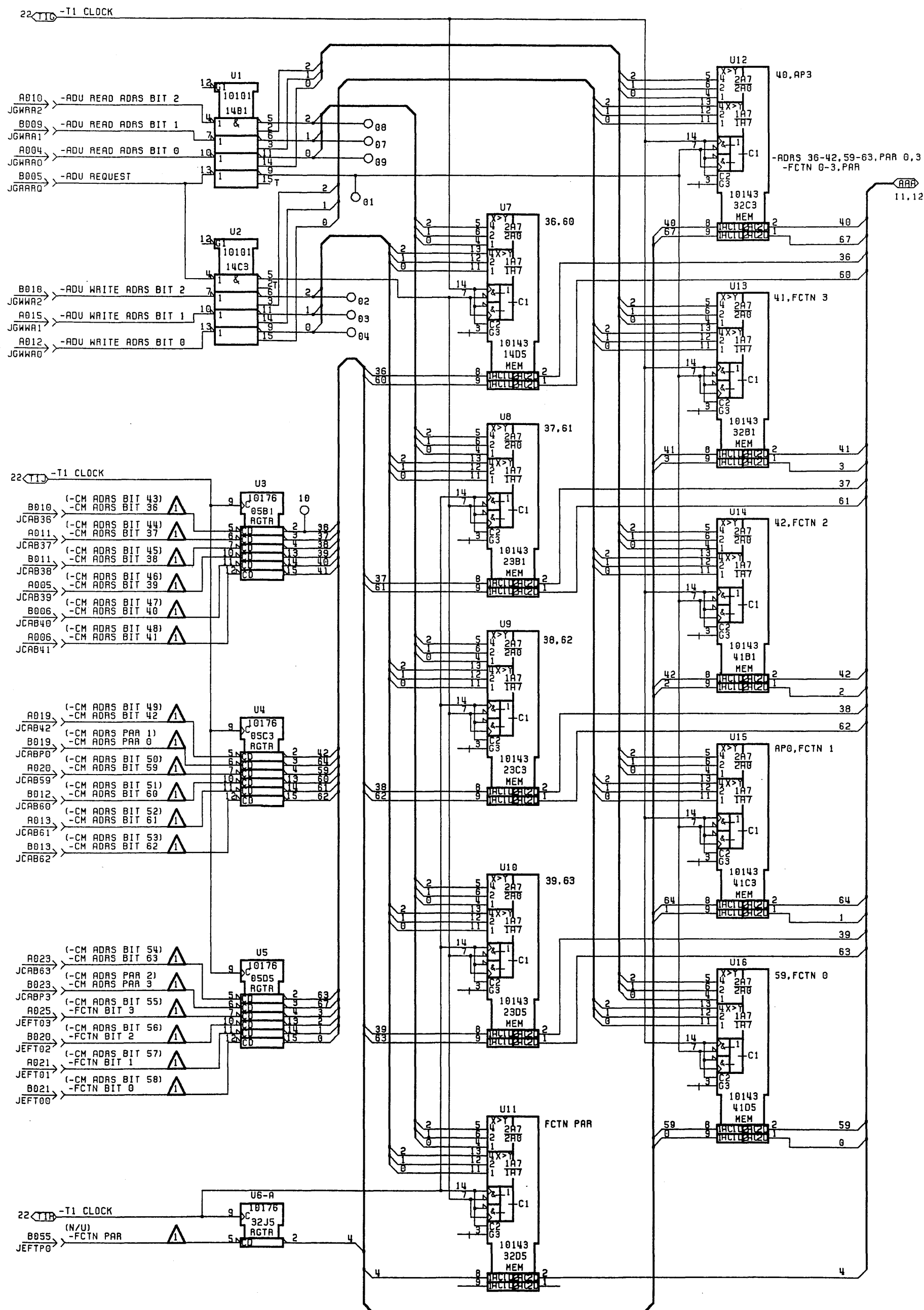
There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

CMI ADRS BOARD


NOTE: THIS BOARD MAY NOT FUNCTION
WHEN EXTENDED
LOC: A06,A07

 CONTROL DATA	REVISION HISTORY	B	DWG NO.	DATE	REV	
			53575508	07/18/86	D	
	TYPE 1JJH					
		N	SHEET NO.	1	60462210	PAGE
						11-01

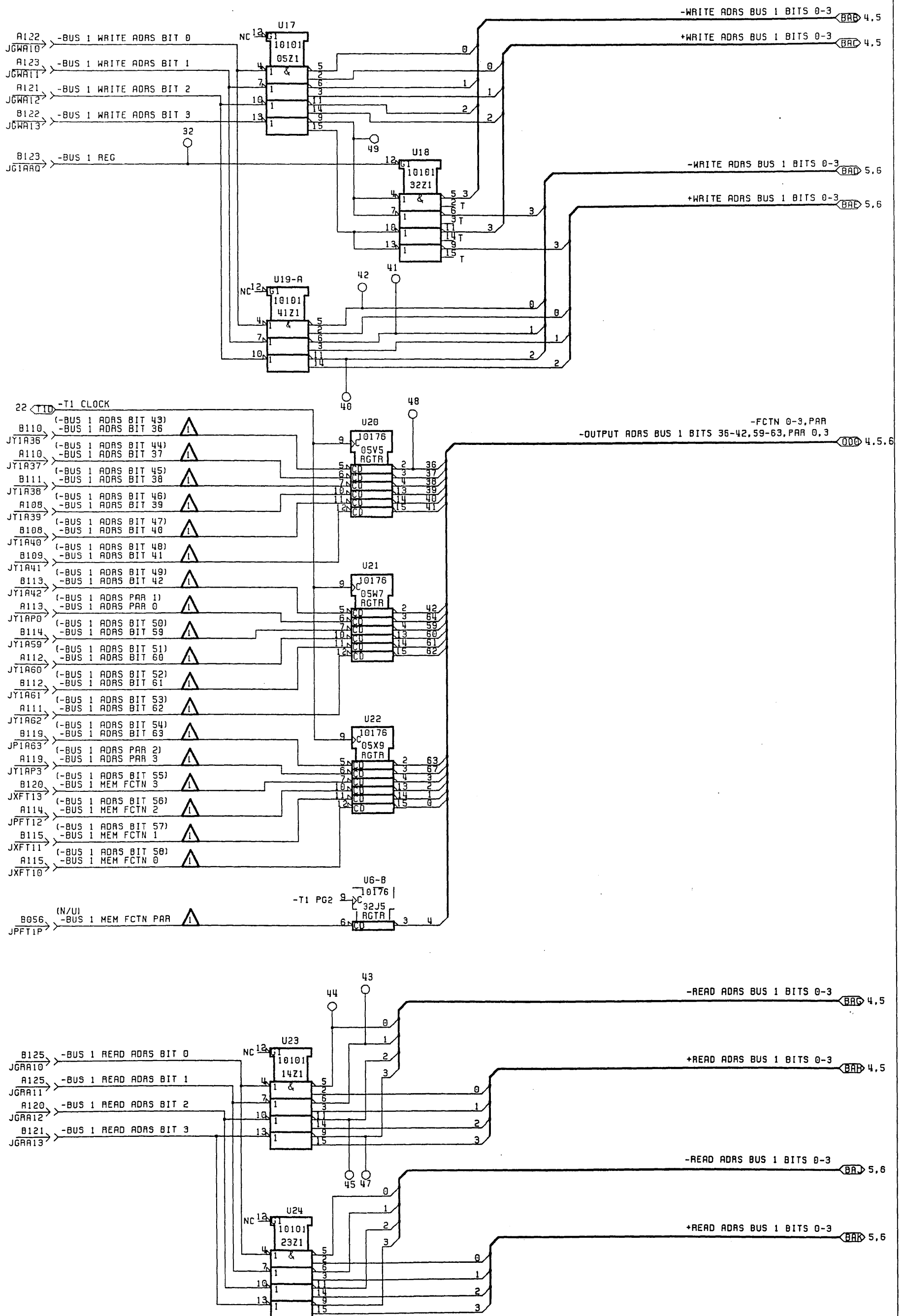
CM ADU ADRS BUFFER BITS 36-42,59-63,PAR 0,3 & MEM FCTN BITS 0-3,PAR



△ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	CM ADU ADDRESS BUFFER. ADDRESS BITS 36-42,59-63,PARITY 0,3		B	DWG NO. 53575508	DATE 11/01/85	REV A
	MEMORY FUNCTION BITS 0-3,PARITY					
	TYPE 1JJH					
SHEET NO. 2			60462210		PAGE JJ-02	

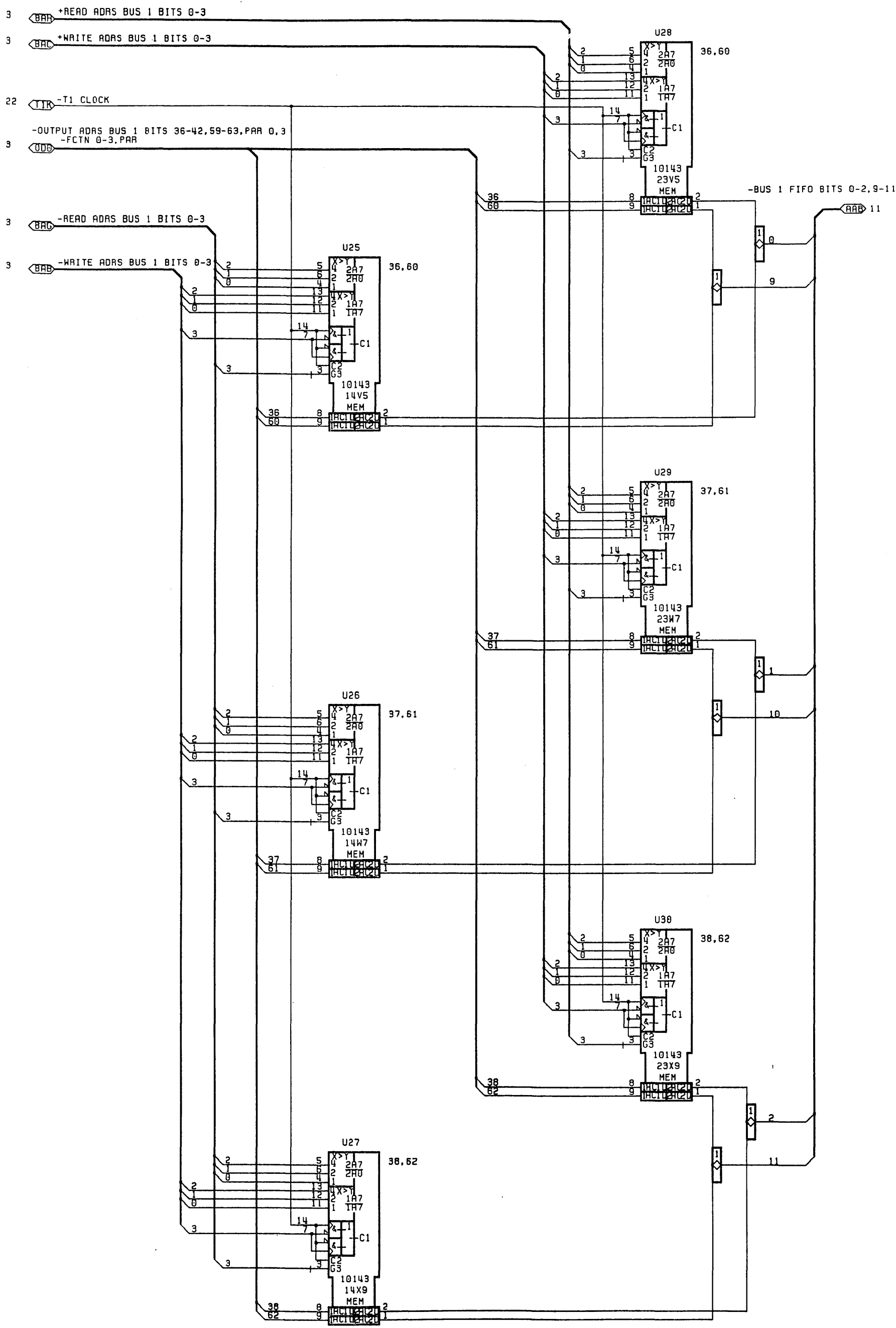
BUS 1. ADRES INPUT RGTR



 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

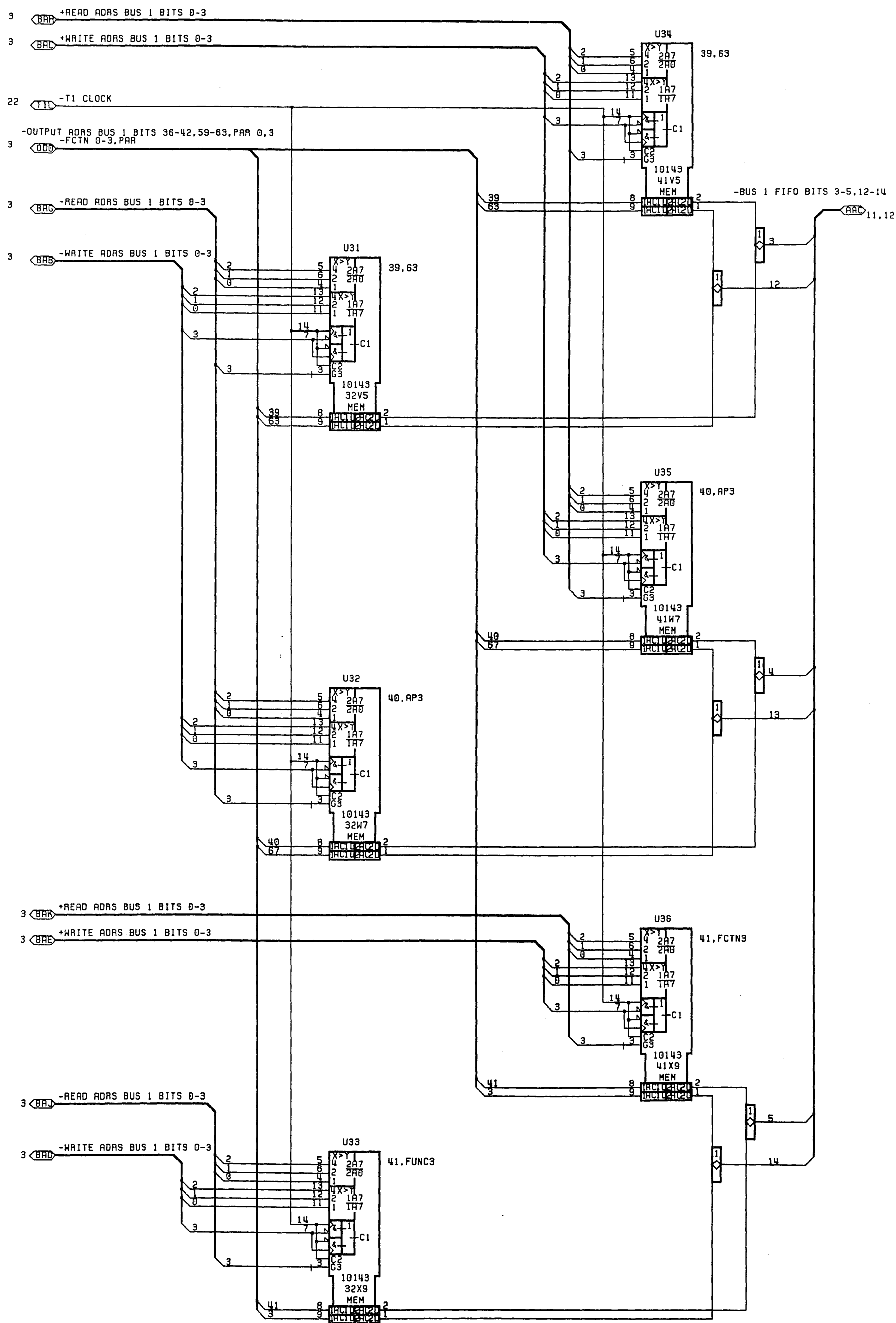
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	TYPE 1JJH		53575508	11/01/85	A
		N	SHEET NO. 3	60462210	PAGE 11-03

CMI FIFO BUS 1 BITS 0-2,9-11, CM WRITE, CM ADRS



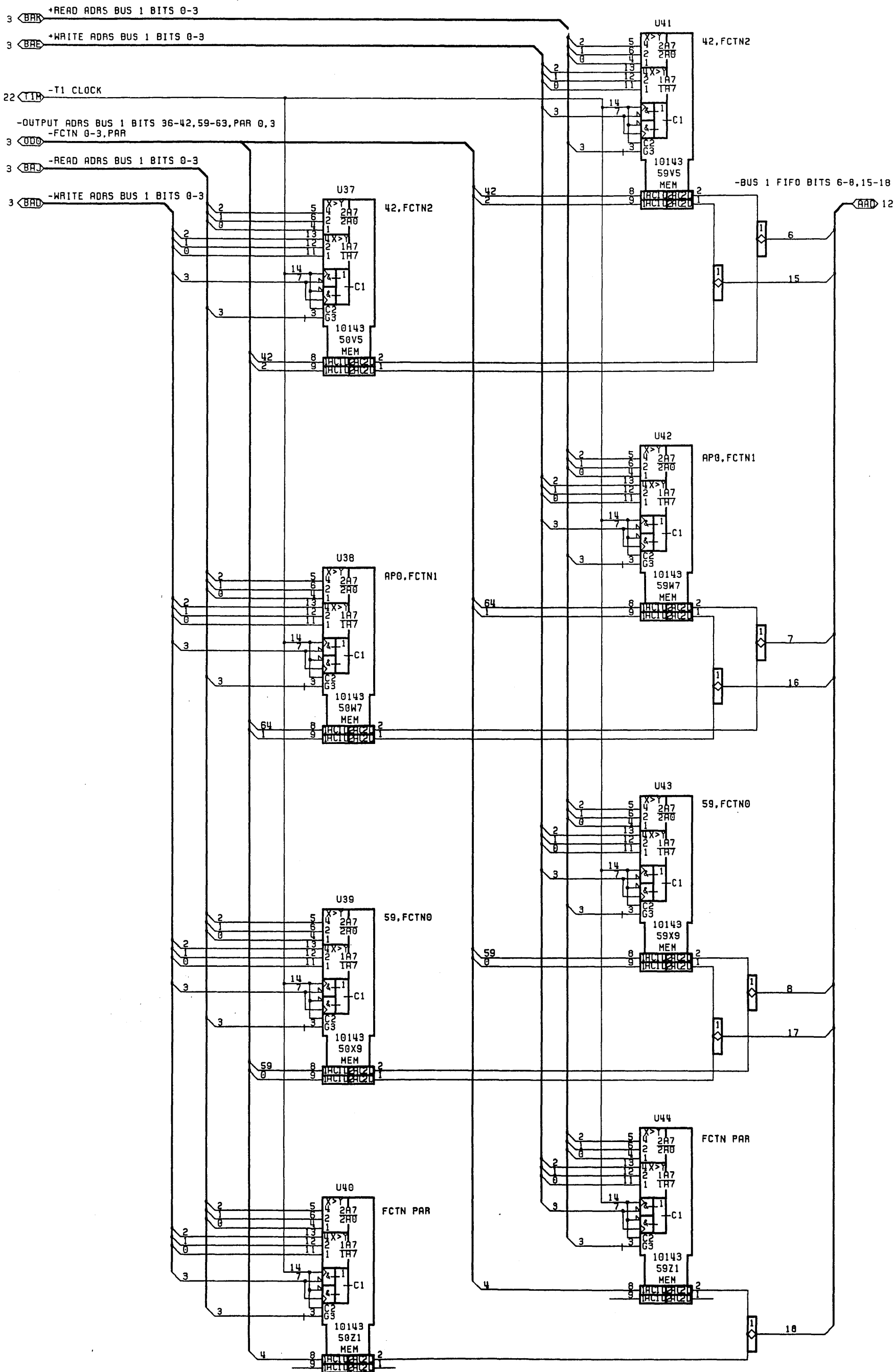
CONTROL DATA	CMI FIFO BUS 1 BITS 0-2,9-11. CM WRITE CM ADDRESS TYPE 1JJH	B	DWG NO.	DATE	REV
			53575508	11/01/85	A
			SHEET NO. 4	60462210	PAGE JJ-04


CMI FIFO BUS 1 BITS 3-5,12-14, CM ADRS/FCTN



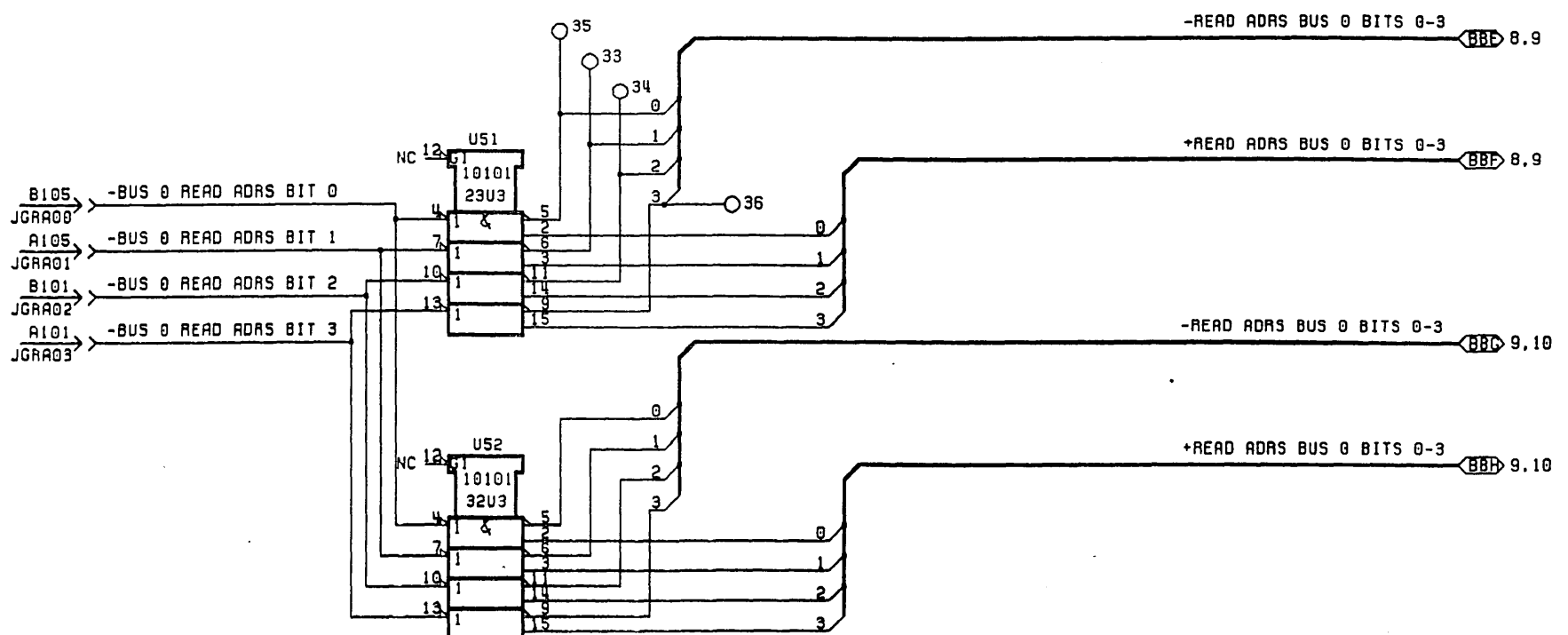
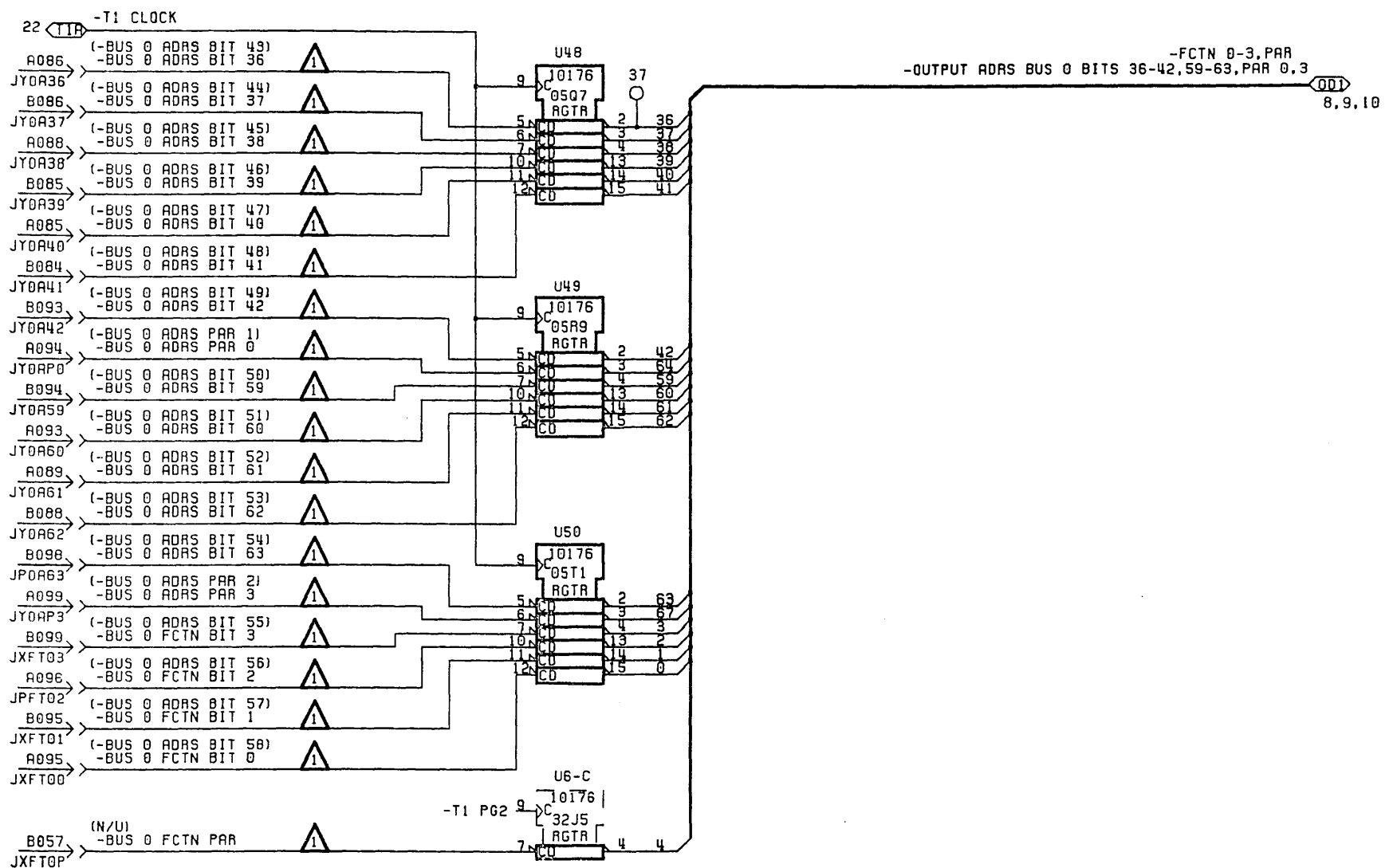
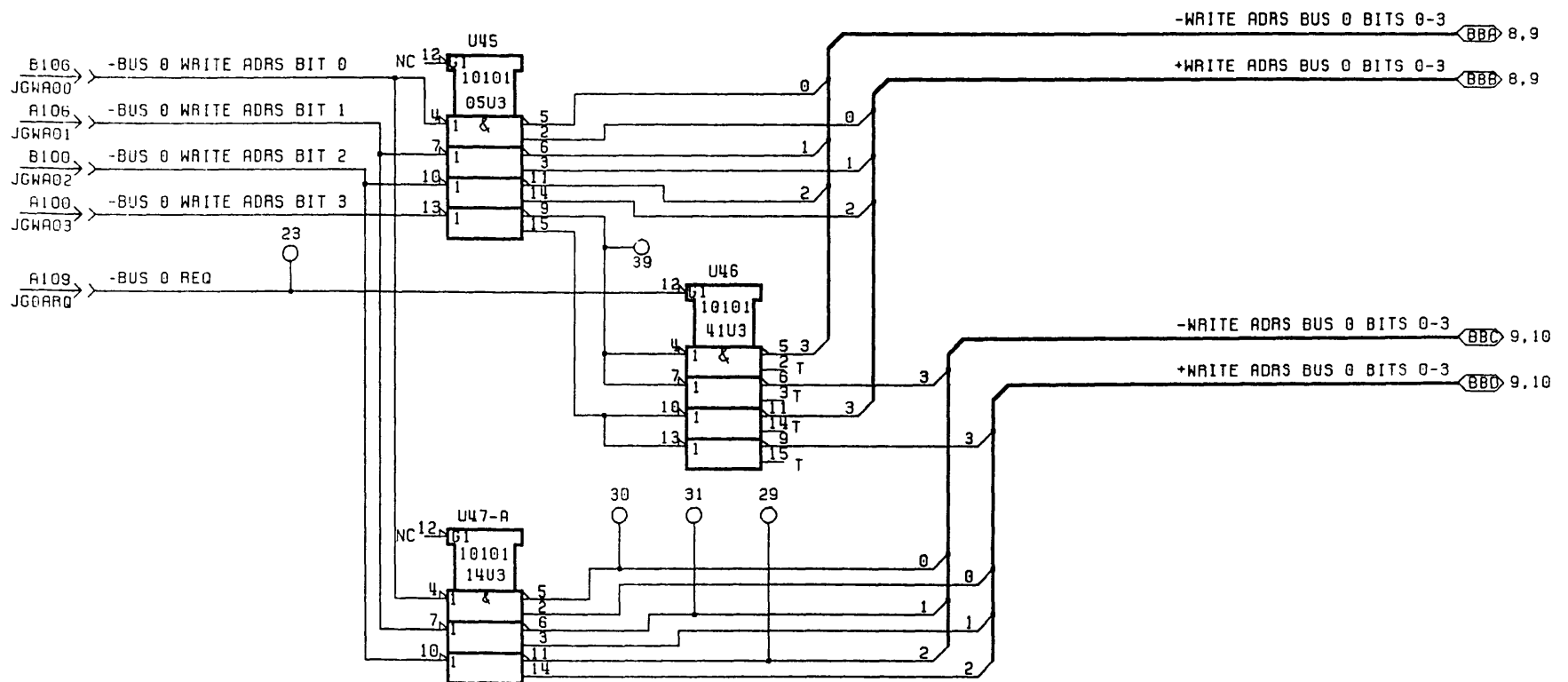
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			53575508	11/01/85	A
		SHEET NO. 5		60462210	PAGE JJ-05

CMI FIFO BUS 1 BITS 6-8,15-18, CM ADRS/FCTN



 CONTROL DATA	CMI FIFO BUS 1 BITS 6-8,15-18 CM ADDRESS/FUNCTION TYPE 1JJH				B	DWG NO. 53575508	DATE 11/01/85	REV A
	N					SHEET NO. 6	60462210	PAGE JJ-06

BUS 0 ADRS INPUT RGTR



△ SIGNAL NAMES IN PARENTHESES APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESES,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07



CHI BUS 0 ADDRESS
INPUT REGISTER

TYPE 1JH

B

DWG NO.
53575508

DATE
11/01/85

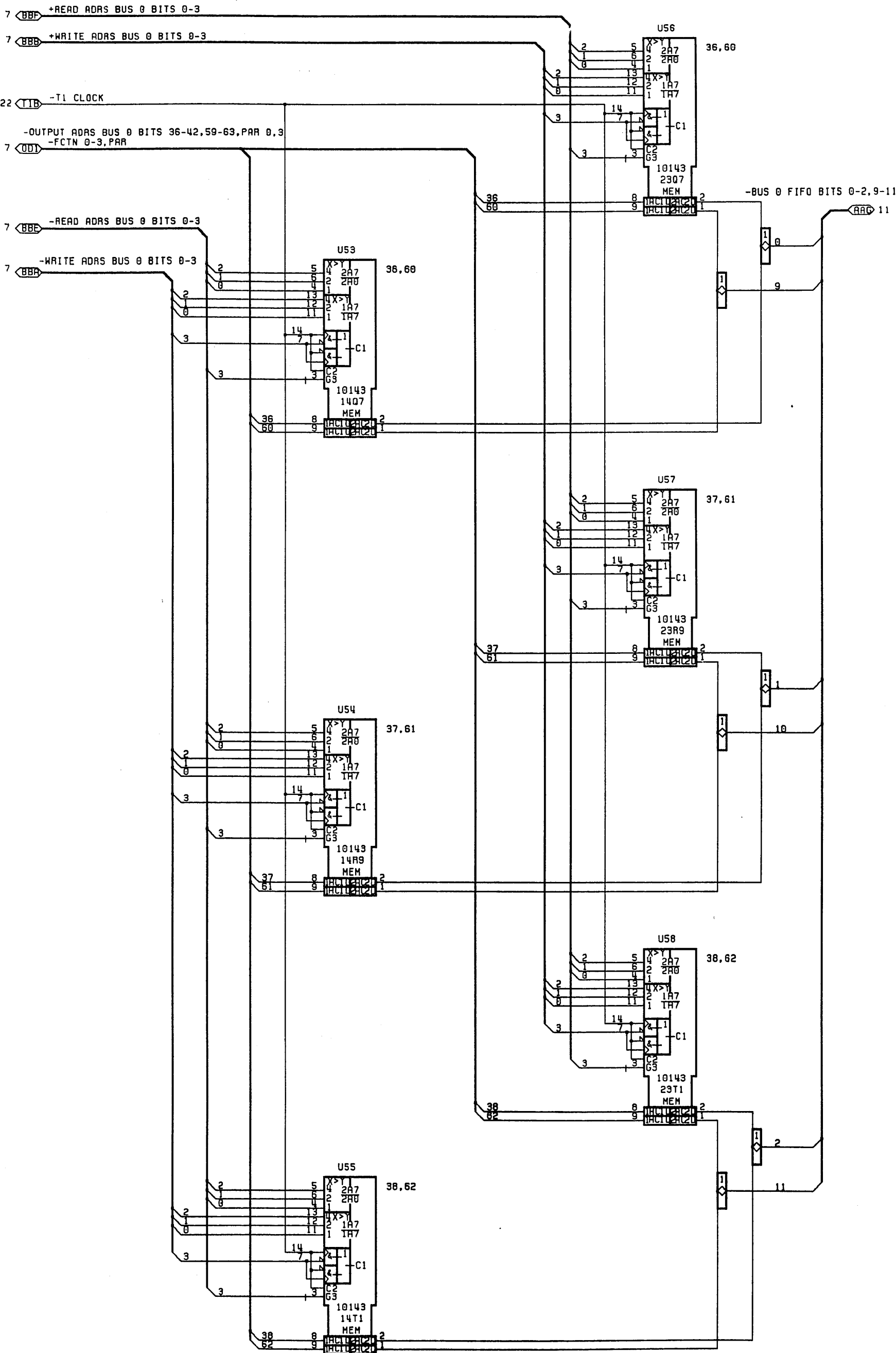
REV
A


SHEET NO. 7

60462210

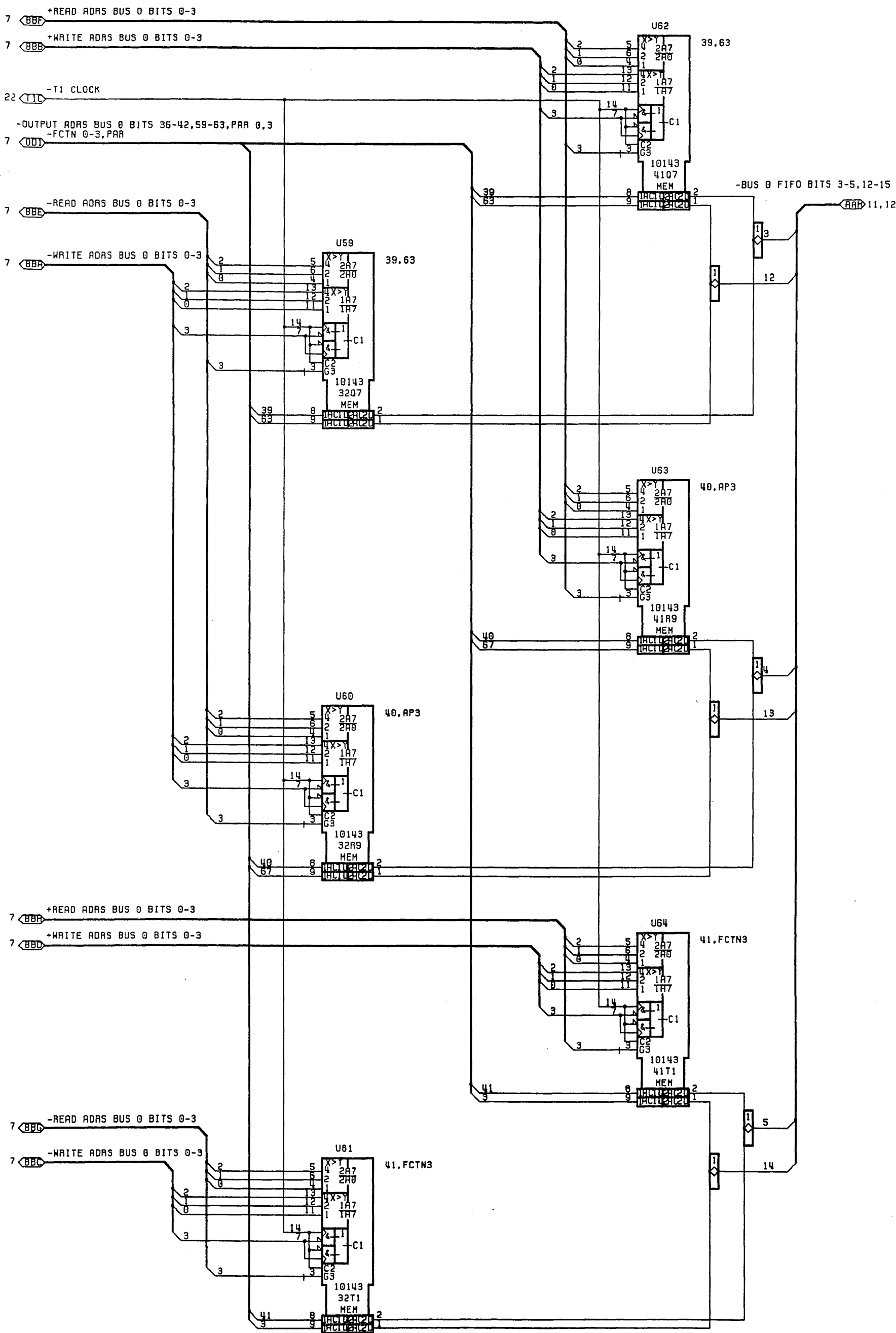
PAGE JJ-07


CMI FIFO BUS 0 BITS 0-2,9-11, CM WRITE, CM ADRS



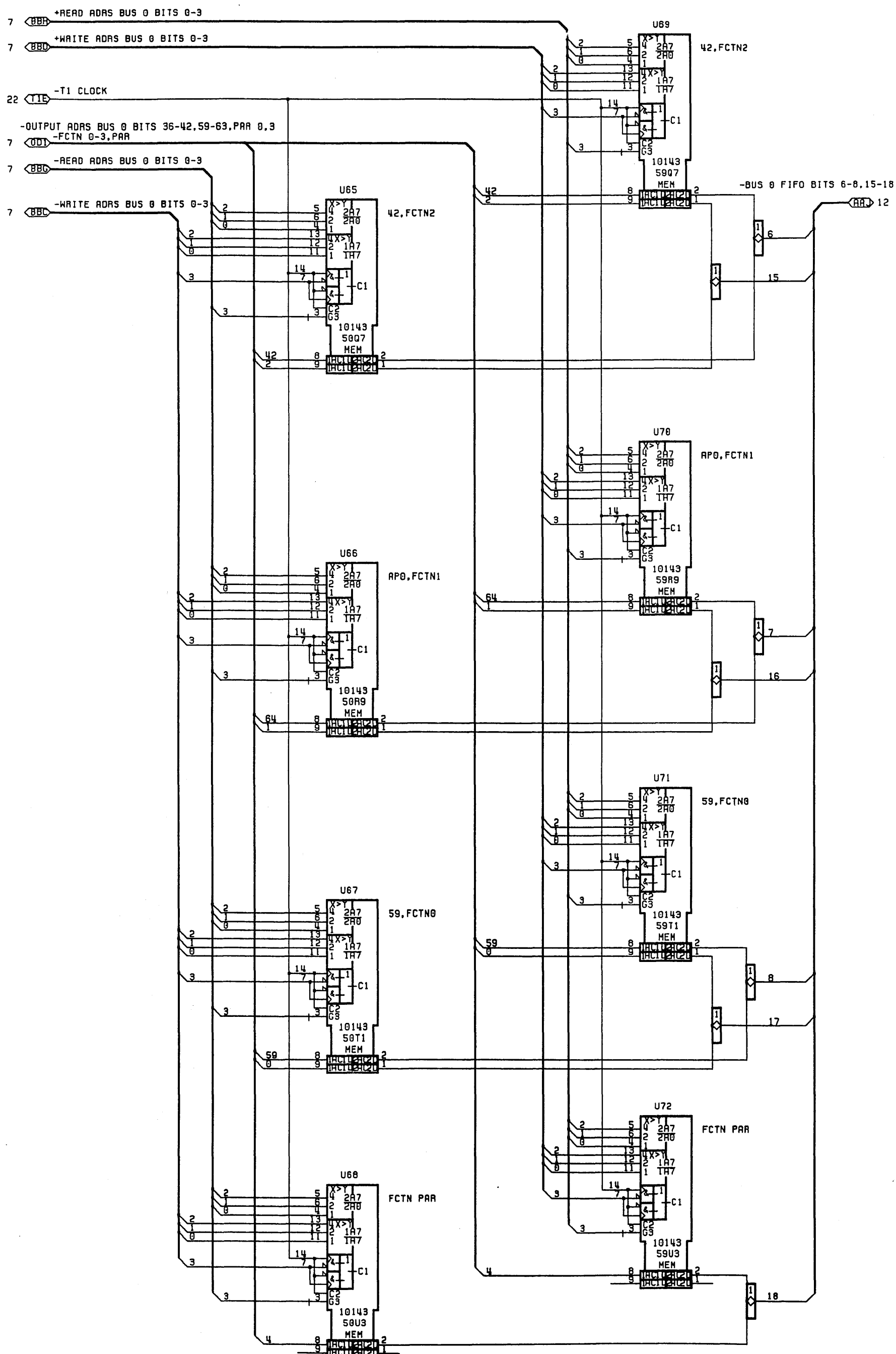
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	BITS 0-2,9-11. CM WRITE			53575508	11/01/85	A
	CM ADDRESS					
	TYPE 1JH		N	SHEET NO. 8	60462210	PAGE

CMI FIFO BUS 0 BITS 3-5,12-14, CM ADRS/FCTN



 CONTROL DATA	CMI FIFO BUS 8 BITS 3-5,12-14 CM ADDRESS/FUNCTION TYPE 1JJH	B	DWG NO. 53575508	DATE 11/01/85	REV A
	N	SHEET NO. 9	60462210	PAGE JJ-09	

CMI FIFO BUS 0 BITS 6-8,15-18, CM ADRS/FCTN



CMI FIFO BUS 0
BITS 6-8,15-18
CM ADDRESS/FUNCTION
TYPE 1JJH

B

DWG NO.

53575508

DATE

11/01/85

REV

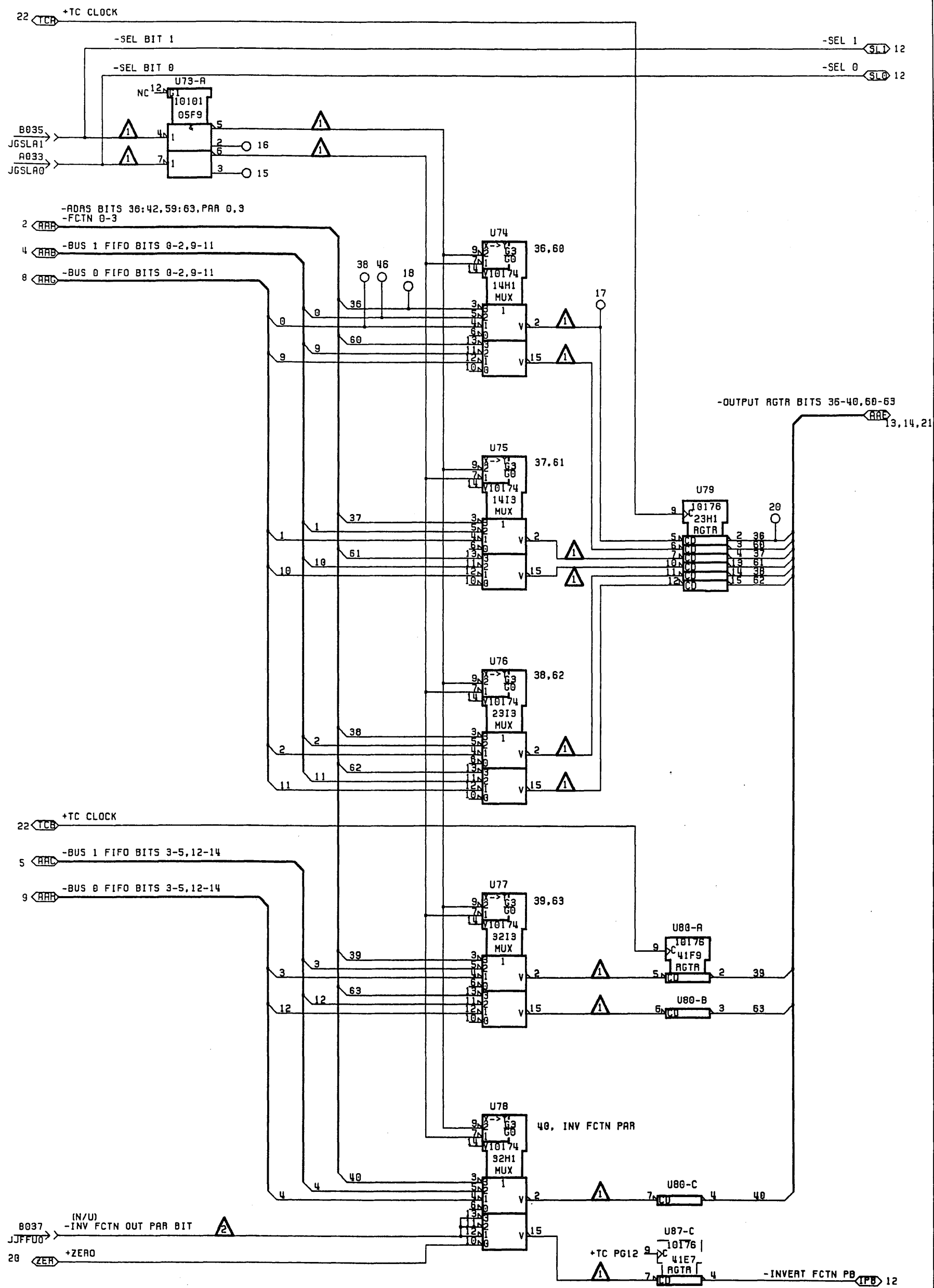
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SHEET NO. 10

60462210

PAGE JJ-10

CMI DATA MUX AND OUT RGTR
ADRS BITS 36-40, 60-63

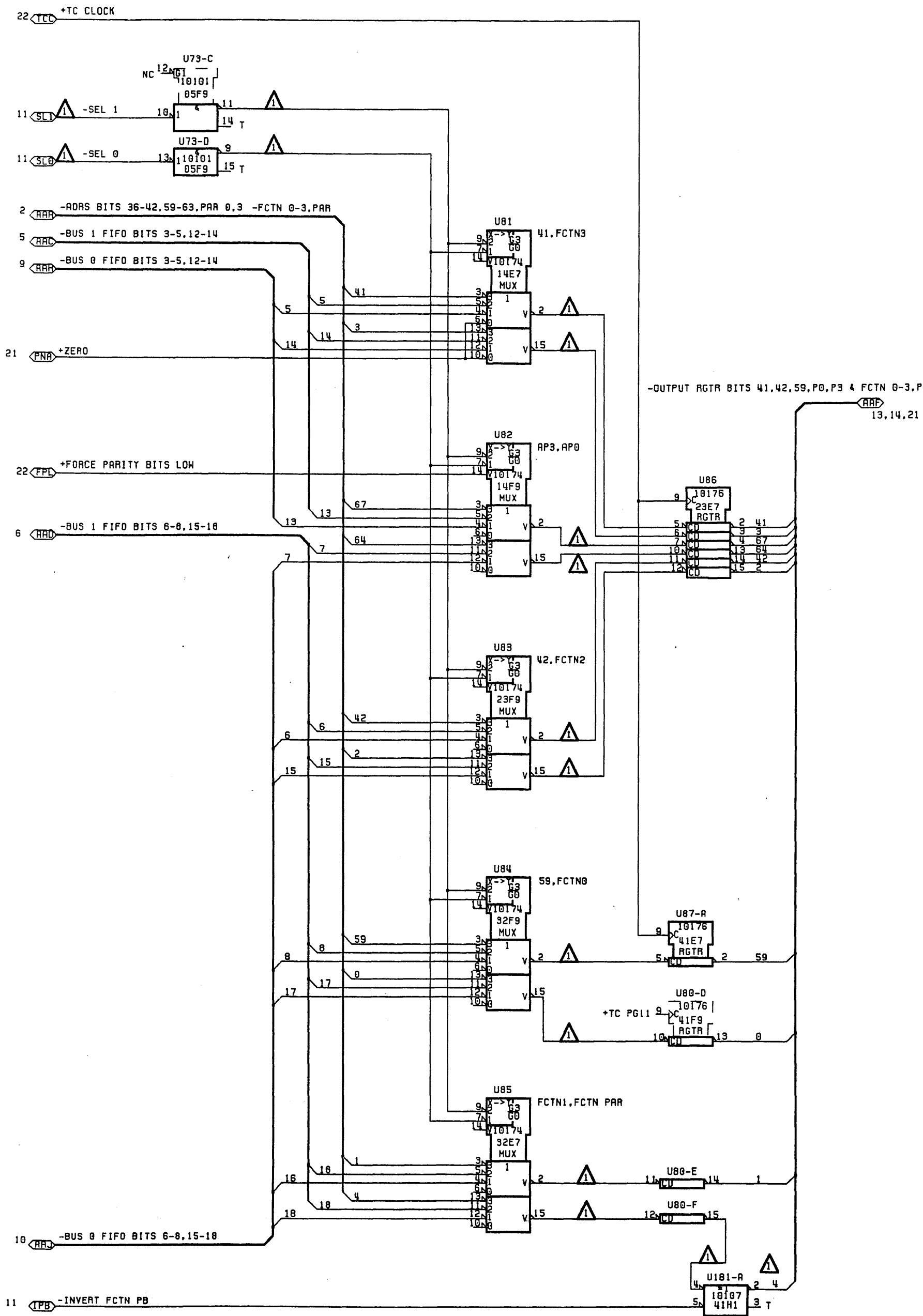



△ SHORT

△ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

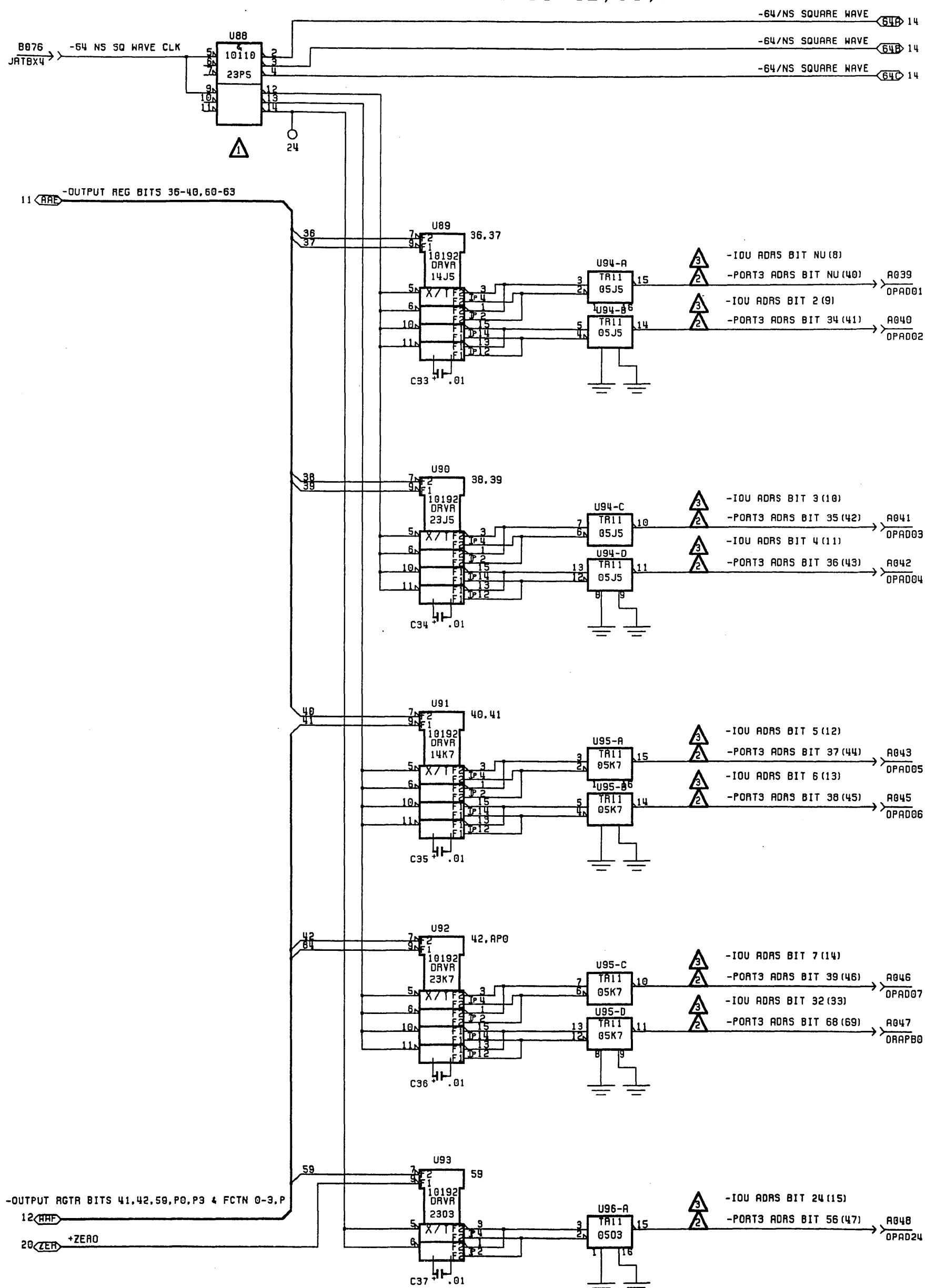
CONTROL DATA	CMI DATA MUX AND OUTPUT RGTR ADRS BITS 36-40, 60-63		DWG NO.	DATE	REV
	TYPE 1JH		B	53575508 11/01/85	A
	SHEET NO. 11		60462210	PAGE	JJ-11

CMI DATA MUX AND OUT RGTR ADRS BITS 5-8,13-18,PAR 0-3



 CONTROL DATA	CMI DATA MUX AND OUTPUT RGTR ADRS BITS 5-8,13-18		B	DWG NO.	DATE	REV
				53575508	11/01/85	A
	TYPE 1JJH			SHEET NO. 12	68462210	PAGE


ADRS TRANSMITTERS TO CM BITS 36-42,59,PAR BIT 0



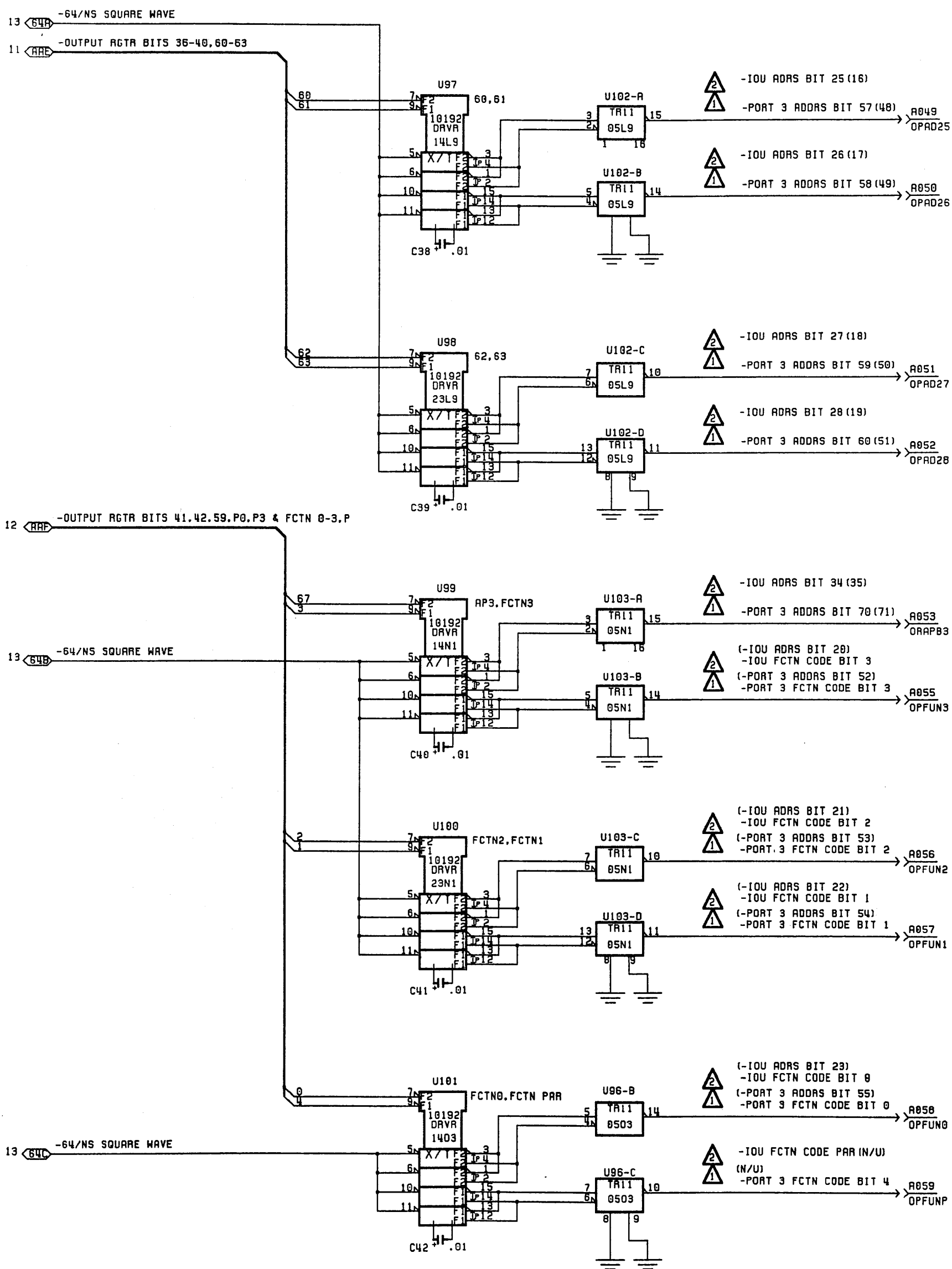
⚠ ALL OUTPUTS SHOULD BE OF EQUAL LENGTH

⚠ THESE SIGNAL NAMES MATCH THE MODEL 990 CMC DIAGRAM NOMENCLATURE. THE FIRST BIT NUMBER APPLIES TO LOCATION A06; THE SECOND (XX) APPLIES TO A07.

⚠ THESE SIGNAL NAMES MATCH THE MODEL 845, 855, 840, 850, 880, MODEL A OR MODEL 3 CMC DIAGRAM NOMENCLATURE. THE FIRST NUMBER APPLIES TO LOCATION A06, THE SECOND (XX) APPLIES TO A07.


 CONTROL DATA	ADDRESS TRANSMITTERS TO CM ADDRESS BITS 36-42, 59, ADDRESS PARITY BIT 0 TYPE 1JJH	B	DWG NO. 53575508	DATE 07/18/86	REV D
		SHEET NO. 13	60462210	PAGE	JJ-13

ADRS TRANSMITTERS TO CM BITS 60-63,
ADRS PAR BIT 3 & FCTN BITS 0-3, PAR

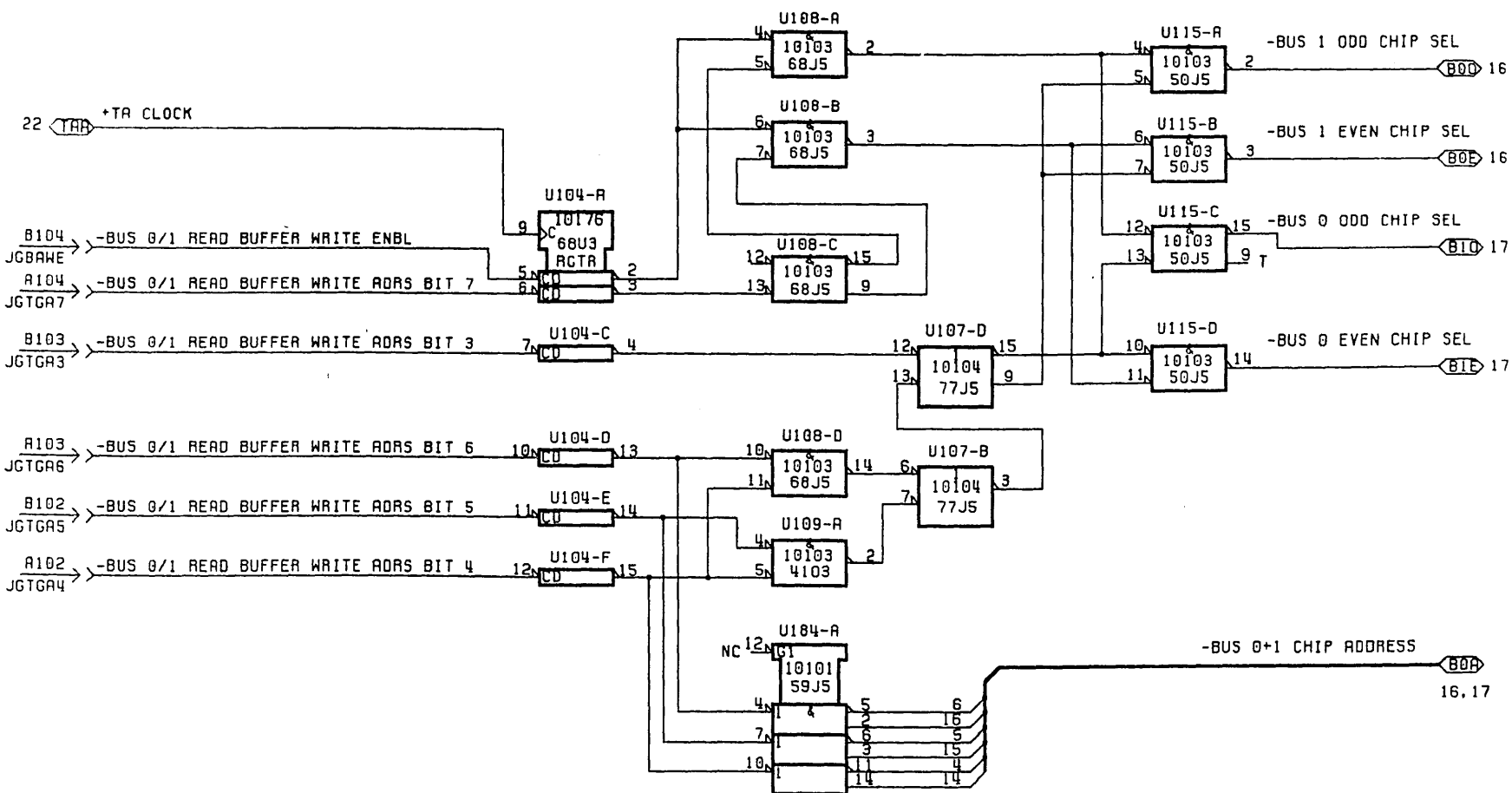


1 THESE SIGNAL NAMES MATCH THE MODEL 990 CMC DIAGRAM NOMENCLATURE.
THE FIRST BIT NUMBER APPLIES TO LOCATION A06; THE NAME
OR BIT NUMBER IN PARENTHESIS APPLIES TO LOCATION A07.

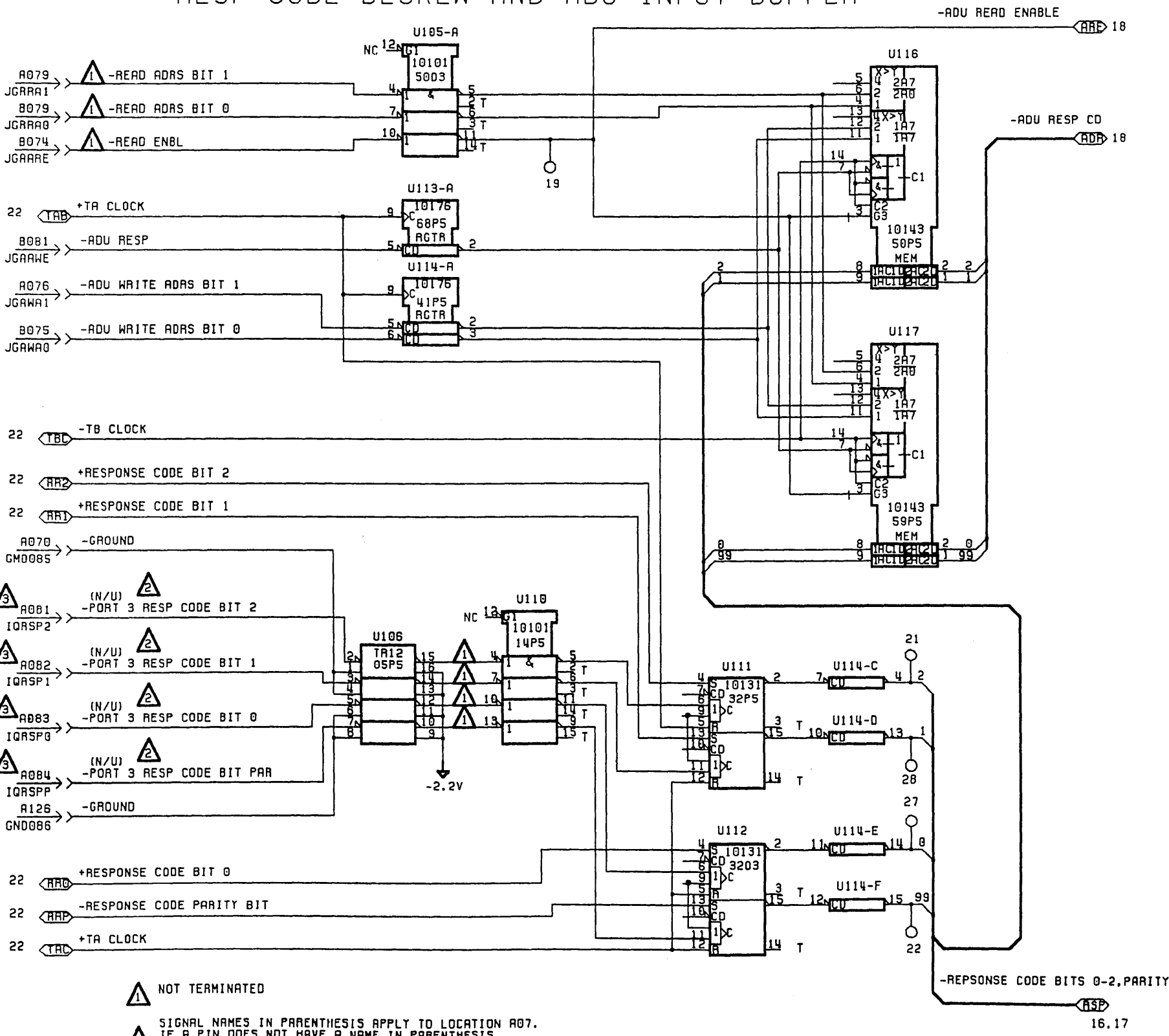
2 THESE SIGNAL NAMES MATCH THE MODEL 845, 855, 840, 850, 860,
MODEL A, OR MODEL S CMC DIAGRAM NOMENCLATURE AT LOCATION A06.
THE BIT IN PARENTHESIS APPLIES TO LOCATION A07.

 CONTROL DATA	ADDRESS TRANSMITTERS TO CM ADDRESS BITS 60-63, AP3 FCTN BITS 0-3, FCTN PAR TYPE 1JJH	B	DWG NO.	DATE	REV
			53575508	04/09/86	C
			SHEET NO. 14		

BUS WRITE ADRS DECODER



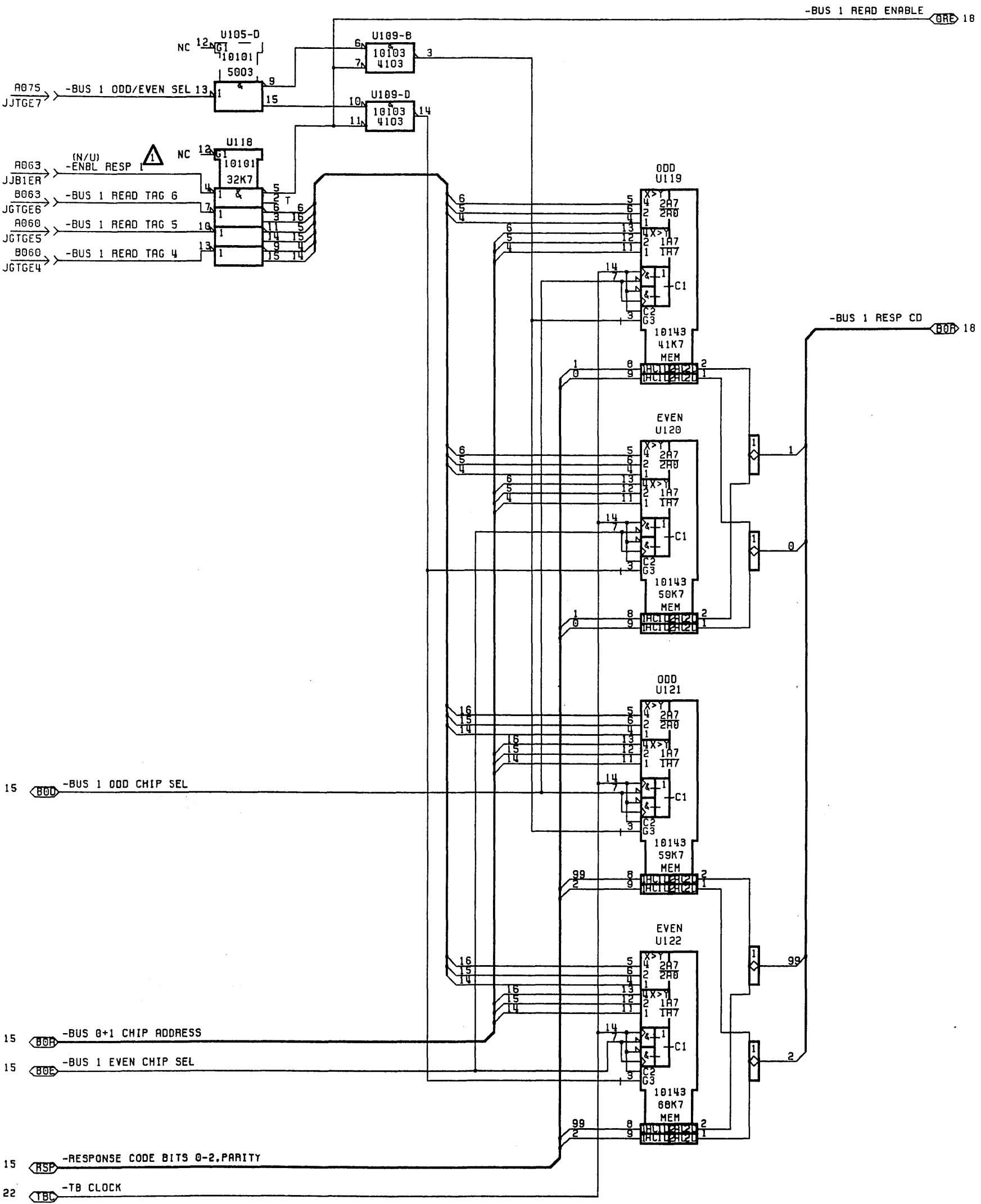
RESP CODE DESKEW AND ADU INPUT BUFFER




- 1 NOT TERMINATED
- 2 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.
- 3 PORT 3 NAME APPLIES TO MODEL 990 CMC. OTHER MODELS' NAMES ARE -IOU RESPONSE CODE BITS 0-2/PAR.

	BUS WRITE ADDRESS DECODE AND RESPONSE CODE DESKEW & ADU INPUT BUFFER		OWG NO.	DATE	REV
	TYPE 1JJH		53575508	04/09/86	C
SHEET NO.	15	60462210	PAGE JJ-15		

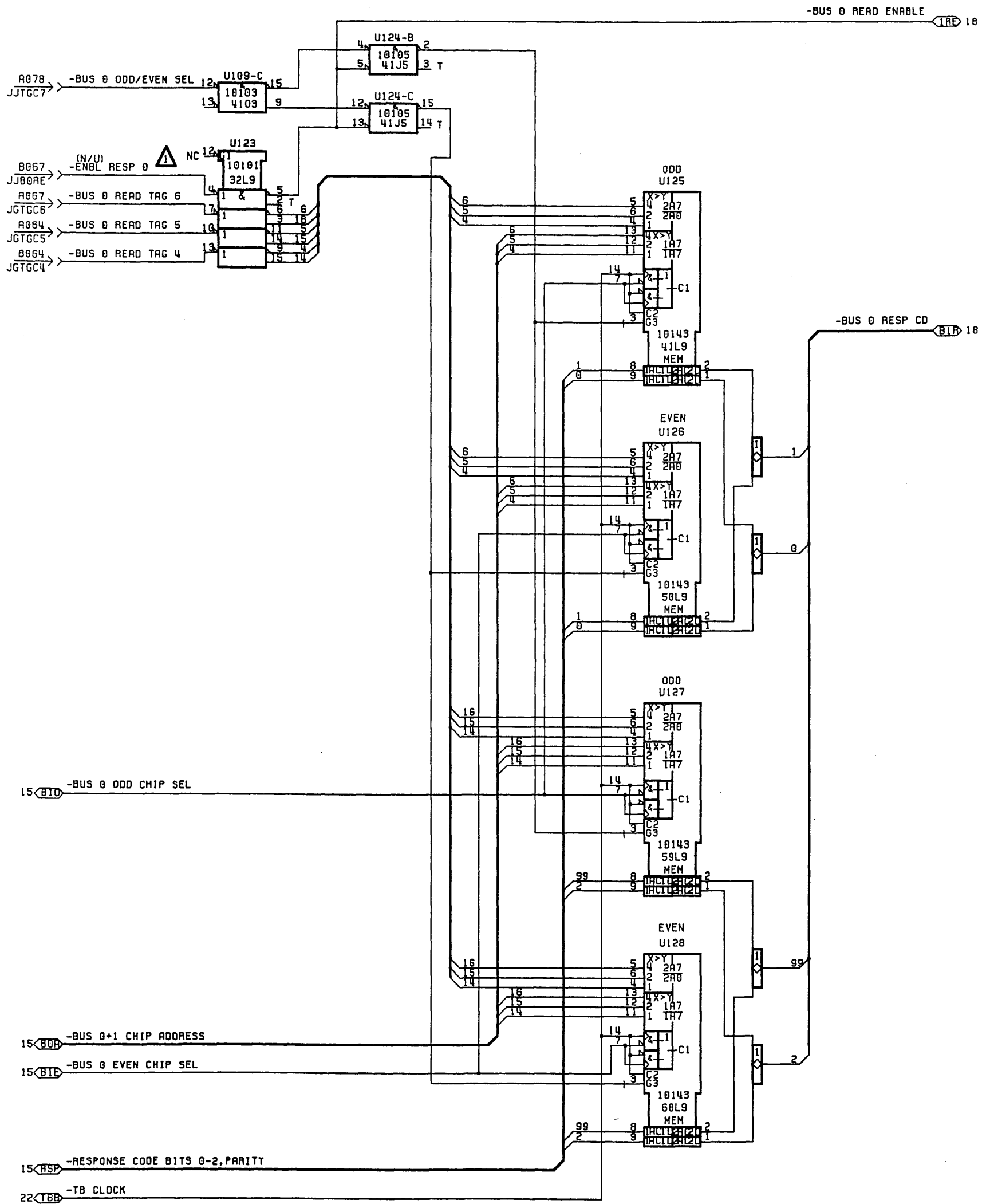
BUS 1 RESP CODE MEM




⚠ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	BUS 1 RESPONSE CODE MEMORY		B	DWG NO.	DATE	REV
	TYPE 1JJH			53575508	11/01/85	A
			N		SHEET NO. 16	60462210

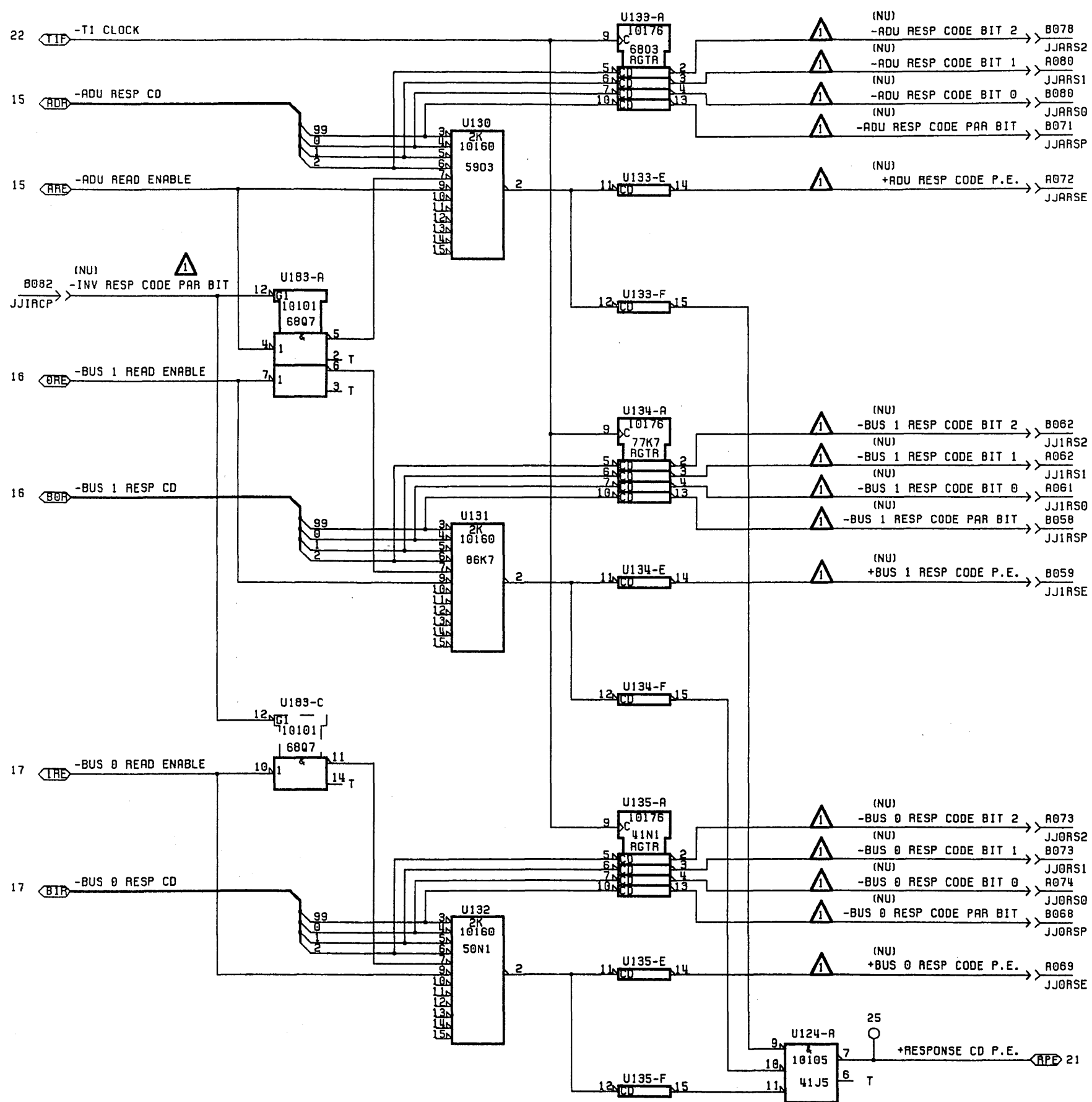
BUS 0 RESP CODE MEM




△ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	BUS 0 RESPONSE CODE MEMORY	B	DWG NO.	DATE	REV
	TYPE 1JJH		53575508	11/01/85	A
			N	SHEET NO. 17	60462210

RESP CODE PAR CHECKER

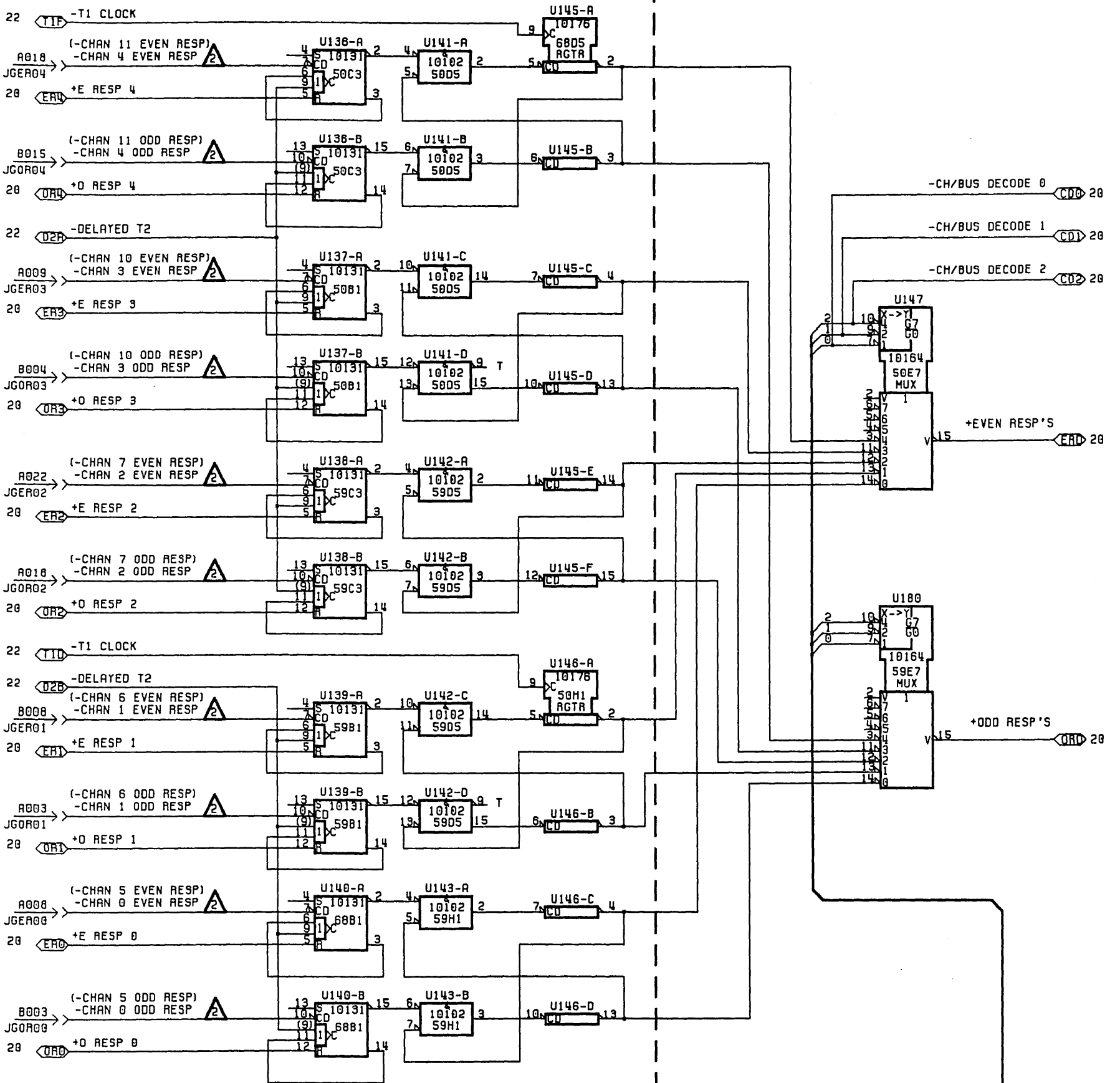


⚠ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	RESPONSE CODE PARITY CHECK		B	DWG NO.	DATE	REV
				53575508	11/01/85	A
	TYPE 1JJH			SHEET NO. 18		60462210

HLDG RGTRS

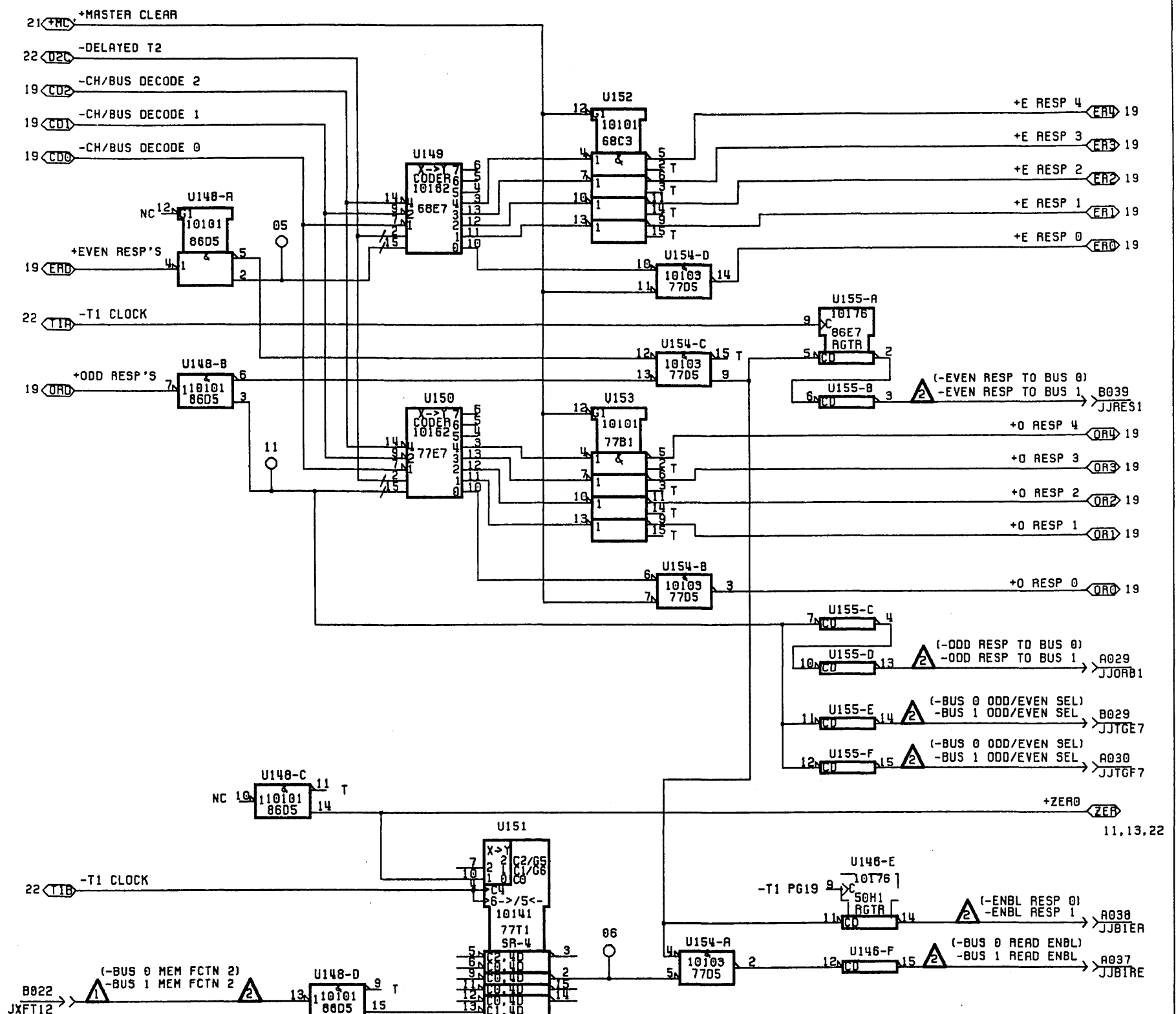
RESP SEL



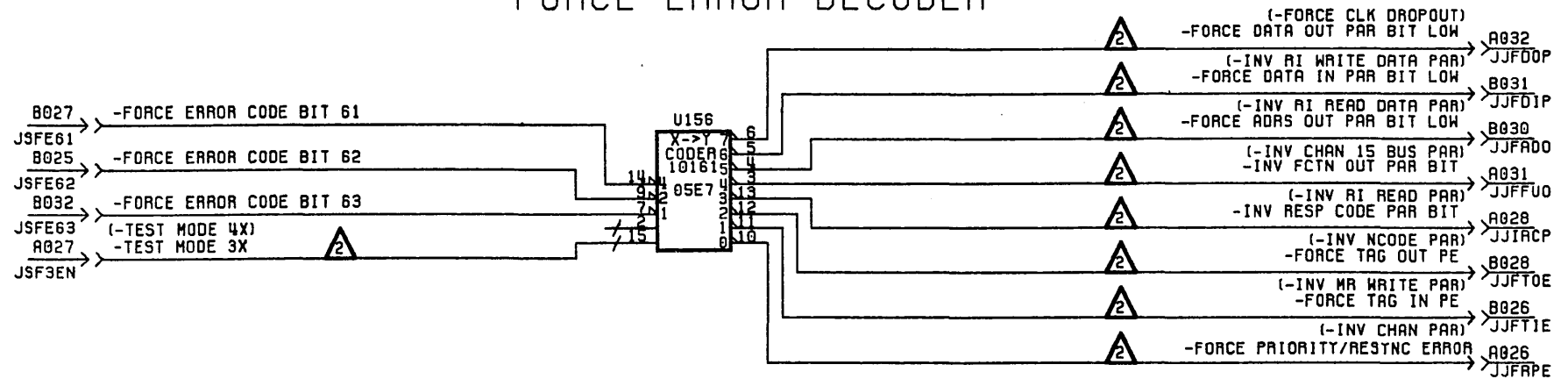
△ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

	HOLDING REGISTERS AND BUS RESPONSE SELECT		B	DWG NO. 53575508	DATE 07/18/88	REV D
	TYPE 1JJH		N	SHEET NO. 19	60462210	PAGE JJ-19

CHAN RESP SEL



FORCE ERROR DECODER



CMI FORCE ERRORS (3X) MUX DECODES FOR LOC A06	
7	FORCE DATA OUT PAR BIT LOW
6	FORCE DATA IN PAR BIT LOW
5	FORCE ADAS OUT PAR BIT LOW
4	INV FCTN OUT PAR BIT
3	INV RESP CODE PAR BIT
2	FORCE TAG OUT PAR ERROR
1	FORCE TAG IN PAR ERROR
0	FORCE REQ PRIORITY RESYNC ERROR

MAC FORCE ERRORS (4X) MUX DECODES FOR LOC A07	
7	FORCE CLK DROPOUT
6	INV RI WRITE DATA PAR
5	INV RI READ DATA PAR
4	INV CHAN 15 BUS PAR
3	INV RI READ PAR BIT
2	INV NCODE PAR
1	INV MR WRITE PAR
0	INV CHAN PAR

1 NOT TERMINATED ON THIS BOARD

2 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.



CHANNEL RESPONSE SELECT
FORCE ERROR DECODER

TYPE 1JJH

8

DWG NO.
53575508

DATE
07/18/86

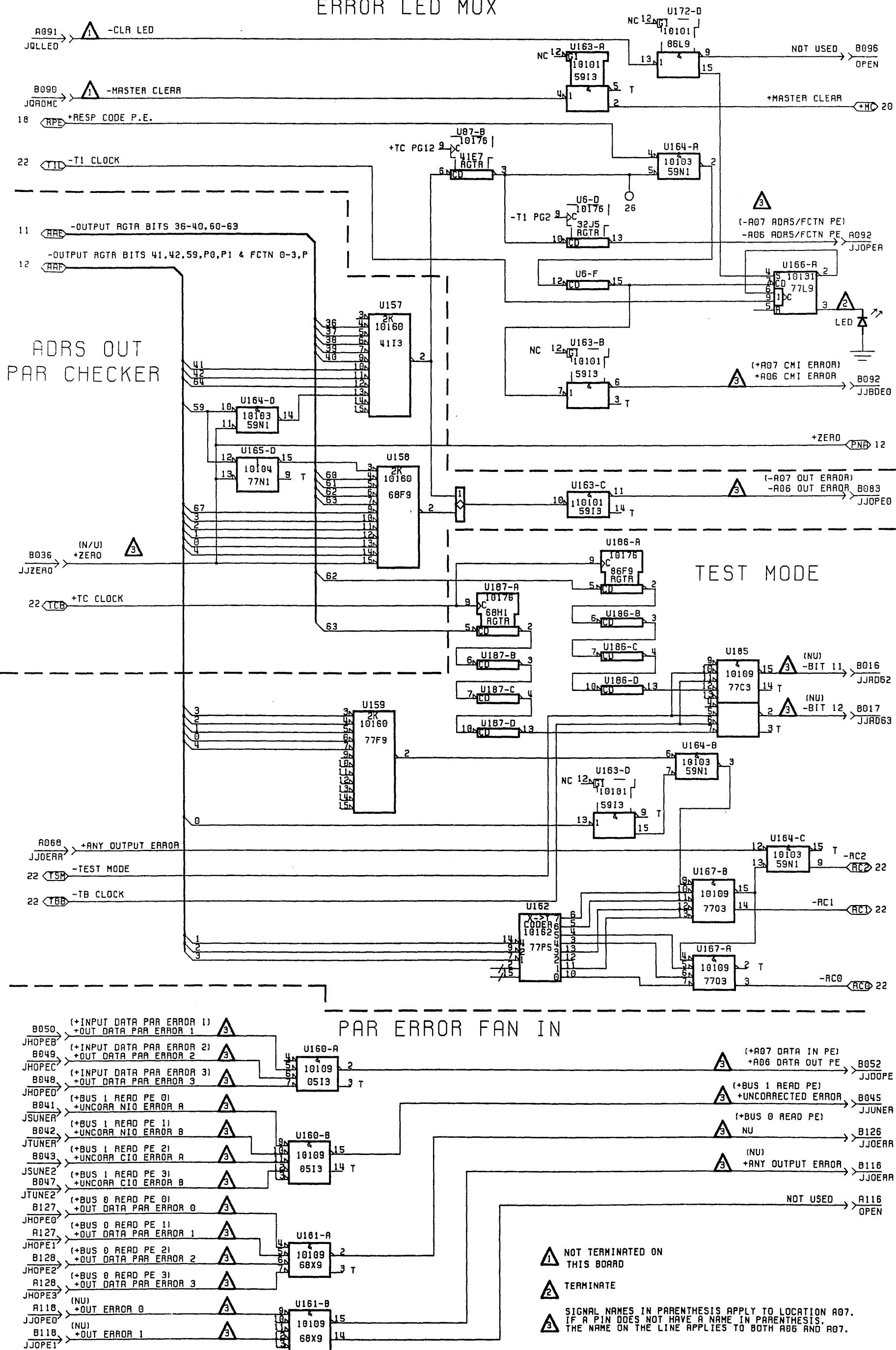
REV
D

SHEET NO. 20

60462210

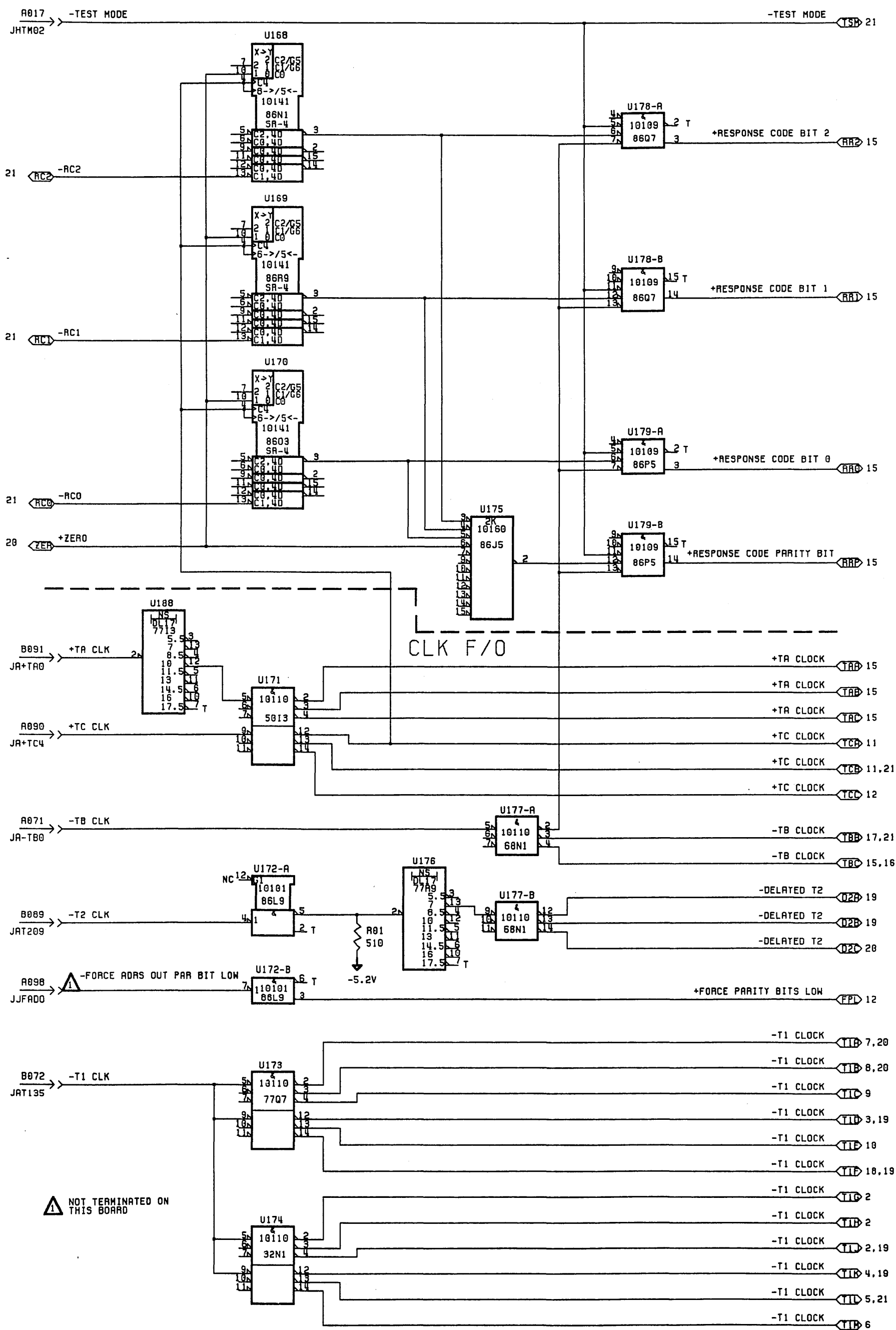
PAGE
JJ-20

ERROR LED MUX



CONTROL DATA	ERROR LED MUX, ADDRESS OUT PARITY CHECK AND TEST MODE TYPE 1JH	B	DWG NO.	DATE	REV
			53575508	11/01/85	A
SHEET NO.	21	N	60462210	PAGE	JJ-21

TEST MODE




 CONTROL DATA	TEST MODE AND CLOCK FANOUT TYPE 1JJH	B	DWG NO. 53575508	DATE 07/18/86	REV D

SHEET NO. 22 60462210 PAGE JJ-22

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	02	-ADU REQUEST	27	15	-RESP CODE BIT 0
02	02	-WRITE ADRS BIT 2	28	15	-RESP CODE BIT 1
03	02	-WRITE ADRS BIT 1	29	07	-WR ADRS BUS0 BIT 2
04	02	-WRITE ADRS BIT 0	30	07	-WR ADRS BUS0 BIT 0
05	20	-EVEN RESPONSES	31	07	-WR ADRS BUS0 BIT 1
06	20	+BUS WRITE	32	03	-BUS 1 REQUEST
07	02	-READ ADRS BIT 1	33	07	-RD ADRS BUS0 BIT 1
08	02	-READ ADRS BIT 2	34	07	-RD ADRS BUS0 BIT 2
09	02	-READ ADRS BIT 0	35	07	-RD ADRS BUS0 BIT 0
10	02	-ADRS BIT 36	36	07	-RD ADRS BUS0 BIT 3
11	20	-ODD RESPONSES	37	07	-WR ADRS BUS0 BIT 3
12	19	+BUS TIME CD BIT 1	38	11	-BUS 0 FIFO BIT 0
13	19	+BUS TIME CD BIT 2	39	07	-WR ADRS BUS0 BIT 3
14	19	+BUS TIME CD BIT 4	40	03	-WR ADRS BUS1 BIT 2
15	11	+SEL BIT 0	41	03	-WR ADRS BUS1 BIT 1
16	11	+SEL BIT 1	42	03	-WR ADRS BUS1 BIT 0
17	11	-CMI DATA MUX BIT36	43	03	-RD ADRS BUS1 BIT 1
18	11	-ADRS BIT 36	44	03	-RD ADRS BUS1 BIT 0
19	15	-ADU READ ENABLE	45	03	-RD ADRS BUS1 BIT 2
20	11	-OUTPUT RGTR BIT 36	46	11	-BUS0 FIFO BIT 0
21	15	-RESP CODE BIT 2	47	03	-RD ADRS BUS1 BIT 3
22	15	-RESP CODE PARITY	48	03	-OUTP ADRS BUS1 BIT36
23	07	-BUS 0 REQUEST	49	03	-WRT ADRS BUS1 BIT3
24	13	-64 N/S SQ WAVE	50		
25	18	+RESP CODE P.E.	51		
26	21	+OUTPUT RGTR P.E.			

CONNECTOR PINS	
GND	A014, B014, A024, B024, A034, B034, A054, B054, A065, B065, A066, B066, A077, B077, A097, B097, A107, B107, A117, B117
-5.2V	A001, B001, A002, B002, A129, B129, A130, B130
-2.2V	A007, B007, A044, B044, A087, B087, A124, B124
+5V	A061, B061, A070, B070 (NOT USED)
TERM	NONE
UNUSED	B046, B051, B053, B061, B069, B070

 CONTROL DATA	CMI ADDRESS BOARD		B	DWG NO.	DATE	REV
	TESTPOINTS AND SIGNAL NAMES AND CONNECTOR PINS			53575508	11/01/85	A
	TYPE 1JJH		N	SHEET NO. 23	60462210	PAGE


CAUTION

There are two sets of logic diagrams for this board. Each set supports a different board version. The appropriate logic diagram set for your board has a board master (B/M) number that matches the printed wiring board (PWB) number of the board. The B/M number is located in the upper right corner of the diagram set cover page (sheet 1), and the PWB number is located on the back of the board.

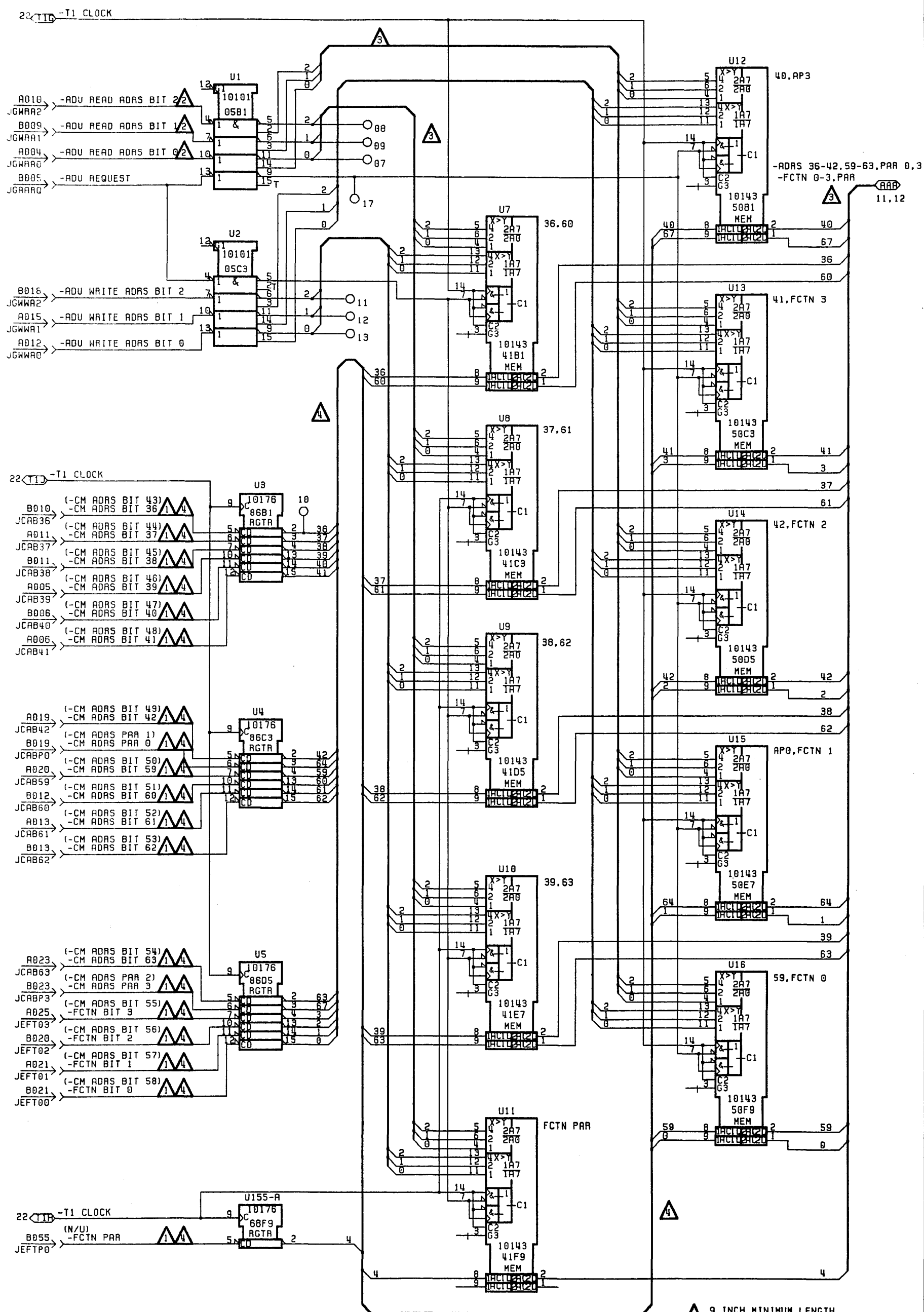
CMI ADRS BOARD

[illegible]

OWN	L H JOHNSON	12/13/85
CHKD	D R FORD	02/24/86
ENG	J P STROMBECK	01/31/86
PUBS	R K BONDE	02/24/86
APP	J P STROMBECK	01/31/86

 CONTROL DATA	REVISION HISTORY	B	DWG NO. 22105674	DATE 07/18/86	REV B
	TYPE 1.1.1H	SHEET NO. 1	60462210	PAGE JJ-01	


CM ADU ADRS BUFFER BITS 36-42,59-63,PAR 0,3 & MEM FCTN BITS 0-3,PAR



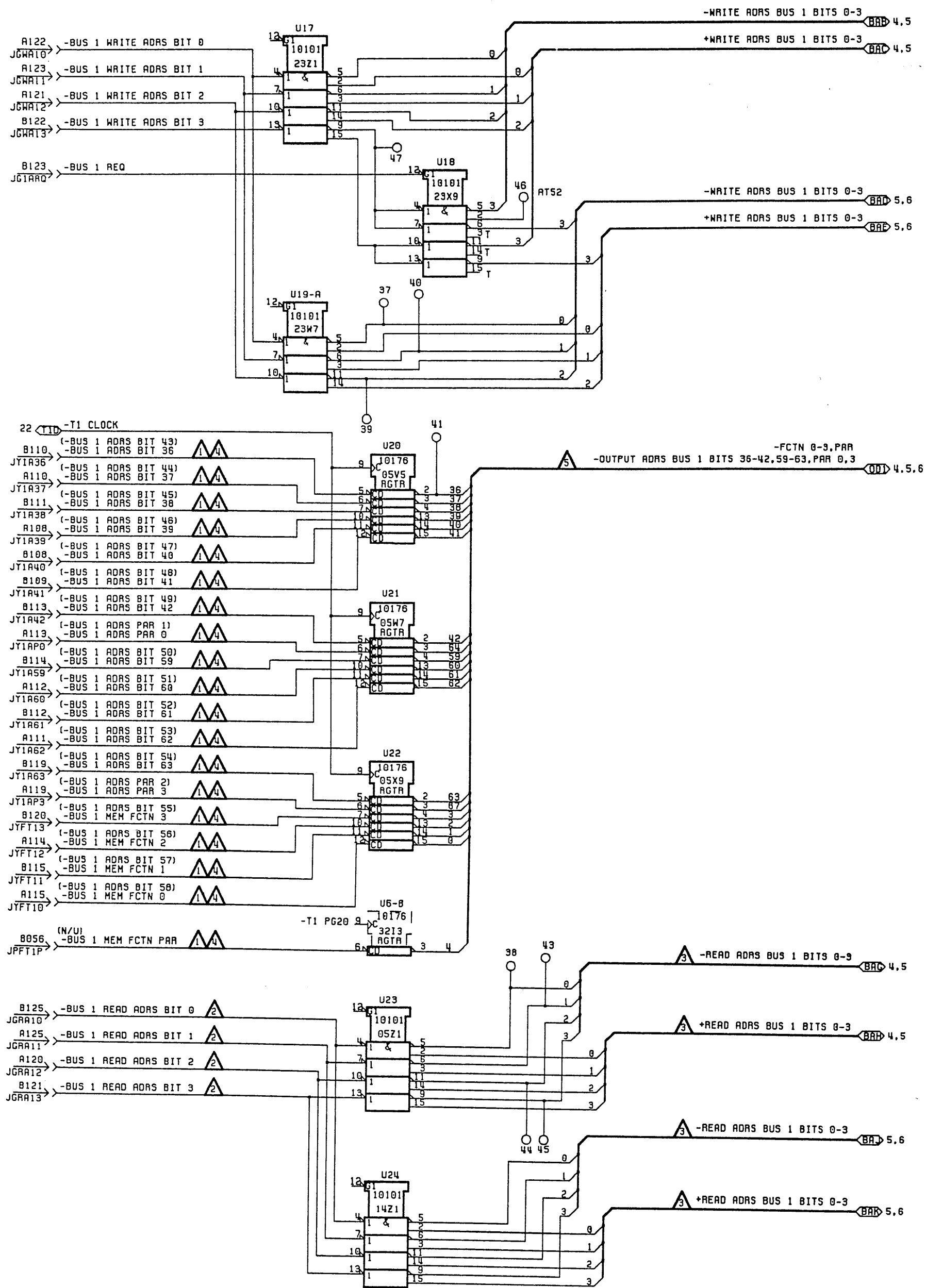
△ SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

△ 3 INCH MAXIMUM LENGTH

△ 9 INCH MAXIMUM LENGTH

 CONTROL DATA	CM ADU ADDRESS BUFFER. ADDRESS BITS 36-42,59-63,PARITY 0,3	B	DWG NO.	DATE	REV
	MEMORY FUNCTION BITS 0-3,PARITY		22105674	12/13/85	A
	TYPE 1JJH		SHEET NO. 2		

BUS 1 ADRS INPUT RGTR




1 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

2 3 INCH MAXIMUM LENGTH

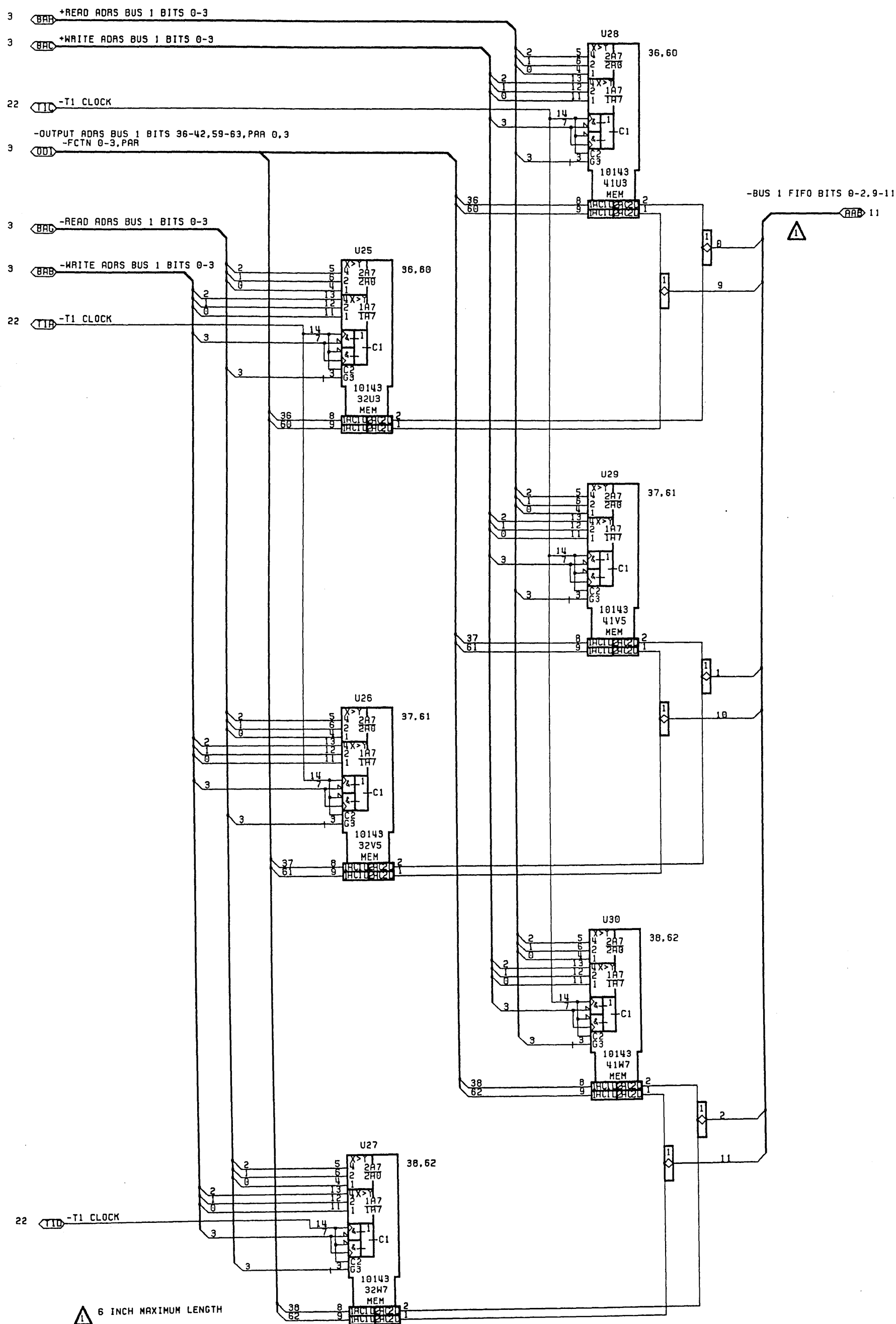
3 9 INCH MAXIMUM LENGTH


4 4.5 INCH MAXIMUM LENGTH

5 9 INCH MINIMUM LENGTH

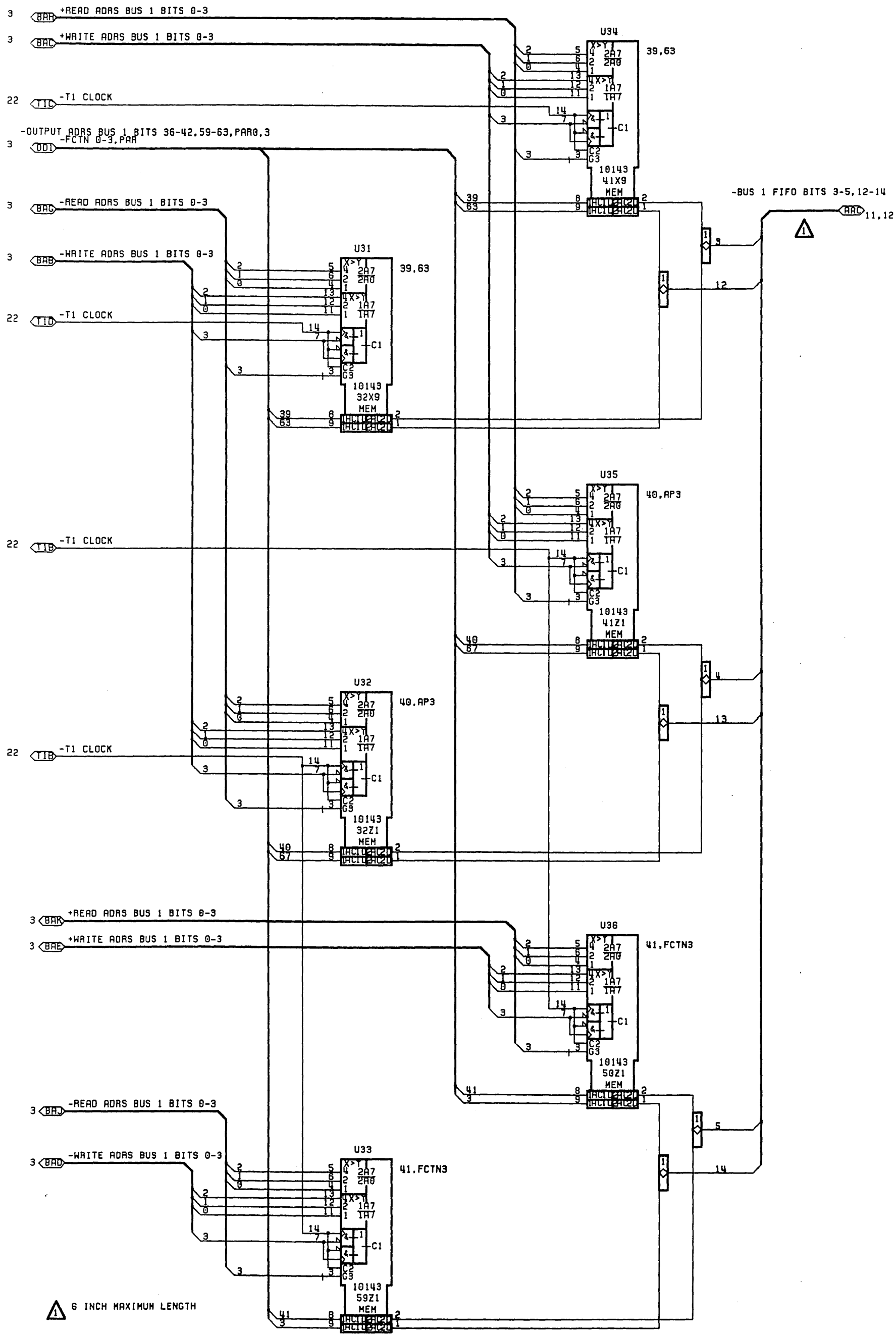
 CONTROL DATA	CHI BUS 1 ADDRESS INPUT REGISTER		B	DWG NO.	DATE	REV
	TYPE 1JJH			22105674	12/13/85	A
	N		SHEET NO.	3	60462210	PAGE JJ-03


CMI FIFO BUS 1 BITS 0-2,9-11, CM WRITE, CM ADRS



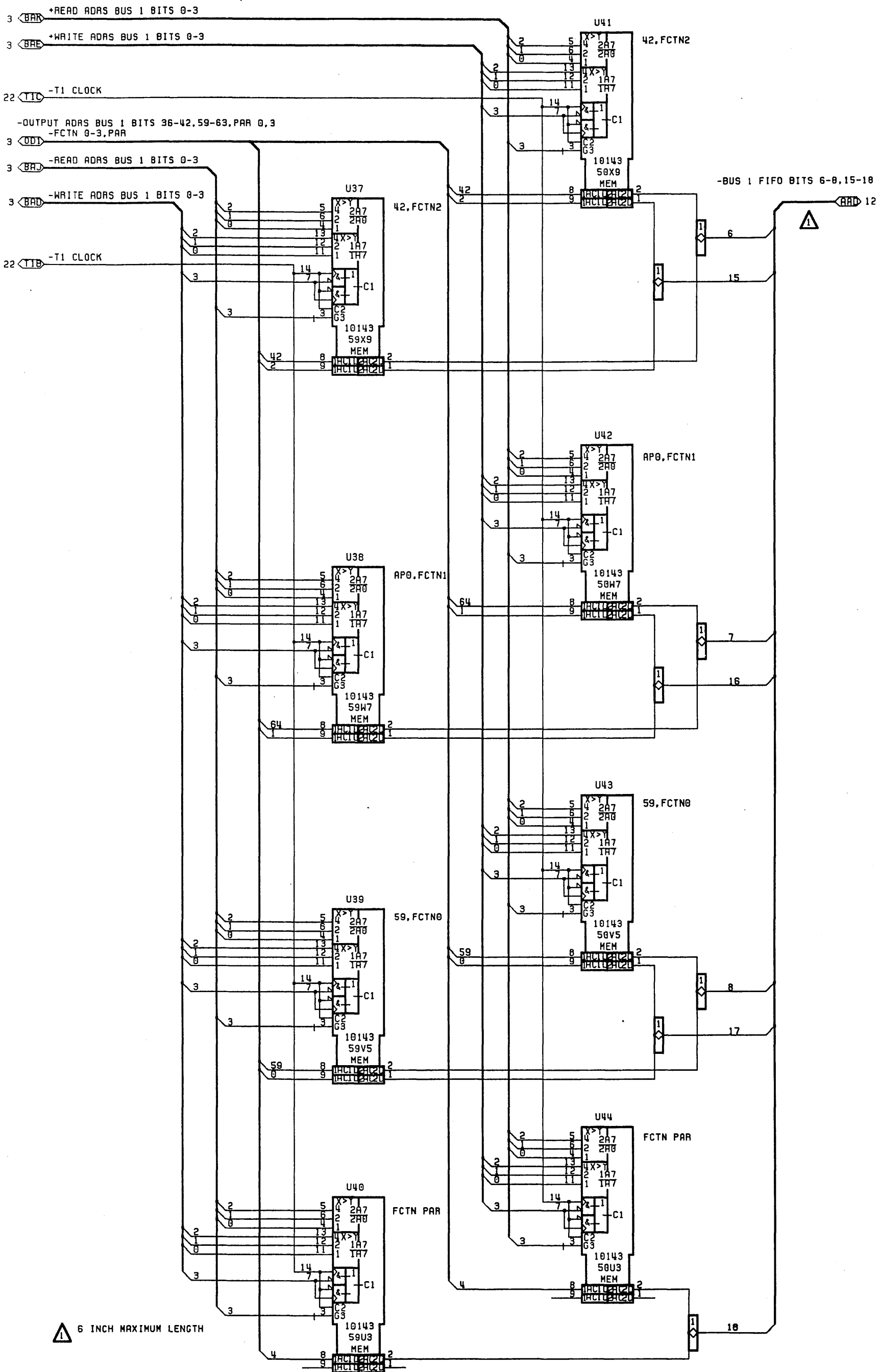
 CONTROL DATA	CMI FIFO BUS 1	B	DWG NO.	DATE	REV
	BITS 0-2,9-11. CM WRITE		22105674	12/13/85	A
	CM ADDRESS				
TYPE 1JH	N	SHEET NO. 4	60462210	PAGE	JJ-04


CMI FIFO BUS 1 BITS 3-5,12-14, CM ADRS/FCTN



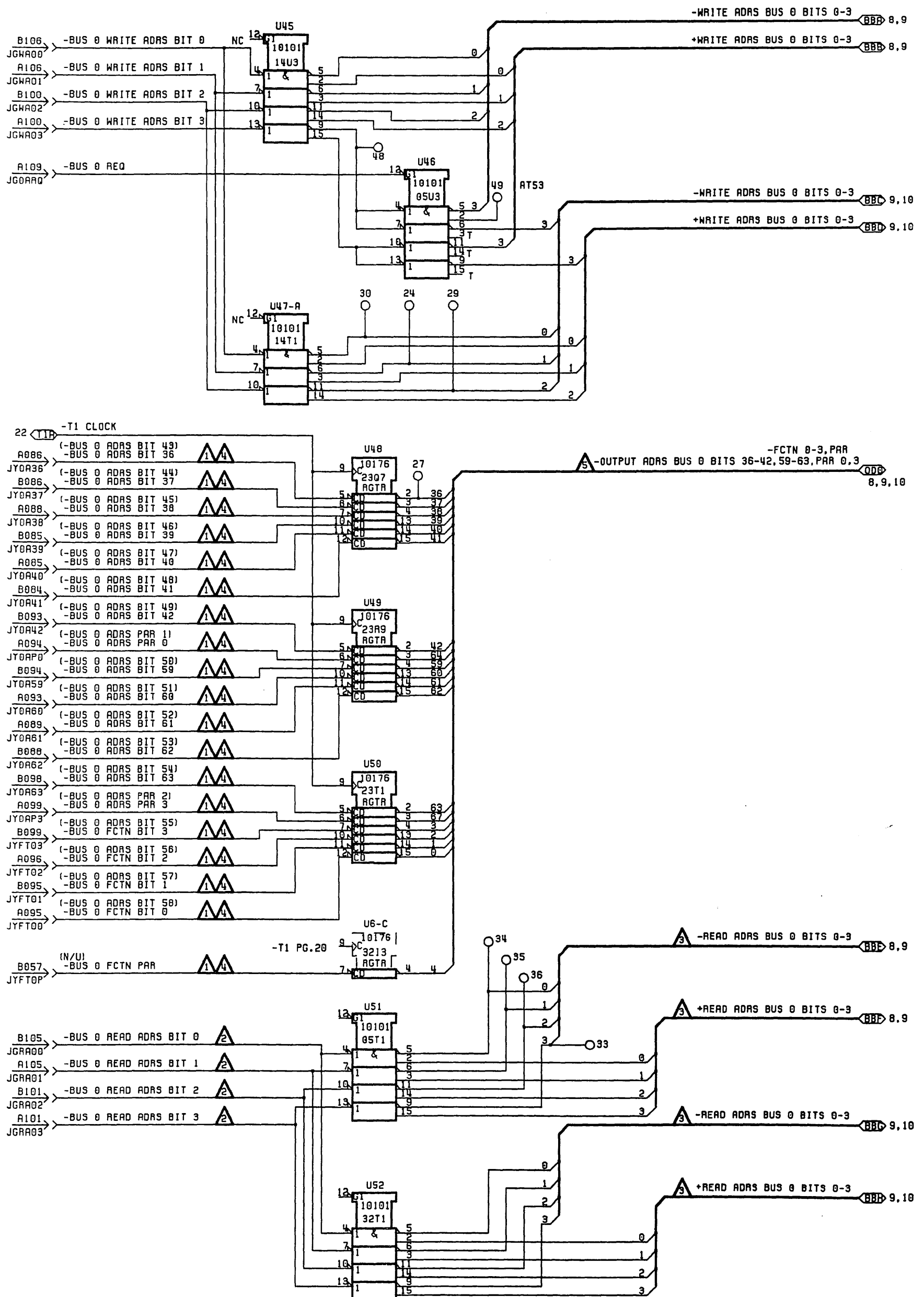
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						22105674	12/13/85	A
	N					SHEET NO. 5	60462210	PAGE JJ-05

FIFO BUS 1 BITS 6-8,15-18, CM ADRS/FCTN



 CONTROL DATA	CMI FIFO BUS 1	B	DWG NO.	DATE	REV
	BITS 6-8,15-18		22105674	12/13/85	A
	CM ADDRESS/FUNCTION				
TYPE 1JJH	N	SHEET NO. 6	60462210	PAGE	JJ-06

BUS 0 ADRS INPU RGTR



1 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07

2 3 INCH MAXIMUM LENGTH

3 9 INCH MAXIMUM LENGTH

5 9 INCH MINIMUM LENGTH

4 4.5 INCH MAXIMUM LENGTH



CMI BUS 0 ADDRESS
INPUT REGISTER

TYPE 1JH

B

DWG NO.

22105674

DATE

12/13/85

REV

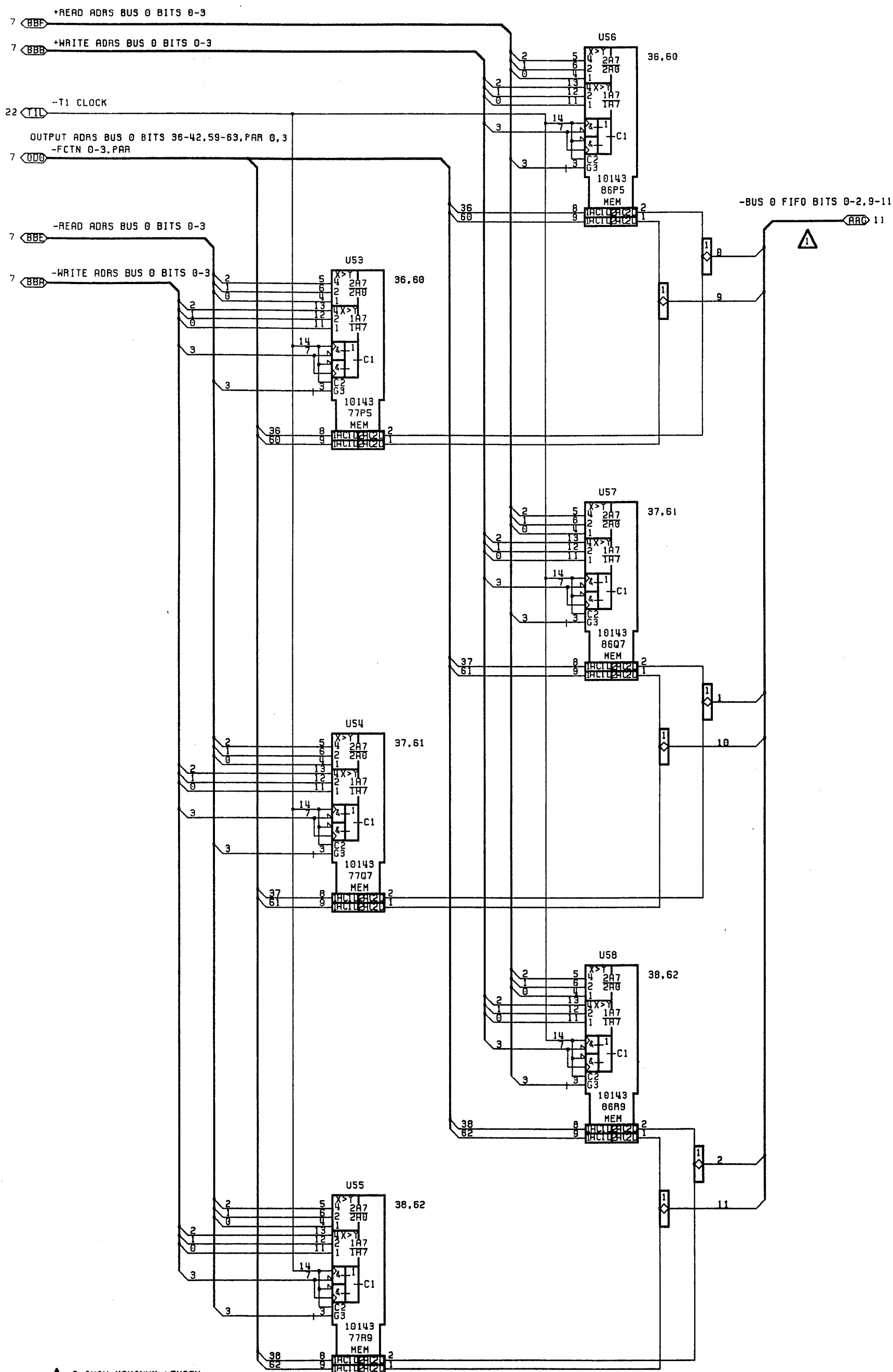
A

SHEET NO. 7

60462210

PAGE JJ-07

CMI FIFO BUS 0 BITS 0-2,9-11, CM WRITE, CM ADRS



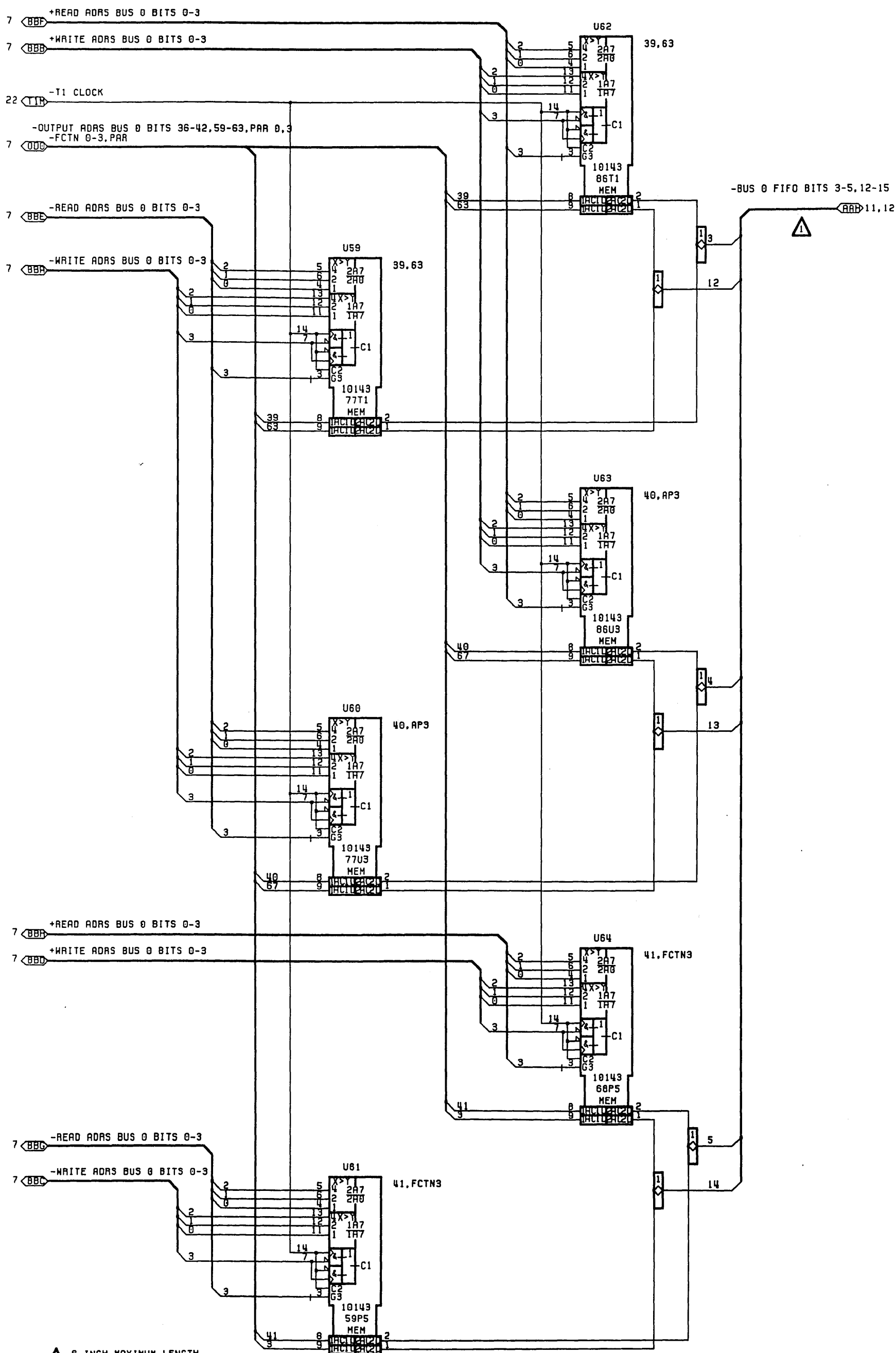
△ 6 INCH MAXIMUM LENGTH



CMI FIFO BUS 0
BITS 0-2,9-11. CM WRITE
CM ADDRESS
TYPE 1JJH

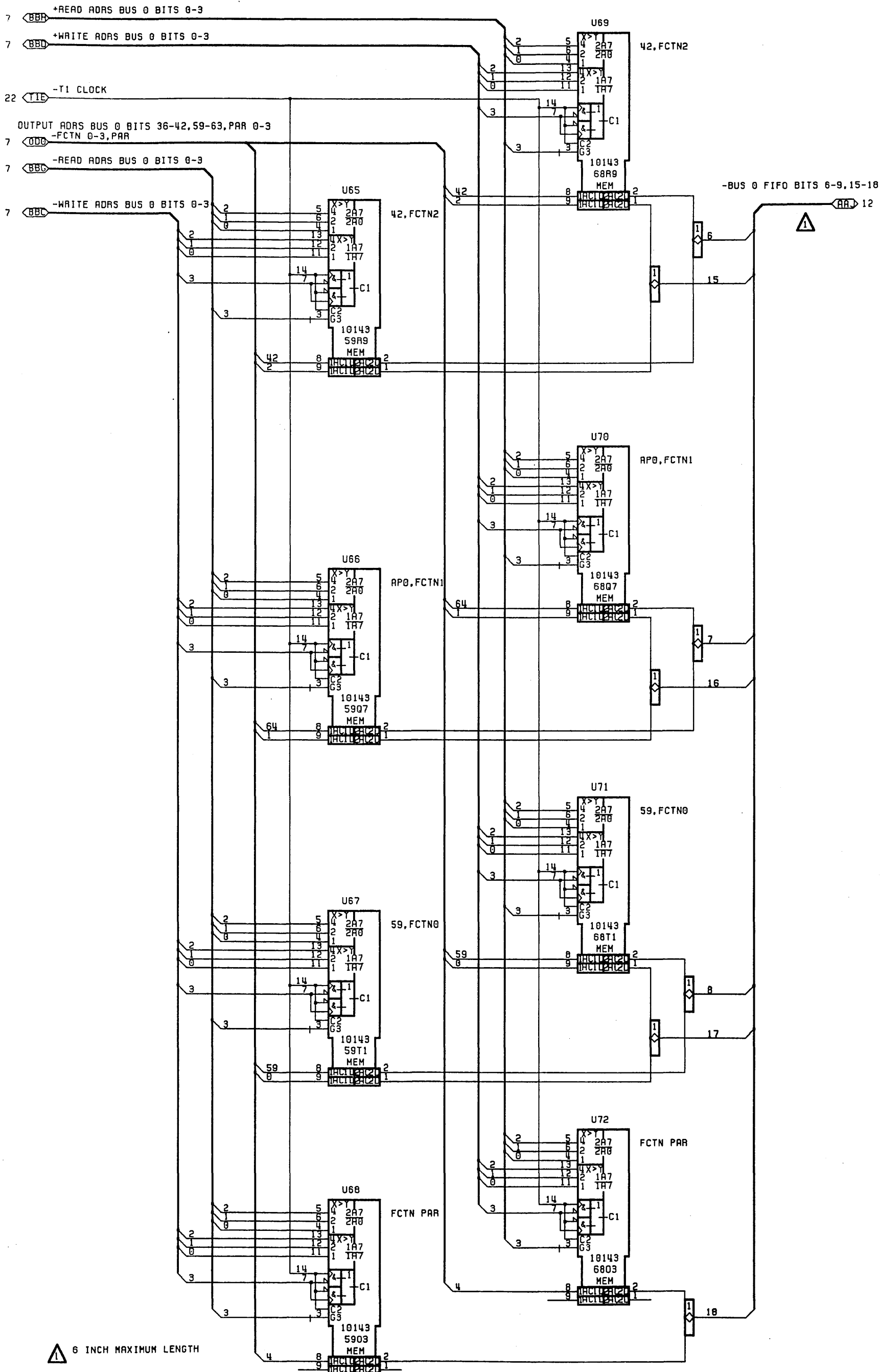
B	DWG NO. 22105674	DATE 12/13/85	REV A
SHEET NO. 8		60462210	PAGE JJ-08

CMI FIFO BUS 0 BITS 3-5,12-15, CM ADRS/FCTN



 CONTROL DATA	CMI FIFO BUS 0	B	DWG NO.	DATE	REV
	BITS 3-5,12-14		22105674	12/13/85	A
	CM ADDRESS/FUNCTION	SHEET NO.	9	68462210	PAGE JJ-89
TYPE 1JH	N				

CMI FIFO BUS 0 BITS 6-8,15-18, CM ADRS/FCTN



 6 INCH MAXIMUM LENGTH



```
CMI FIFO BUS 0
BITS 6-8,15-18
CM ADDRESS/FUNCTION
TYPE 1JH
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D

DWG NO.

DATE

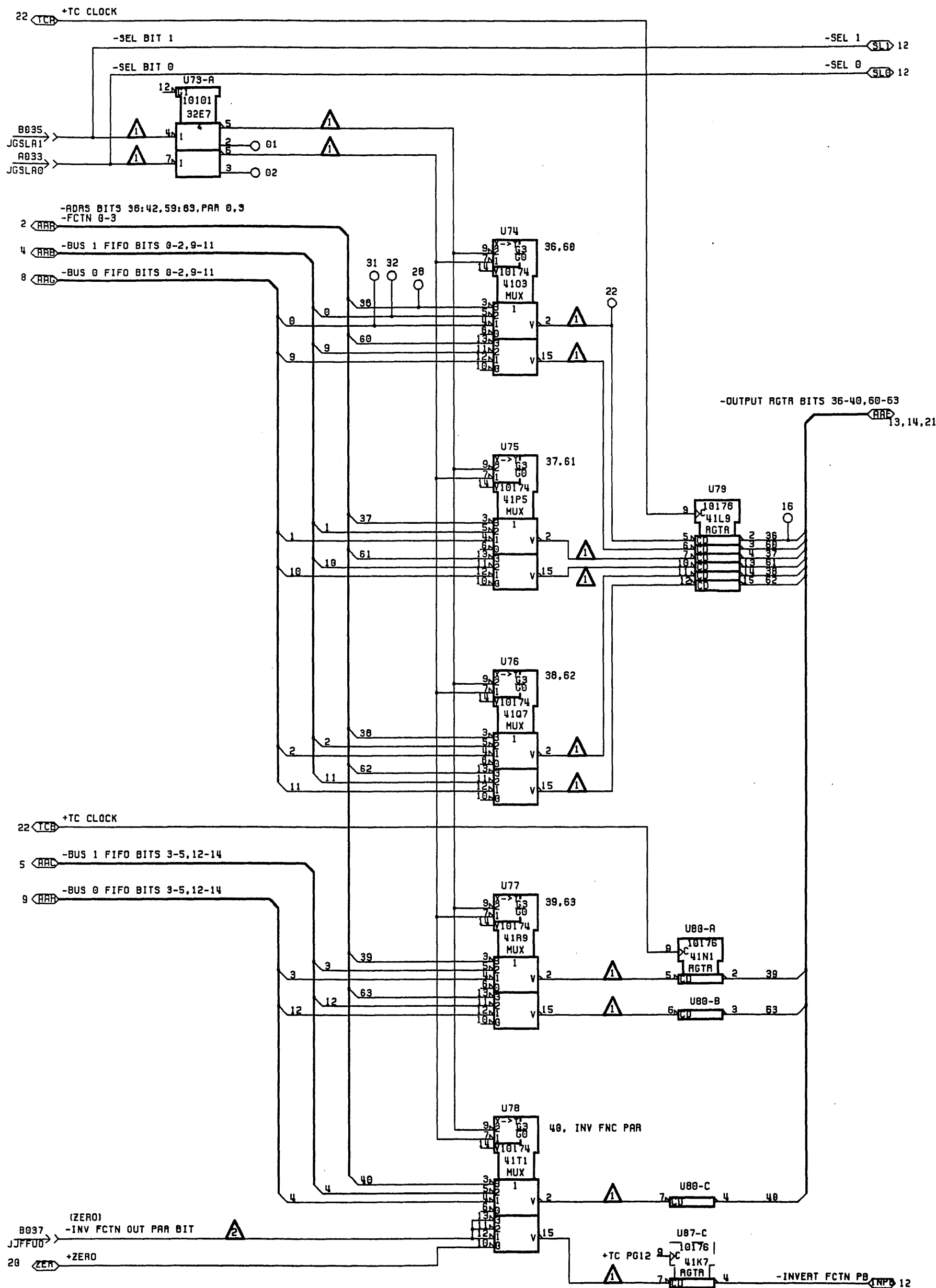
REV

SHEET NO. 10


60462

PAGE JJ-10

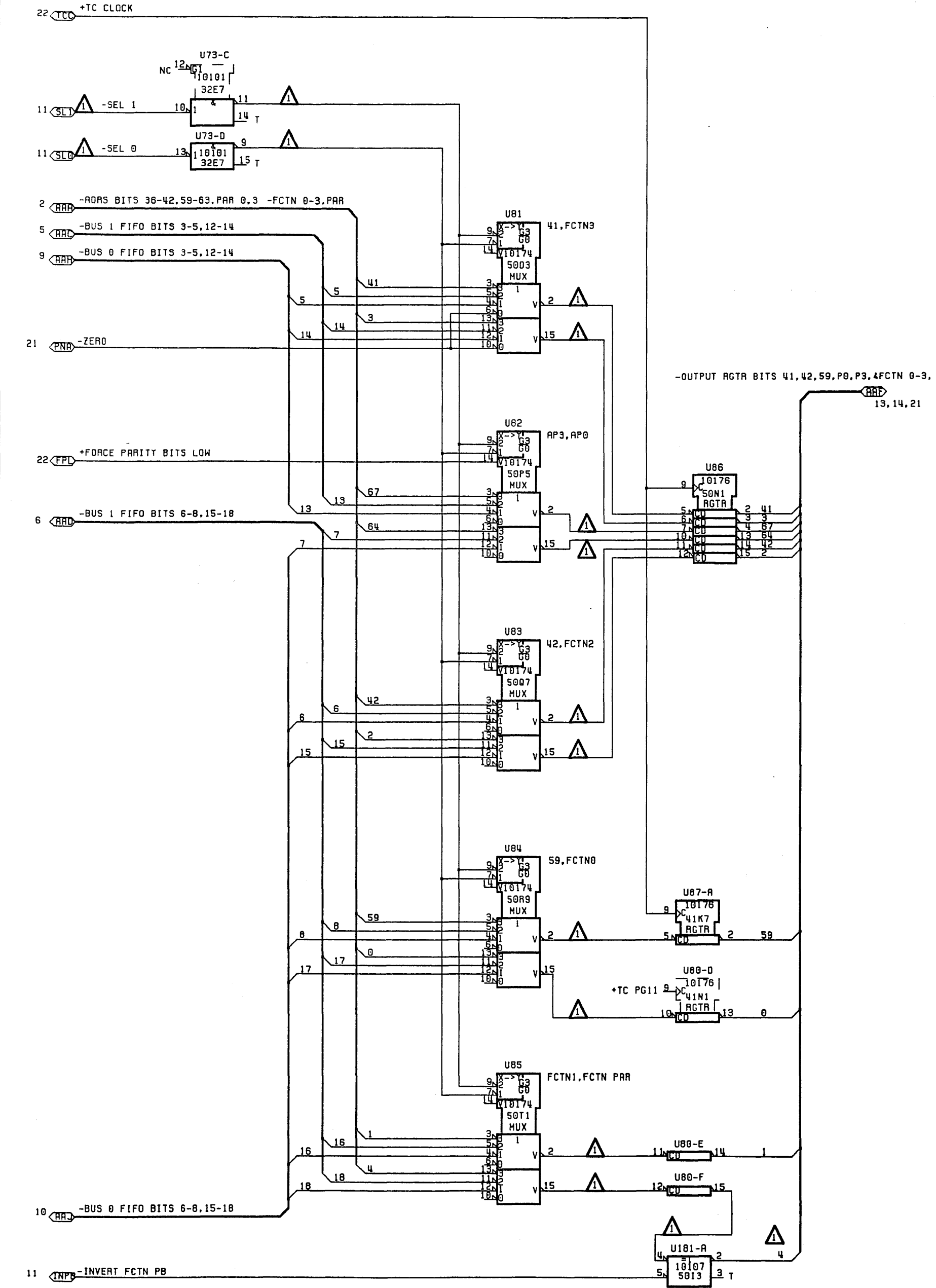
CMI DATA MUX AND OUT RGTR
ADRS BITS 36-40,60-63



4.5 INCH MAXIMUM LENGTH
SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	CMI DATA MUX AND OUTPUT RGTR ADRS BITS 36-40,60-63 TYPE 1JJH	B	DWG NO.	DATE	REV
			22185674	87/18/86	B
			SHEET NO. 11		

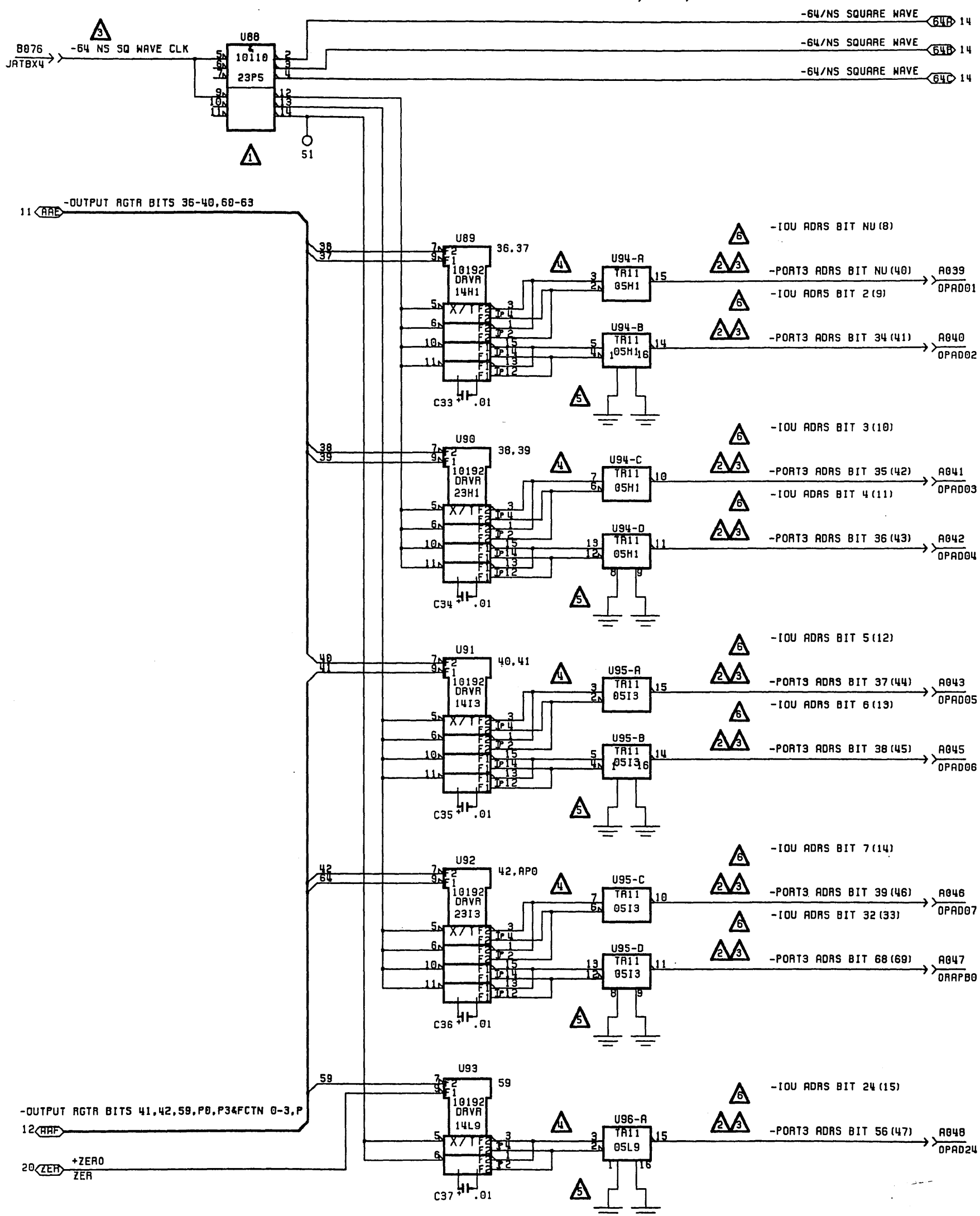
CMI DATA MUX AND OUT RGTR
 ADRS BITS 5-8,13-18,PAR 0-3




4.5 INCH MAXIMUM LENGTH

CONTROL DATA	CMI DATA MUX AND OUTPUT RGTR ADRS BITS 5-8, 13-18		DWG NO. 22105674	DATE 12/13/85	REV A
	TYPE 1JJH		SHEET NO. 12	60462210	PAGE JJ-12

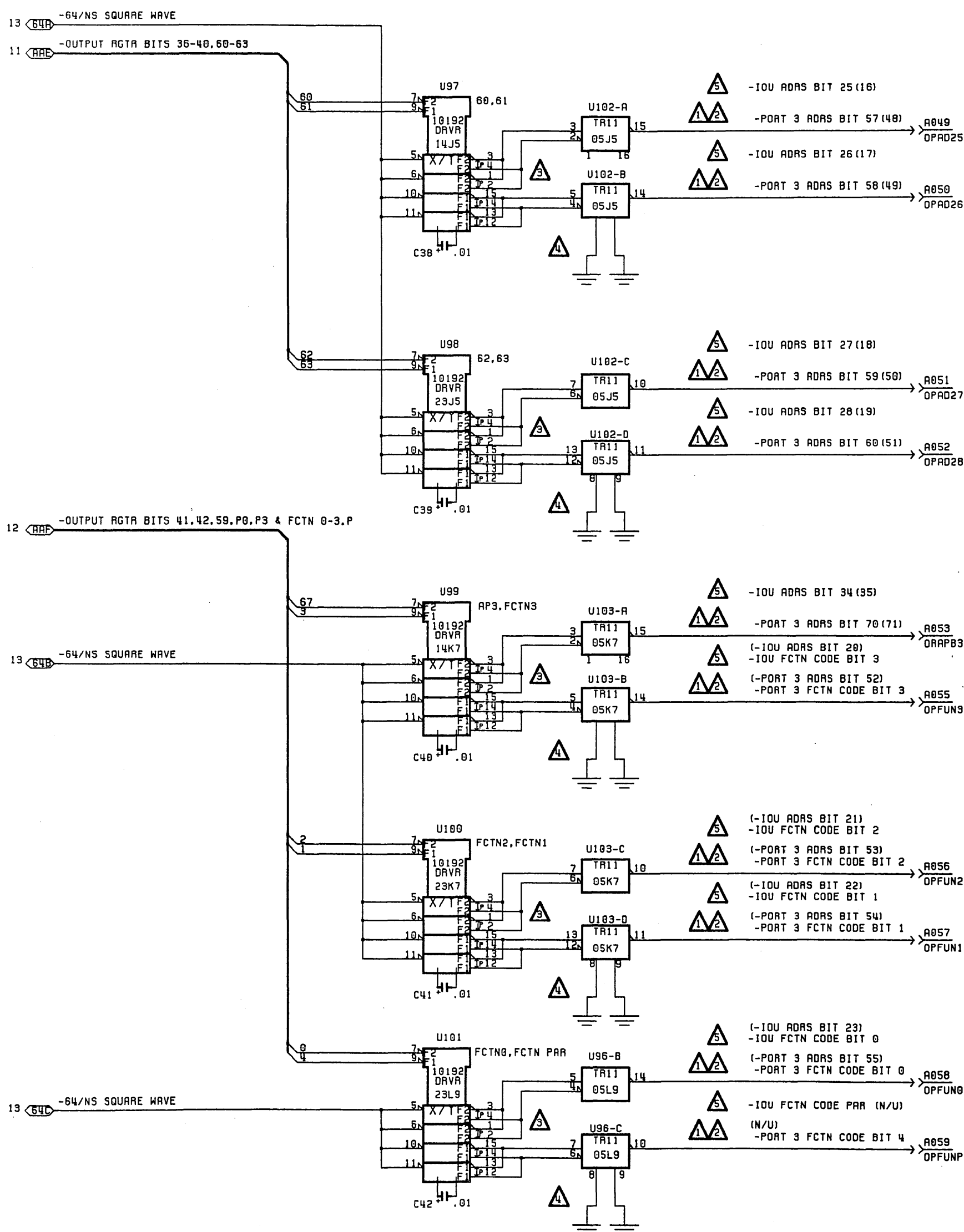
ADRS TRANSMITTERS TO CM BITS 36-42,59,PAR BIT 0



- 1 ALL OUTPUTS SHOULD BE 12 INCH MAXIMUM LENGTH & EQUAL +/- 1 INCH.
- 2 THESE SIGNAL NAMES MATCH THE MODEL 990 CMC DIAGRAM NOMENCLATURE. THE FIRST BIT NUMBER APPLIES TO LOCATION A08; THE SECOND (XX) APPLIES TO A07.
- 3 4.5 INCH MAXIMUM LENGTH
- 4 3 INCH MAXIMUM BETWEEN 10192 & TR11 CHIPS.
- 5 GND PINS 1 & 8 OF THE TR11 CHIPS SHOULD BE GROUNDED AT PIN 16 OF THEIR RESPECTIVE 10192 CHIPS WITH A MINIMUM FOIL WIDTH OF .032 INCHES.
- 6 THESE SIGNAL NAMES MATCH THE MODEL 845, 855, 840, 850, 860, MODEL A OR MODEL S CMC DIAGRAM NOMENCLATURE. THE FIRST NUMBER APPLIES TO LOCATION A08; THE SECOND (XX) APPLIES TO A07.

 CONTROL DATA	ADDRESS TRANSMITTERS TO CM	B	DWG NO.	DATE	REV
	ADDRESS BITS 36-42,59, ADDRESS PARITY BIT 0		22105674	07/18/86	B
	TYPE 1JJH	SHEET NO. 13	60462210	PAGE JJ-13	

ADRS TRANSMITTERS TO CM BITS 60-63,
ADRS PAR BIT 3 & FCTN BITS 0-3, PAR



1 THESE SIGNAL NAMES MATCH THE MODEL 990 CNC DIAGRAM NOMENCLATURE.
THE FIRST BIT NUMBER APPLIES TO LOCATION A08; THE NAME
OR BIT NUMBER IN PARENTHESES APPLIES TO LOCATION A07.

2 4.5 INCH MAXIMUM LENGTH

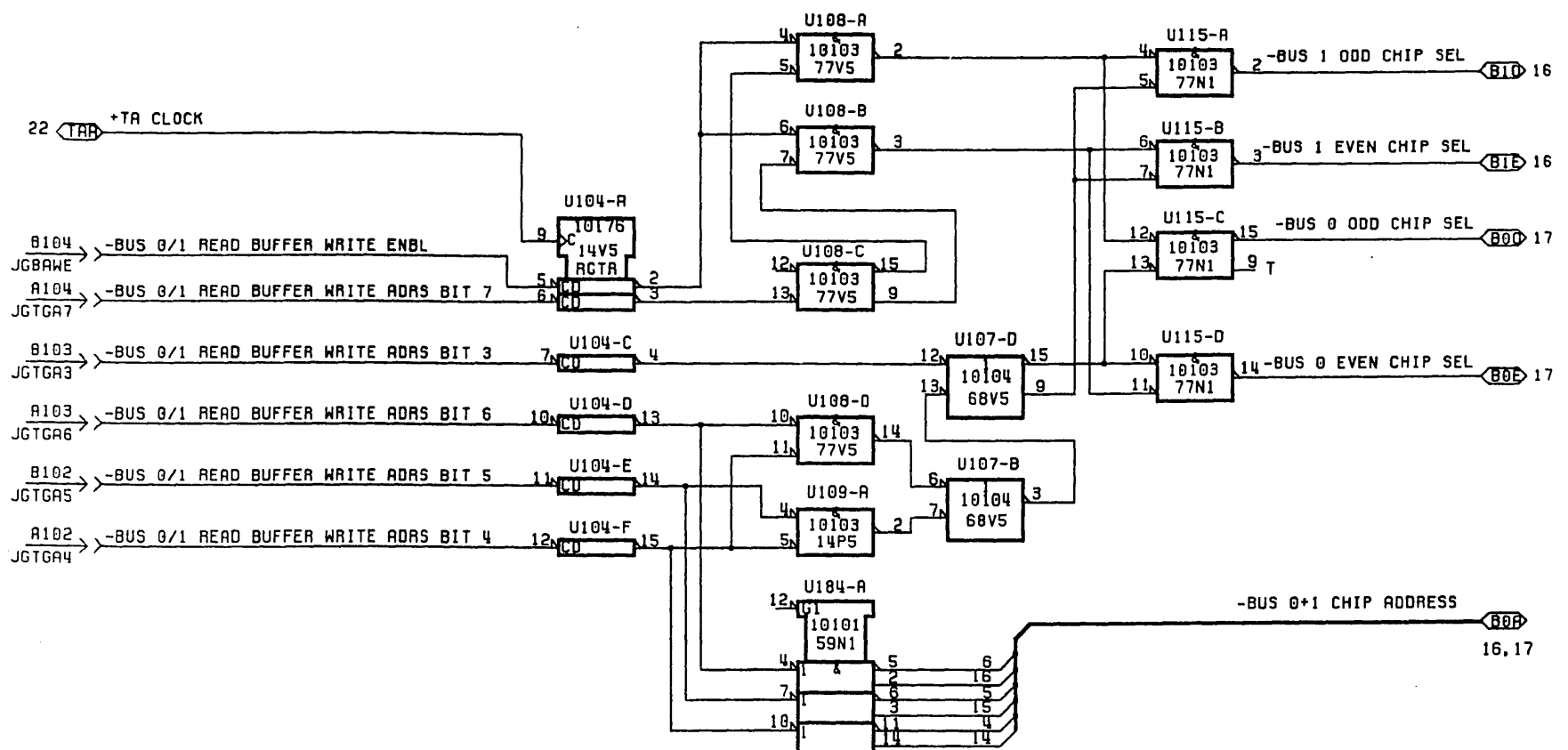
3 3 INCH MAXIMUM BETWEEN 10192 & TR11 CHIPS.

4 GND PINS 1 & 8 OF THE TR11 CHIPS SHOULD BE GROUNDED
AT PIN 16 OF THEIR RESPECTIVE 10192 CHIPS WITH
A MINIMUM FOIL WIDTH OF .032 INCHES.

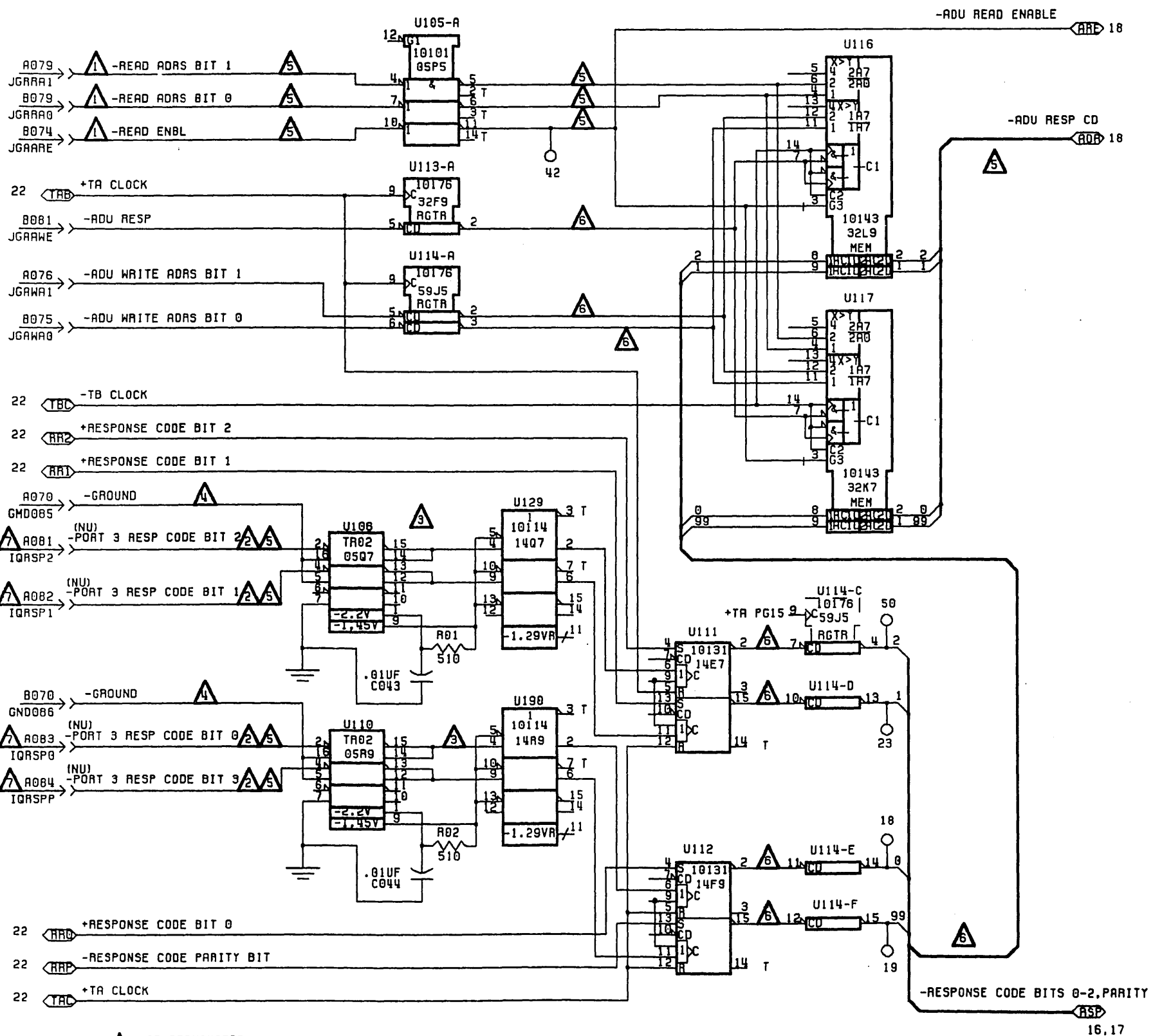
5 THESE SIGNAL NAMES MATCH THE MODEL 845, 855, 940, 850, 860,
MODEL A, OR MODEL S CNC DIAGRAM NOMENCLATURE AT LOCATION A06.
THE BIT IN PARENTHESES APPLIES TO LOCATION A07.

CONTROL DATA	ADDRESS TRANSMITTERS TO CM ADDRESS BITS 60-63, AP3 FCTN BITS 0-3, FCTN PAR TYPE 1JJH	8	DWG NO. 22105674	DATE 12/13/85	REV A
			SHEET NO. 14	60462210	PAGE JJ-14

BUS WRITE ADRS DECODER FOR RESP CODE MEM



RESP CODE DESKEW AND ADU INPUT BUFFER



- 1 NOT TERMINATED
- 2 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.
- 3 2 INCH MAX BETWEEN TR02 AND 10114
- 4 SEPARATE LINES TO CONNECTOR PINS AND PARALLEL TO ASSOCIATED SIGNAL LINES
- 5 4.5 INCH MAXIMUM LENGTH
- 6 9 INCH MINIMUM LENGTH

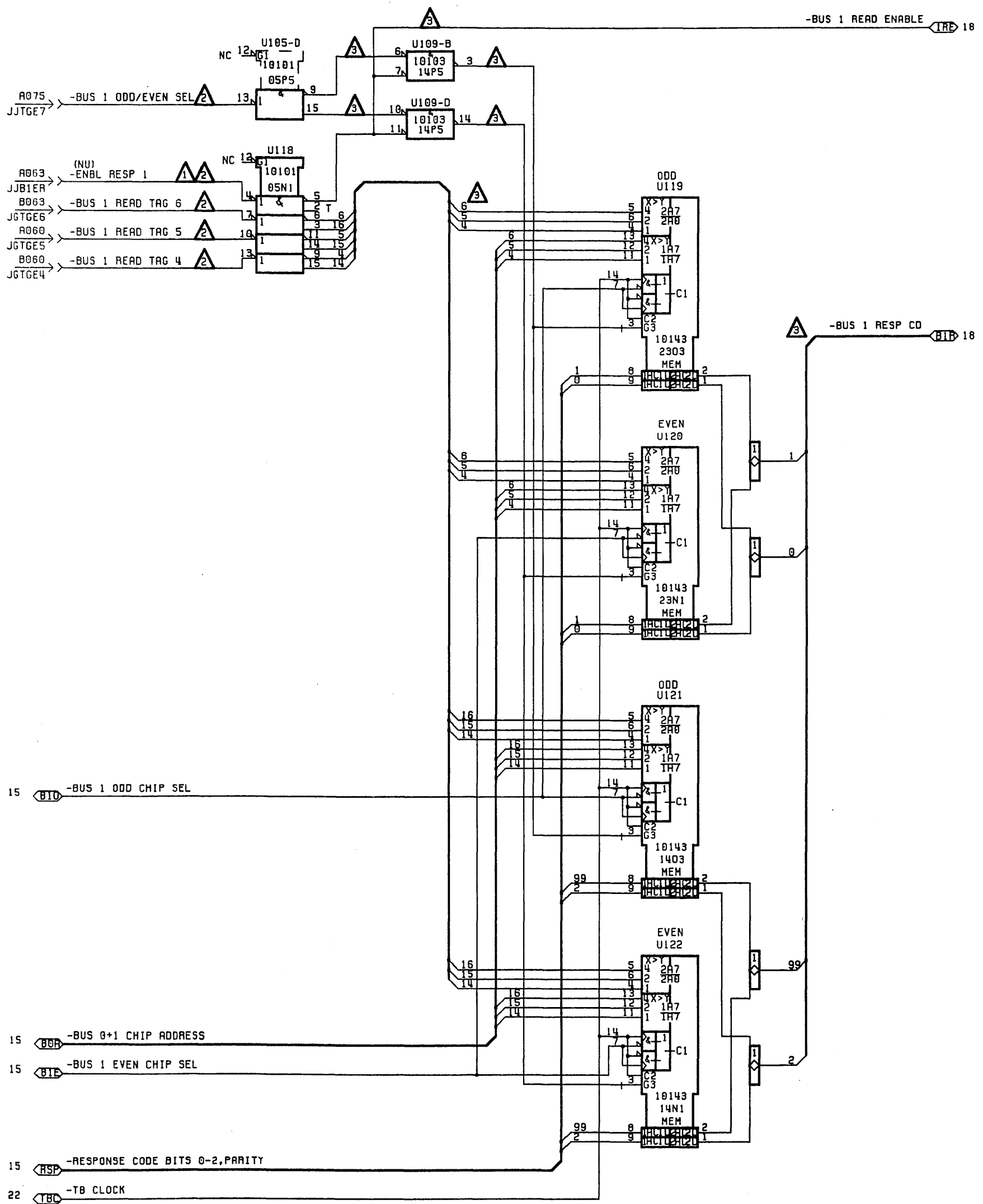
PORT 3 NAME APPLIES TO MODEL 990 CMC. OTHER MODELS' NAMES ARE -IOU RESPONSE CODE BITS 0-2/PAR.



BUS WRITE ADDRESS DECODE AND
RESPONSE CODE DESKEW &
ADU INPUT BUFFER
TYPE 1JJH

DWG NO.	DATE	REV
22105674	12/19/85	A
SHEET NO.	PAGE	REV
15	60462210	JJ-15


BUS 1 RESP CODE MEM



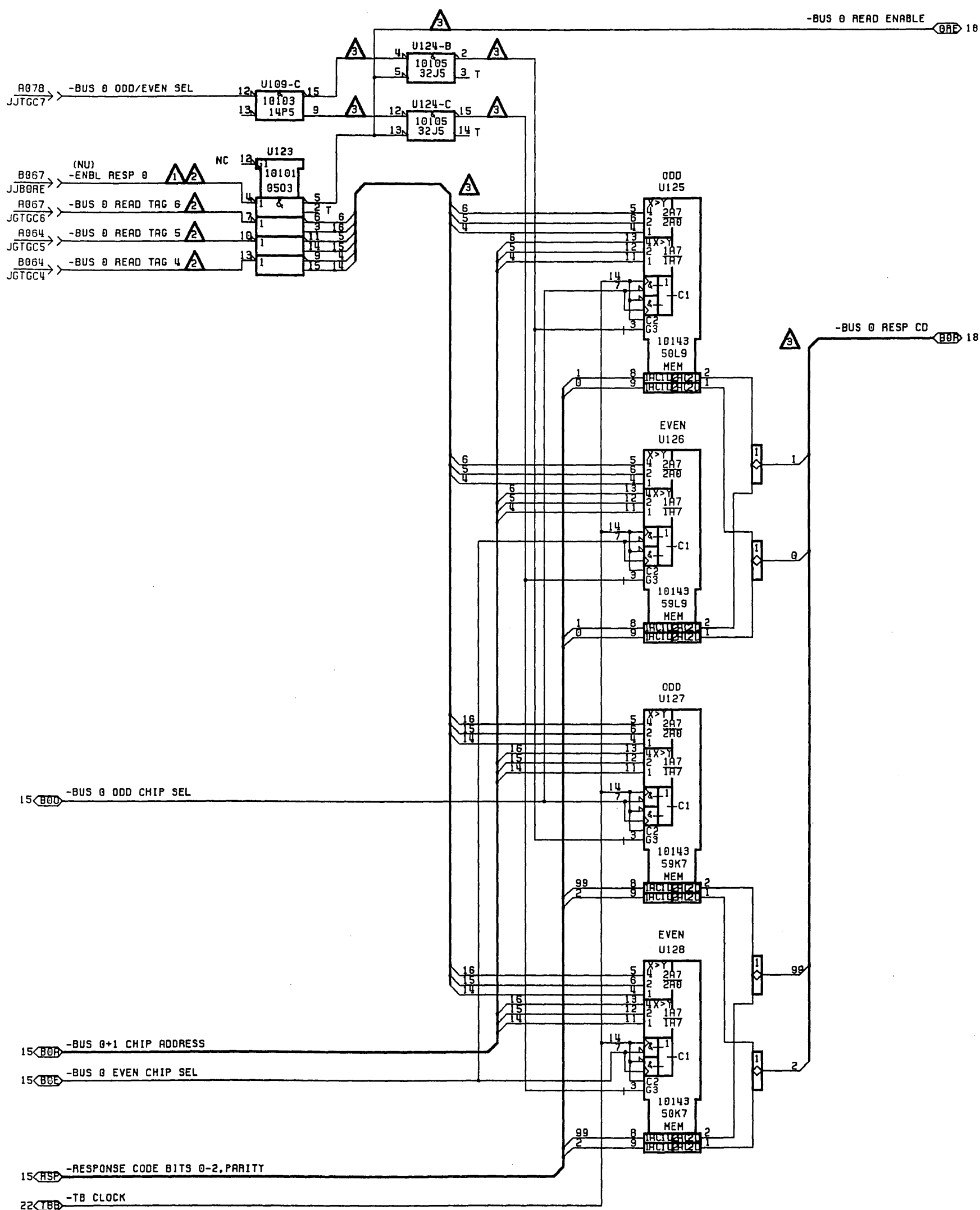
1 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

2 3 INCH MAXIMUM LENGTH


3 4.5 INCH MAXIMUM LENGTH

 CONTROL DATA	BUS 1 RESPONSE CODE MEMORY		B	DWG NO.	DATE	REV
	TYPE 1J1H			22105674	12/13/85	A
			SHEET NO. 16	68462210	PAGE JJ-16	

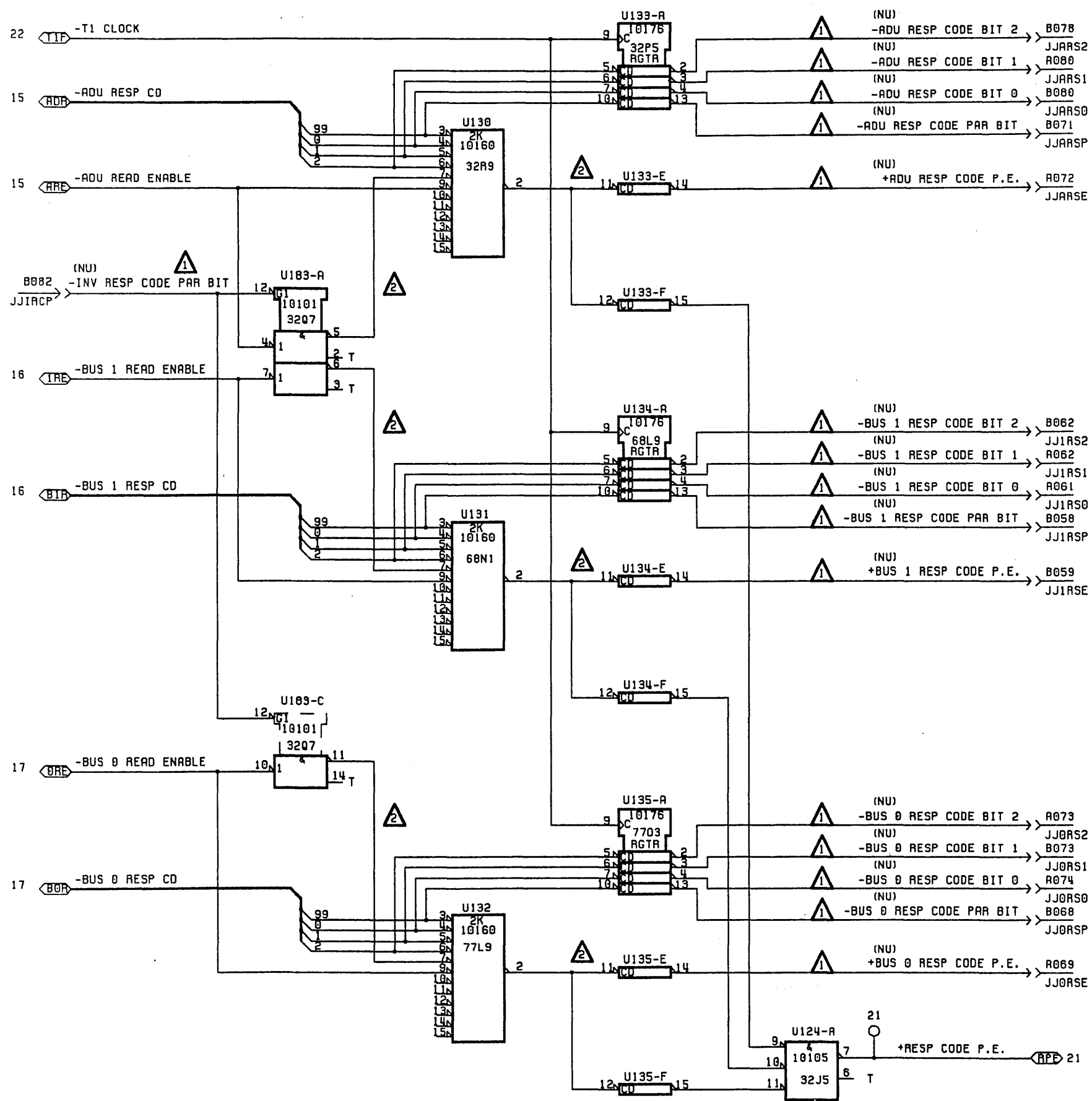
BUS 0 RESP CODE MEM



- 1 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.
- 2 3 INCH MAXIMUM LENGTH
- 3 4.5 INCH MAXIMUM LENGTH

 CONTROL DATA	BUS 0 RESONSE CODE MEMORY		B	DWG NO. 22105674	DATE 12/13/85	REV A
	TYPE 1JJH		SHEET NO. 17	60462210		PAGE JJ-17

RESP CODE PAR CHECKER



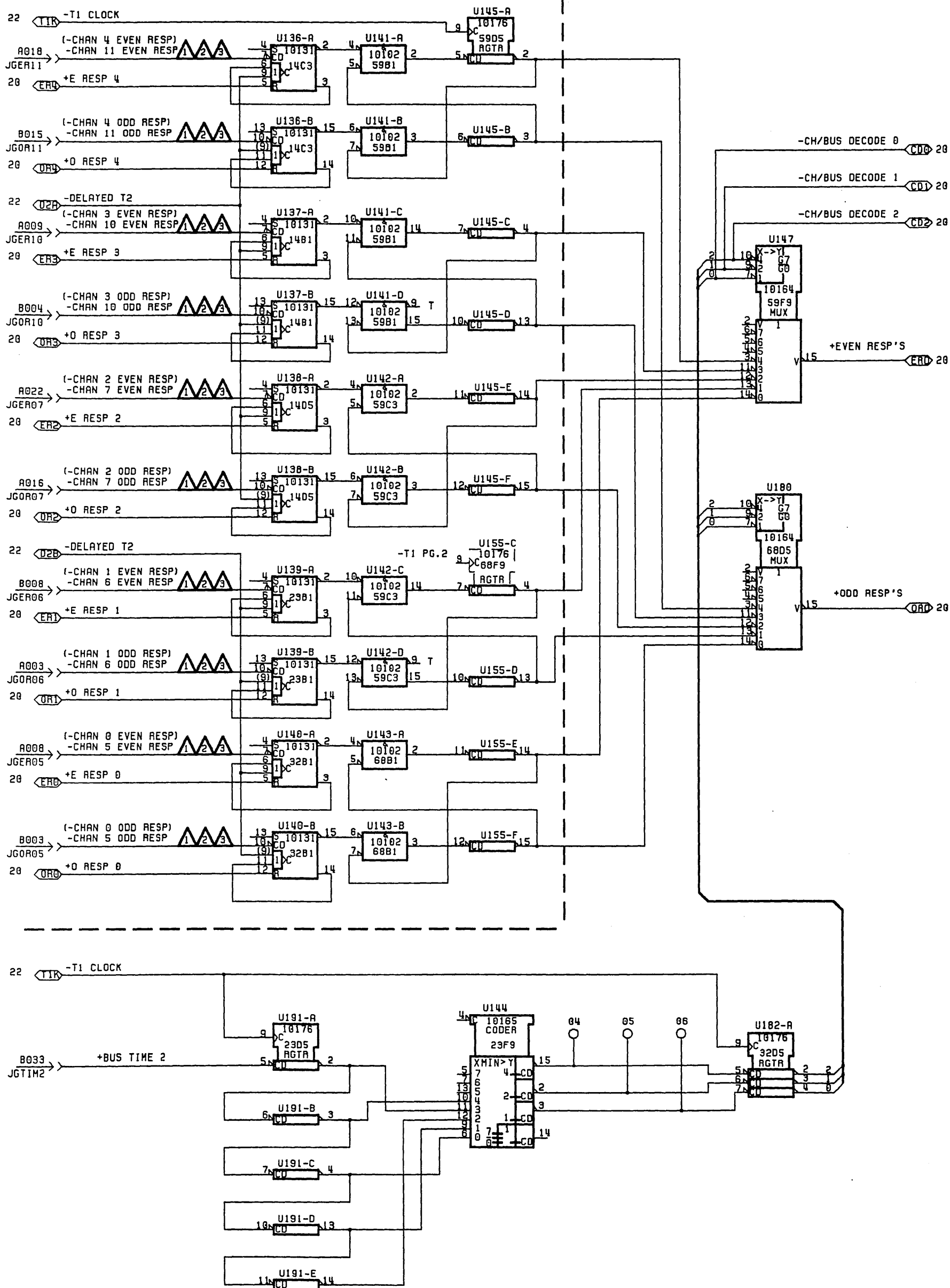
1 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

2 4.5 INCH MAXIMUM LENGTH

CD CONTROL DATA	RESPONSE CODE PARITY CHECK TYPE 1JJH	B	DWG NO. 22185674	DATE 12/13/85	REV A
			SHEET NO. 18	60462210	PAGE JJ-18

HLDG RGTRS


RESP SEL



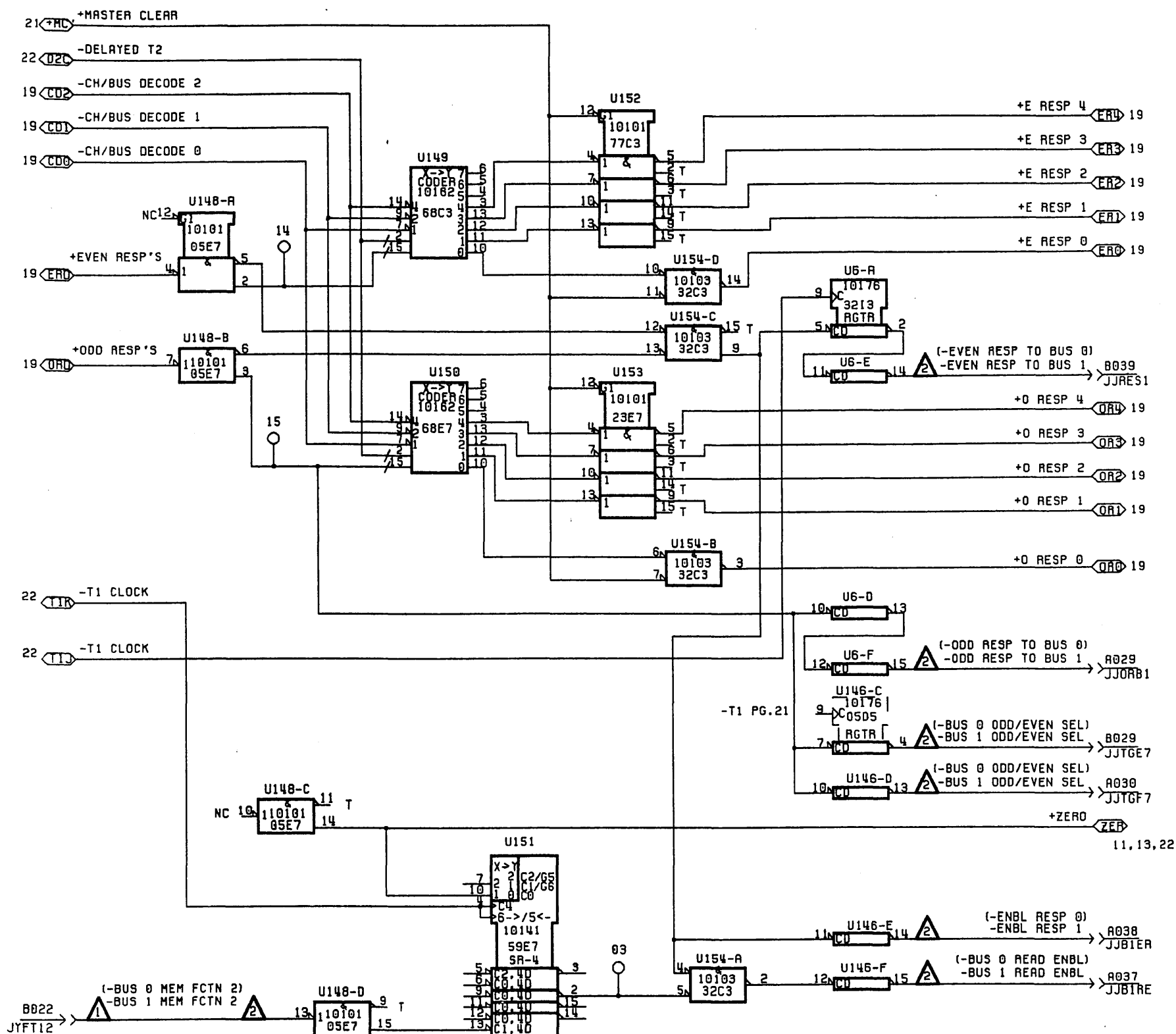
1 NOT TERMINATED ON THIS BOARD

2 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

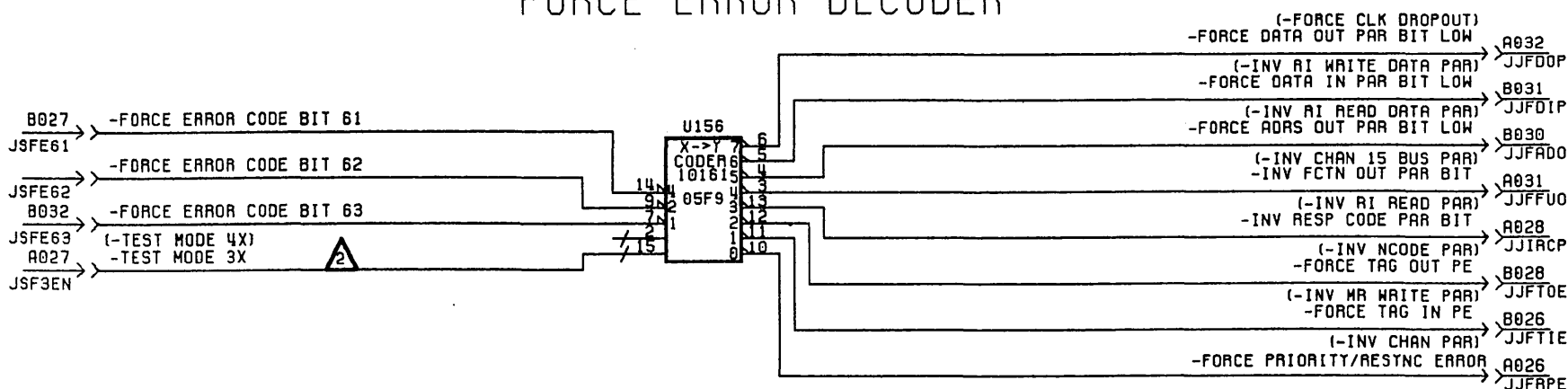
3 4.5 INCH MAXIMUM LENGTH

 CONTROL DATA	HOLDING REGISTERS AND BUS RESPONSE SELECT TYPE 1JH	8	DWG NO.	DATE	REV
			22185674	07/18/86	8
			SHEET NO. 19		

CHAN RESP SEL




FORCE ERROR DECODER



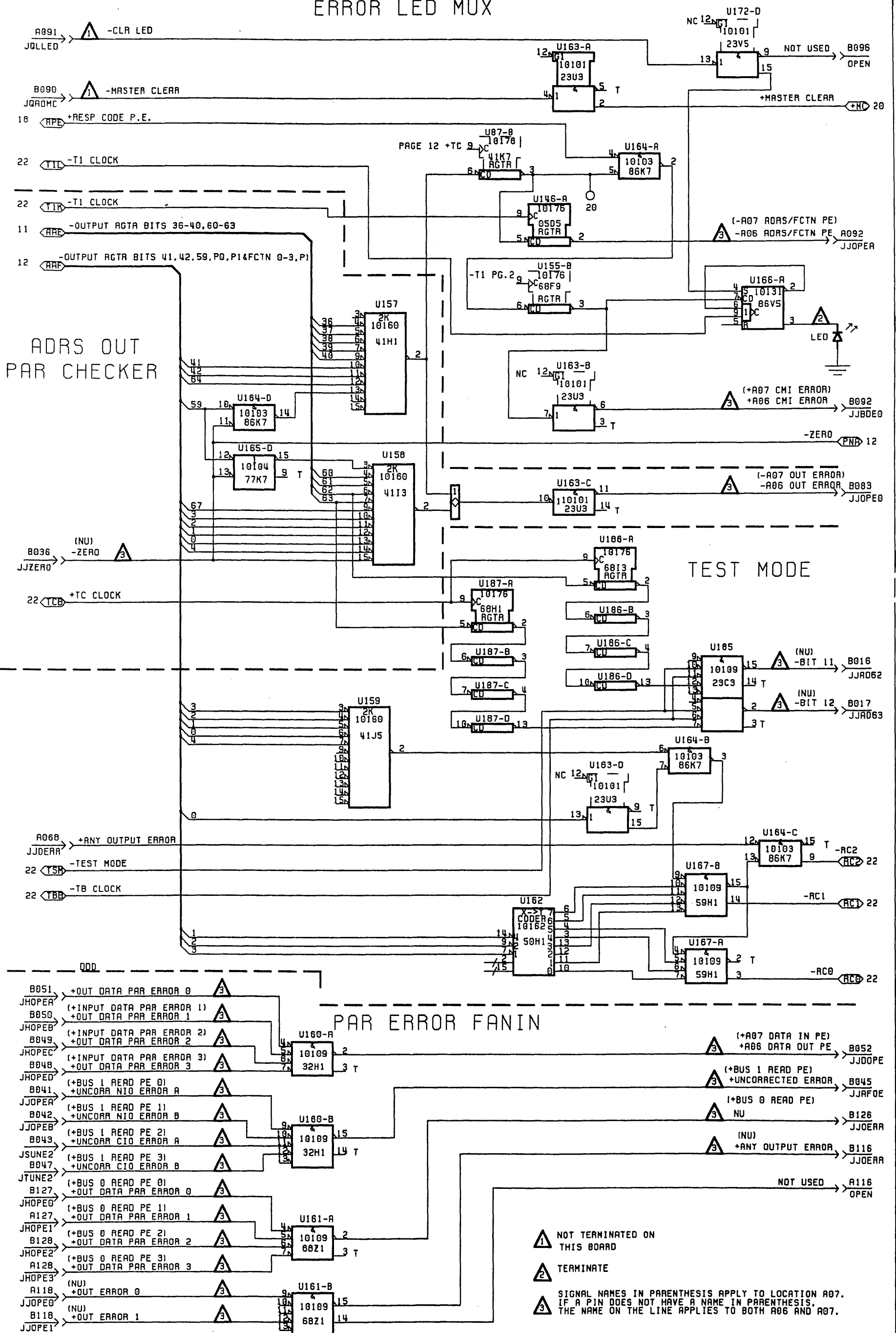
CMI FORCE ERRORS (3X) MUX DECODES FOR LOC A06	
7	FORCE DATA OUT PAR BIT LOW
6	FORCE DATA IN PAR BIT LOW
5	FORCE ADRS OUT PAR BIT LOW
4	INV FCTN OUT PAR BIT
3	INV RESP CODE PAR BIT
2	FORCE TAG OUT PAR ERROR
1	FORCE TAG IN PAR ERROR
0	FORCE REQ PRIORITY RESYNC ERROR

MAC FORCE ERRORS (4X) MUX DECODES FOR LOC A07	
7	FORCE CLK DROPOUT
6	INV RI WRITE DATA PAR
5	INV RI READ DATA PAR
4	INV CHAN 15 BUS PAR
3	INV RI READ PAR
2	INV NCODE PAR
1	INV MR WRITE PAR
0	INV CHAN PAR

- 1 NOT TERMINATED ON THIS BOARD AND 3 INCH MAXIMUM LENGTH
 2 SIGNAL NAMES IN PARENTHESES APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESES, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	CHANNEL RESPONSE SELECT FORCE ERROR DECODER		B	DWG NO. 22105674	DATE 07/18/86	REV B
	TYPE 1.1JH			SHEET NO. 20	60462210	PAGE JJ-20


ERROR LED MUX



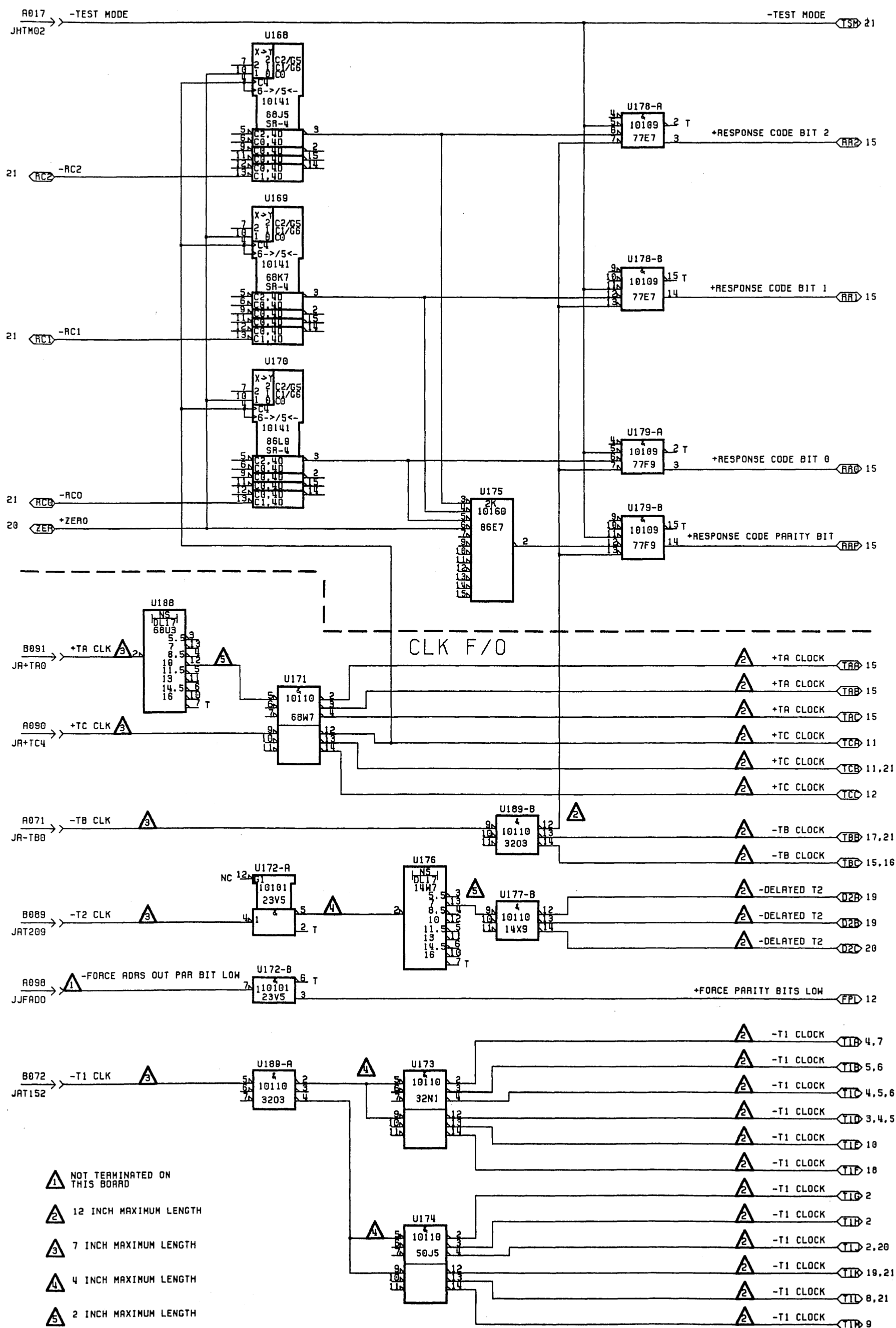
NOT TERMINATED ON THIS BOARD

TERMINATE

SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07. IF A PIN DOES NOT HAVE A NAME IN PARENTHESIS, THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	ERROR LED MUX, ADDRESS OUT PARITY CHECK AND TEST MODE	B	DWG NO.	DATE	REV
			22105674	12/13/85	A
	TYPE 1JJH		SHEET NO. 21	60462210	PAGE JJ-21

TEST MODE




 CONTROL DATA	TEST MODE AND CLOCK FANOUT TYPE 1JJH	B	DWG NO. 22105674	DATE 07/18/86	REV B
		SHEET NO. 22	60462210	PAGE	JJ-22

TP	SHT	SIGNAL NAME	TP	SHT	SIGNAL NAME
01	11	+SEL BIT 1	27	07	-ADRS BUS0 BIT36 (43)
02	11	+SEL BIT 0	28	11	-ADU BIT 36 (43)
03	20	+BUS 1 (0) WRITE	29	07	-WR ADRS BUS0 BIT 2
04	19	+BUS TIME CD BIT 2	30	07	-WR ADRS BUS0 BIT 0
05	19	+BUS TIME CD BIT 1	31	11	-BUS 0 BIT 36 (43)
06	19	+BUS TIME CD BIT 0	32	11	-BUS 1 BIT 36 (43)
07	02	-RD ADRS ADU BIT 0	33	07	-RD ADRS BUS0 BIT 3
08	02	-RD ADRS ADU BIT 2	34	07	-RD ADRS BUS0 BIT 0
09	02	-RD ADRS ADU BIT 1	35	07	-RD ADRS BUS0 BIT 1
10	02	-ADU ADRS BIT 36 (43)	36	07	-RD ADRS BUS0 BIT 2
11	02	-WRT ADRS ADU BIT 2	37	03	-WR ADRS BUS1 BIT 0
12	02	-WRT ADRS ADU BIT 1	38	03	-RD ADRS BUS1 BIT 0
13	02	-WRT ADRS ADU BIT 0	39	03	-WR ADRS BUS1 BIT 2
14	20	-BUS 1 (0) EVEN RESP	40	03	-WR ADRS BUS1 BIT 1
15	20	-BUS 1 (0) ODD RESP	41	03	-ADRS BUS1 BIT36 (43)
16	11	-OUTPUT BIT 36 (43)	42	15	-ADU READ ENABLE
17	02	-ADU REQUEST	43	03	-RD ADRS BUS1 BIT 1
18	15	-RESP CODE BIT 0 (NU)	44	03	-RD ADRS BUS1 BIT 2
19	15	-RESP CODE PAR (NU)	45	03	-RD ADRS BUS1 BIT 3
20	21	+OUTPUT RGTR P.E.	46	03	+WR ADRS BUS1 BIT 3
21	18	+RESP CODE P.E. (NU)	47	03	-WR ADRS BUS1 BIT 3
22	11	-MUX BIT 36 (43)	48	07	-WR ADRS BUS0 BIT 3
23	15	-RESP CODE BIT 1 (NU)	49	07	+WR ADRS BUS0 BIT 3
24	07	-WR ADRS BUS0 BIT 1	50	15	-RESP CODE BIT 2 (NU)
25			51	13	-64 N/S SQ WAVE
26					

CONNECTOR PINS	
GND	A014,B014,A024,B024,A034,B034,A054,B054,A065,B065,A066,B066,A077,B077,A097,B097,A107,B107,A117,B117,B046,B053,B061,B069,A126
-5.2V	A001,B001,A002,B002,A129,B129,A130,B130
-2.2V	A007,B007,A044,B044,A087,B087,A124,B124
+5V	(NOT USED)
TERM	NONE
UNUSED	NONE

3 SIGNAL NAMES IN PARENTHESIS APPLY TO LOCATION A07.
IF A TP DOES NOT HAVE A NAME IN PARENTHESIS,
THE NAME ON THE LINE APPLIES TO BOTH A06 AND A07.

 CONTROL DATA	CMI ADDRESS BOARD TESTPOINTS AND SIGNAL NAMES AND CONNECTOR PINS TYPE 1JJH	8	DWG NO.	DATE	REV
			22105674	12/13/85	B
			SHEET NO. 23		60462210

[illegible][illegible]

1. The first step in the process is to identify the problem. This involves gathering information about the situation and understanding the needs of the stakeholders involved.

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seal edges with tape only.

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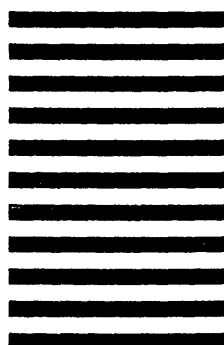
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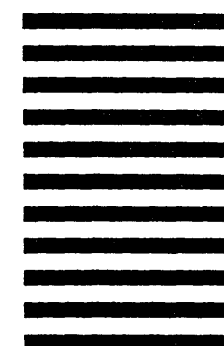
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COMMENT SHEET

MANUAL TITLE: AT478-A/B, AT481-A/B IOU and Associated Equipment
Hardware Maintenance Manual, Volume 2, Book 1 of 3
PUBLICATION NO.: 60462210 REVISION: P

NAME: _____

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1. The first part of the report is a summary of the work done during the year. It includes a list of the projects completed and a brief description of the results achieved. The second part of the report is a detailed account of the work done on each project. It includes a description of the objectives of the project, the methods used, the results obtained, and a discussion of the significance of the results.

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3. The third part of the report is a summary of the work done during the year. It includes a list of the projects completed and a brief description of the results achieved. The fourth part of the report is a detailed account of the work done on each project. It includes a description of the objectives of the project, the methods used, the results obtained, and a discussion of the significance of the results.

CONCLUDED

4. The fourth part of the report is a detailed account of the work done on each project. It includes a description of the objectives of the project, the methods used, the results obtained, and a discussion of the significance of the results. The fifth part of the report is a summary of the work done during the year. It includes a list of the projects completed and a brief description of the results achieved.

5. The fifth part of the report is a summary of the work done during the year. It includes a list of the projects completed and a brief description of the results achieved. The sixth part of the report is a detailed account of the work done on each project. It includes a description of the objectives of the project, the methods used, the results obtained, and a discussion of the significance of the results.

6. The sixth part of the report is a detailed account of the work done on each project. It includes a description of the objectives of the project, the methods used, the results obtained, and a discussion of the significance of the results. The seventh part of the report is a summary of the work done during the year. It includes a list of the projects completed and a brief description of the results achieved.

CONCLUDED

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